

LiDAR Transmitter Driver White Paper

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ABSTRACT

Large-scale automotive deployment of 905 nm multi-junction VCSELs (vertical-cavity surface-emitting lasers) places combined demands on the TX driver: 60–80 V voltage rating, 20–50 A peak current, and nanosecond pulse edges. Starting from the $V = L \cdot di/dt$ loop constraint, this paper derives the drive-voltage budget, analyzes the system-level design considerations of the "high-side charging + low-side pulsing" architecture, reviews the eye-safety protection essentials required by IEC 60825-1 and ISO 26262, and presents a full-portfolio selection guide covering three application classes: Flash solid-state, scanning, and integrated power stage. 3PEAK supports these with a complete TX-driver portfolio — high-side charging (TPM8909Q/AQ), low-side pulsing (TPM8918Q/BQ), an integrated power stage (TPM8915Q), and GaN gate drivers (TPM102x/TPM202x).

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1. Introduction

Automotive LiDAR is moving from a premium ADAS option toward a high-volume, cost-sensitive standard feature. This transition puts the transmitter (TX) at the center of the design effort: large-scale 905 nm multi-junction VCSEL arrays call for 60–80 V rail voltages, 20–50 A peak currents, and sub-2 ns pulse edges, all while meeting IEC 60825-1 eye-safety limits and ISO 26262 functional-safety targets and keeping the bill of materials low.

Meeting these requirements takes a coordinated set of design choices spanning voltage, current, edge rate, parasitic inductance, thermal limits, and channel count. Starting from the governing $V = L \cdot di/dt$ loop constraint, this white paper derives the TX drive-voltage budget, examines the design considerations of the high-side charging + low-side pulsing topology, covers the eye-safety protections required for series production, and maps a complete driver portfolio to three application classes — Flash solid-state, scanning, and integrated power stage. The aim is to give designers a clear view of the full TX-driver solution space and the 3PEAK portfolio that spans it.

2. LiDAR Scanning Architecture Classification and Technology Evolution

Scanning Architecture Classification

The beam-scanning method determines the LiDAR architecture and its TX-driver requirements. Before discussing the TX-driver electrical design, this section classifies automotive LiDAR by beam-steering principle. The three main classes are mechanical, semi-solid-state, and solid-state. The discussion then explains how each architecture affects channel count, peak current, and timing.

Automotive LiDAR Scanning Architectures

By beam steering: Mechanical → Semi-solid-state → Solid-state (no moving parts)

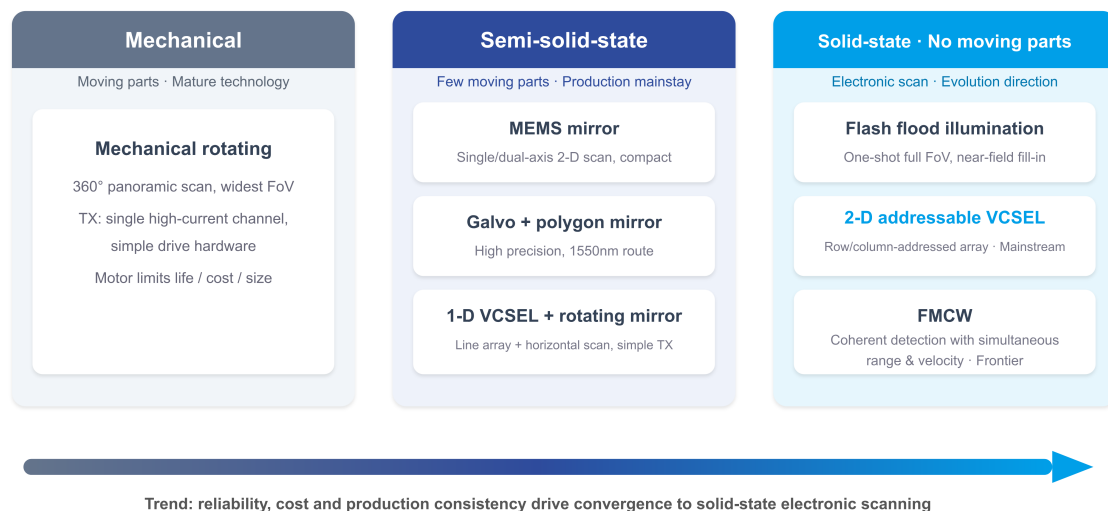


Figure 2-1 Classification Of Automotive LiDAR Scanning Architectures

- Mechanical rotating (mechanical): the entire transmit/receive module rotates to achieve 360° panoramic scanning; the technology is mature and the field of view (FoV) is wide, but the motor brings lifetime/cost/size issues. In passenger-car front-mounted applications it is gradually being replaced by solid-state designs, while it remains widely deployed in Robotaxi and robotics scenarios (mowing, delivery, AGV/AMR).

- MEMS mirror (semi-solid-state): a single-/dual-axis micromirror performs 2-D scanning; a single emitter delivers high-resolution coverage in a compact structure; the mirror aperture limits the receive aperture, constraining long-range signal-to-noise ratio (SNR), and it remains a moving micro-mechanical component. Wang et al. review MEMS scanning mirrors for LiDAR in Micromachines (2020).
- 1-D VCSEL array + rotating mirror or MEMS mirror (semi-solid-state): the transmitter is a vertical line array that directly covers the vertical FoV, eliminating vertical scanning; only single-axis horizontal scanning is needed. TX hardware is simple (single channel, high current), but mechanical parts remain, and all VCSELs fire every frame, so per-device duty cycle and thermal load are higher than in 2-D zone-addressed schemes.
- Flash (flood illumination, solid-state): the transmitter illuminates the entire field of view at once while a 2-D detector array on the receive side captures in parallel; there is no scanning mechanism and the frame rate is set by electronic timing; the energy is spread across the full field of view, suiting near-field blind-spot coverage.
- 2-D addressable VCSEL array (solid-state): row-column matrix electronic addressing with zone illumination, no moving parts; each emitter is lit for only about 1/N of the time per frame (N being the number of addressed zones, e.g., the row count), correspondingly lowering the per-device average thermal load, and supporting region-of-interest (ROI) adaptive illumination. This comes at the cost of markedly higher TX-driver complexity: independent per-channel charge/discharge, matrix addressing, reverse-bias management, and channel-to-channel crosstalk.
- FMCW (frequency-modulated continuous wave): replaces pulsed time-of-flight with coherent detection and beat-frequency ranging, acquiring range and velocity simultaneously; it is a detection scheme rather than a scanning method, is not directly related to pulsed TX drive, and is not covered further in this paper.

Passenger-car front-mounted applications are accelerating toward solid-state designs, gradually displacing mechanical rotating and MEMS mirror solutions. The 2-D addressable VCSEL array implements flexible illumination patterns electronically and offers structural gains in reliability, cost, and volume-production consistency, but demands a higher level of multi-channel integration from the TX driver; commercial addressable multi-junction VCSEL arrays of this kind are described by Lumentum.

2.1 TX Requirements and Matching Driver Architectures for Different LiDAR Types

Table 2-1 LiDAR Types vs. TX Driver Requirements

LiDAR Type	Scanning Method	Typical Laser Source	TX Requirement Profile	Matching Driver Architecture
Mechanical rotating	360° mechanical rotation	Mainly EEL (edge-emitting laser)	Extremely high single-pulse energy, single-channel high current	Single-channel GaN low-side driver
1-D scanning (semi-solid-state)	1-D VCSEL line array + rotating mirror or MEMS mirror	EEL, 1-D VCSEL array	High single-pulse energy, single or few channels	Single- or few-channel GaN low-side driver
2-D solid-state (Flash or addressable)	No moving parts, 2-D VCSEL array with flood or addressable zone illumination	2-D VCSEL array	Multi-channel matching, high homogeneity requirements	Multi-channel low-side driver + high-side array charging
FMCW coherent LiDAR	Coherent detection scheme, compatible with various scanning methods	Narrow-linewidth continuous-wave laser	Coherent detection, direct velocity measurement	Pulsed drive not applicable (not covered in this paper)

2.2 Technology Generation Evolution: Gen1 → Gen2 → Gen3

Table 2-2 Automotive LiDAR Technology Generation Evolution

Generation	TX Side	RX Side	Scanning Method	Approximate Timeframe
Gen1	EEL + mechanical rotation	APD (avalanche photodiode)	360° mechanical rotation	~2017–2020
Gen2	1-D VCSEL array + rotating mirror or MEMS mirror	Linear SPAD (single-photon avalanche diode) array	Semi-solid-state	~2021–2024
Gen3	2-D addressable VCSEL array	2-D SPAD array	Solid-state electronic scanning	From 2025

The core drivers of Gen1 → Gen2 were VCSELs replacing EELs (circularly symmetric beam spot, low wavelength temperature drift, array integration and cost advantages) and SPADs replacing APDs (single-photon sensitivity lowering TX power requirements); Gen2 has reached volume production in vehicles. Gen2 → Gen3 stems from three physical bottlenecks: photon utilization, thermal management, and flexible region-of-interest control. The engineering cost of breaking through these bottlenecks shows up chiefly as a significant rise in TX-driver complexity, which is the main thread of the chapters that follow. Liang et al. describe this evolution from an industry perspective in Nature Communications (2024).

3. Core Constraints of the TX Driver

System Background and Loop Inductance Constraint

Direct time-of-flight (dToF) LiDAR obtains range information by emitting narrow laser pulses and measuring the echo flight time. The TX driver injects high-peak, narrow-pulse-width, fast-edge current pulses into the VCSEL at precise instants; the electrical parameters of this stage directly determine the system's detection range and ranging accuracy.

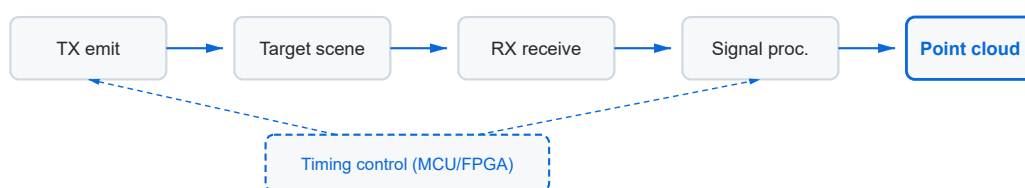


Figure 3-1 LiDAR dToF System Signal Chain

Core Constraint: Loop Inductance $V = L \cdot di/dt$

The core physical constraint of TX-driver design is simple: under fast current change (di/dt), the loop parasitic inductance L produces an inductive voltage drop $V = L \cdot di/dt$, so every nH of inductance directly consumes drive-voltage headroom and lengthens the pulse current rise time.

Two conclusions follow. First, the higher the inductance and the shorter the current rise time (the faster the edge), the higher the required drive voltage. In a typical long-range scenario (about 20 A peak; loop inductance estimated at an optimistic 1 nH level, while real systems are usually higher), pushing the current rise time down to the 1 ns level consumes about 20 V of voltage headroom from loop inductance alone.

Second, current rise time directly determines ranging accuracy. The slower the leading edge, the more the leading-edge discriminator's trigger instant drifts with echo amplitude (time-walk error) — empirically, every additional ~1 ns of current rise time adds about 15 cm of ranging error. Relaxing the current rise time eases the voltage pressure but at the expense of ranging accuracy; the two must be traded off.

3.1 Drive-Voltage Budget

A narrow pulse width improves range resolution and a fast edge improves leading-edge discrimination accuracy; together (high di/dt) they are key to improving LiDAR ranging performance. But high di/dt carries a direct cost — it elevates the voltage drop V_L across the loop parasitic inductance into the dominant term of the voltage budget. The voltage budget below targets exactly such narrow-pulse-width, fast-edge scenarios; if the application can relax the pulse-width and edge requirements, the voltage budget drops accordingly.

Taking a six-junction VCSEL at about 20 A peak as the baseline, summing the voltage terms yields the following:

Table 3-1 Six-Junction VCSEL Drive-Voltage Budget (Narrow Pulse Width / High di/dt, ~20 A Baseline)

Voltage Term	Source	Typical Value
V_f (VCSEL forward voltage)	Six junctions, ~2 V per junction stacked	~12 V
V_L (loop inductance voltage drop)	Inductive drop under narrow pulse width / high di/dt	~20 V
$I \times R + V_{ds(on)}$	PCB trace resistance + MOSFET on-state voltage drop	6–8 V
Design margin	Temperature drift, device variation, aging derating	3–5 V
Total (six junctions)		~41–45 V

Multi-junction VCSELs are evolving from six junctions toward eight (V_f ~16 V) and ten (V_f ~20 V); stacked with higher peak-current demands, the total voltage budget rises above 50–60 V. Adding forward-looking margin for device derating and higher-junction-count VCSELs, a 60–80 V voltage rating becomes the baseline specification for high-performance TX drivers — with 80 V representing the device voltage-rating ceiling reserved for derating and high junction counts.

3.2 Mapping TX Parameters to System Performance

Table 3-2 TX Driver Parameters vs. System Performance Mapping

TX Driver Parameter	System Impact	Typical Magnitude
Peak current	Laser peak optical power → detection range	20 A → 40 A, range improves by about 41% (for diffuse-surface targets, detection range is proportional to the square root of peak current; for point targets it scales as the fourth root, with smaller gain)
Current rise time	Leading-edge discrimination accuracy → time-walk error	Empirical magnitude: 1 ns → ~15 cm; 2 ns → ~30 cm (actual error also depends on echo dynamic range and discrimination method)

TX Driver Parameter	System Impact	Typical Magnitude
Pulse width	Trade-off between single-pulse energy ($\rightarrow$ detection range) and range resolution; narrower is not always better	The theoretical range resolution equals half the distance light travels during the pulse (2 ns $\rightarrow$ 30 cm; 5 ns $\rightarrow$ 75 cm). Short-range, high-accuracy scenarios favor narrow pulse widths. Long-range applications require sufficient energy and commonly use about 5 ns. Actual results vary with the receiver.
Pulse-width jitter	Pulse-to-pulse energy or timing fluctuation $\rightarrow$ random ranging error, magnitude depends on the receiver	Theoretically 100 ps rms $\approx$ 1.5 cm, but in SPAD+TDC systems it is largely masked by time quantization error and has limited impact; it warrants more attention with other receivers and applications
Channel-to-channel skew	Probabilistic stacking of multi-channel timing skew $\rightarrow$ broadened point-cloud depth-noise distribution	Per-channel skews stack statistically and broaden the depth-noise distribution (not a fixed offset); $\sim$ 1 ns of skew corresponds to about 15 cm of depth broadening
Programmable slew rate	Electromagnetic interference (EMI) vs. performance trade-off	20 V/ns $\rightarrow$ 5 V/ns, high-frequency EMI significantly reduced

Note that all entries in the table are system-level performance metrics; the system can, to some extent, mitigate the impact of individual parameters through algorithmic compensation, back-end calibration, and similar means. However, improving the driver's own (analog) performance reduces system-design complexity at its root, lowers calibration effort, and improves consistency in volume production and across temperature extremes.

The $V = L \cdot di/dt$ constraint points to three design directions: high voltage (60–80 V) to support fast current slew rates; low inductance (PCB and package optimization, targeting < 1 nH); and fast switching (nanosecond edges). Meanwhile, as automotive LiDAR evolves toward Flash solid-state solutions, 2-D addressable VCSEL arrays require the TX driver to provide multi-channel parallel capability and per-channel programmable control.

4. Driver Architecture — High-Side Charging + Low-Side Pulsing

Three Architectures for VCSEL Pulse Drive

VCSEL pulse drivers use three architectures: pure high-side drive, pure low-side drive, and high-side charging with low-side pulsing.

Pure high-side drive. A high-side switch supplies the VCSEL pulse current directly.

Pure low-side drive. An energy-storage capacitor connects across the high-voltage bus. A low-side switch pulls the VCSEL cathode to GND and discharges the capacitor.

High-side charging with low-side pulsing. A controlled high-side circuit charges a local capacitor. A low-side switch then discharges the stored energy through the VCSEL.

The two capacitor-based architectures differ in their charging methods. Pure low-side drive charges passively from the bus. High-side charging uses a dedicated IC with controlled charging and integrated diagnostics.

Table 4-1 Comparison of the Three VCSEL Pulse-Drive Architectures

Comparison Dimension	Pure High-Side Drive	Pure Low-Side Drive (TPM8918Q + Energy-Storage Capacitor)	High-Side Charging + Low-Side Pulsing (TPM8909Q + TPM8918Q)
Operating principle	During the pulse, current is supplied in real time by the power source through the high-side switch and fed directly into the VCSEL	The VCSEL anode connects to the high-voltage bus; the energy-storage capacitor sits directly across the bus (a large capacitor suffices, no charging RC needed); a low-side NMOS instantaneously pulls the cathode to GND to fire the discharge; the peak comes from the capacitor	A controlled high-side circuit charges the local capacitor; the low side discharges it through the VCSEL; the peak current comes from the capacitor
Peak-current ceiling	The peak flows through the high-side switch in real time, limited by the switch's current capability, loop inductance, and gate drive; very high peaks are hard to reach	Powered by a large local capacitor; can reach tens to over a hundred amperes	Powered by the local capacitor; can reach tens to over a hundred amperes
Supply requirements	The supply must deliver large currents instantaneously, stressing the Boost and decoupling design	The large capacitor is powered directly from the bus with no charging RC; the supply only provides average power; if an RC is added to limit power, the charging rate is RC-constrained, capping the repetition-rate ceiling	The supply only provides average power (slow charging); transients are handled by the capacitor
Pulse shaping	Current is directly controllable; amplitude, pulse width, and waveform are programmable, enabling precise shaping	Pulse width is set by the low-side on-time and the edges are programmable; amplitude varies with bus/capacitor voltage because no controlled high-side charging is present, so consistency is weaker	Pulse width is set by the low-side switch on-time and the edges are programmable; amplitude droops slightly as the capacitor discharges; turn-off ringing and tails must be suppressed
Residual charge and repetition rate	No stored residual charge; repetition rate is flexible	No active charge management; residual-charge and repetition-rate management is weak (active discharge and diagnostics require external circuits)	Active discharge is needed to clear residual charge; the charge/discharge cadence caps the frame rate
Safety fallback	Turning off the high side stops emission, but the energy source and the switch share the same device, coupling failures	Turning off the low side stops emission, but lacking active discharge and diagnostics, fallback means are limited	Stopping charging cuts off the energy source, decoupled from the low-side pulsing, providing an independent fallback
Switch implementation and cost	Requires a high-side high-power switch: PMOS die area and cost are about 2.5× to 3× those of an equivalent NMOS, making this option unsuitable at high voltage and high current; a high-side NMOS requires complex high-side level shifting, with major reliability challenges at high speed and low latency	Each channel needs one high-voltage, high-current low-side switch plus an energy-storage capacitor; saves the high-side charging IC, but without the marginal-cost amortization of shared charging the cost scales linearly with channel count; overall between pure high-side and high-side + low-side	Fast pulses are handled by a source-grounded low-side NMOS, with no level shifting and simple drive; the high side only handles controlled charging with relaxed speed requirements
BOM and board area	No energy-storage capacitor array needed, lean external circuitry	Low-side pulse IC + energy-storage capacitors (saves the high-side charging IC), moderate board area	Requires an energy-storage capacitor array, increasing BOM and board area

Comparison Dimension	Pure High-Side Drive	Pure Low-Side Drive (TPM8918Q + Energy-Storage Capacitor)	High-Side Charging + Low-Side Pulsing (TPM8909Q + TPM8918Q)
Suitable scenarios	Small-to-medium currents, flexible waveforms, single- or few-channel scanning systems	Common-anode 1-D line-array VCSEL small arrays with few channels and modest charging-rate and diagnostics requirements	High peak currents, Flash and 2-D arrays, multi-channel parallel operation

Pure high-side drive. This architecture places the fast, high-current switch on the high-voltage rail. A PMOS avoids level shifting but increases die area and cost at the same on-resistance. A high-side NMOS improves silicon efficiency but requires fast, reliable gate-level shifting.

Capacitor-based architectures. These architectures move the fast pulse to a source-grounded low-side NMOS. This arrangement simplifies the gate drive and avoids high-side level shifting. A dedicated high-side IC also provides controlled charging and diagnostics.

Pure low-side drive. This architecture omits the charging IC. However, each channel requires a high-voltage switch and an energy-storage capacitor. The architecture also lacks integrated charging control and diagnostics. Its cost scales with channel count and remains between the other two architectures.

Flash and 2-D addressable arrays. These arrays can require tens of amperes within a few nanoseconds. Multiple channels can fire in parallel. Such pulses exceed the transient current capability of the system supply. Local capacitors supply the pulse current and decouple slow charging from fast pulsing. The following sections therefore focus on high-side charging with low-side pulsing.

Application fit. Pure high-side drive suits scanning LiDARs that require flexible waveforms and moderate peak current. Pure low-side drive suits small common-anode 1-D arrays. These arrays typically have few channels and modest charging or diagnostic requirements.

4.1 Architecture Overview and System Composition

Local energy storage isolates the high-current transmit pulse from the system supply.

This section details the multi-channel array implementation — high-side charging (TPM8909Q/AQ) paired with low-side pulsing (TPM8918Q/BQ). The TPM8915Q integrated power stage is the complementary single-channel / Flash-class option; the two are parallel branches of the same portfolio, each matched to a different application class rather than competing topologies.

System Composition

The complete drive chain consists of four functional blocks:

- Boost stage: steps the system voltage (5–36 V) up to a 60–80 V high-voltage DC bus
- High-side multi-channel charging IC (16 channels, 80 V / 1 A constant current): charges row by row via row gating, providing active discharge, charge-voltage diagnostics (CVD), and residual-voltage diagnostics (RVD)
- Energy-storage capacitor array: configured independently per channel on the VCSEL anode side
- Low-side multi-channel pulse driver IC (8 channels, 20 A per channel): turns on the power MOSFET with ~1 ns edges; the energy-storage capacitor discharges through the VCSEL to generate the laser pulse

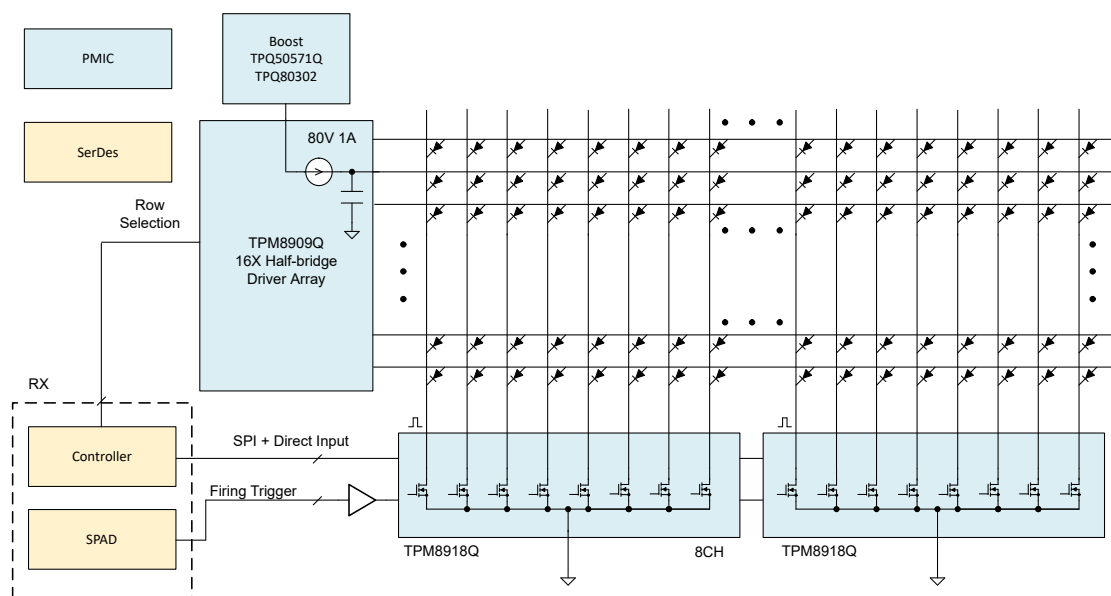


Figure 4-1 2-D Flash LiDAR TX Drive System Architecture

Boost + TPM8909Q high-side charging + TPM8918Q low-side pulsing + VCSEL array

Operating sequence: Boost supplies energy → high-side constant-current charging → charging complete → low side turns on and the capacitor discharges through the VCSEL → turn-off → high-side active discharge clears the residual charge → next charging cycle. The architecture decouples slow charging from fast pulsing: transient high currents come from local capacitors, the charge voltage is adjustable to match VCSELs of different junction counts, and stopping the charging cuts off the energy source.

4.2 Charging Topology Comparison

Table 4-2 Constant-Current Charging vs. Resonant Charging

Comparison Dimension	Constant-Current Charging (TPM8909Q)	Resonant Charging (TPM8909AQ)
Operating principle	Constant-current source charges linearly to the target voltage	LC resonant single-pulse energy transfer with zero-current-switching (ZCS) commutation
Energy-transfer efficiency	The linear current source dissipates $(V_{\text{supply}} - V_{\text{cap}}) \cdot I$ throughout; since charging starts from a low voltage, efficiency is inherently limited (ideal ceiling about 50% at full discharge)	>98% in the resonant stage, about 85–95% including the Boost front end (typical)
Design complexity	Low: mature topology, few external components	Higher: requires matched LC parameters, two-stage power architecture
Suitable scenarios	Multi-channel arrays where electromagnetic compatibility (EMC) and reliability come first	Fast charging of large capacitors, high-frame-rate systems

The constant-current charging solution holds advantages in most Flash LiDAR production systems: deterministic charging timing, excellent EMC performance, simplified external BOM, and on-chip CVD and active-discharge functions that directly serve the eye-safety protection chain.

4.3 Active Discharge of the Energy-Storage Capacitor

After each pulse, the energy-storage capacitor retains residual voltage due to VCSEL V_f clamping, pulse-width limits, and LC ringing recharge. If not cleared, the residual charge causes pulse-to-pulse energy drift, faint unintended emission from unlit channels, and switching-transient crosstalk. TPM8909Q / TPM8909AQ integrate an on-chip low-side discharge path: an anode pull-down device (a low-side device between the VCSEL anode and GND) bleeds the energy-storage capacitor charge to GND (bypassing the VCSEL, so the discharge emits no light), and once the RVD loop confirms discharge completion the next charging cycle starts automatically, with no external discharge circuit required.

Handling unselected channels balances two opposing risks. If the residual charge is retained, when an adjacent channel sharing the same column (cathode) fires and pulls that column's cathode low at tens of V/ns, the charge pre-stored on the unselected VCSEL's anode drives forward current through the forward path, glowing faintly and creating "ghost" false echoes in the point cloud. If instead the anode is held continuously at 0 V, lateral coupling from adjacent charged rows through the shared column keeps that VCSEL repeatedly reverse-biased over the long run — especially harmful to low-junction-count VCSELs, where the reverse voltage concentrates rather than being shared, degrading reliability. The continuously conducting pull-down device also forms a static bleed path between the bus and GND that wastes power.

The TPM8909Q MODE pin controls whether unselected channels enable this anode pull-down device: with MODE=H, unselected channels pull the anode low through the device, clearing the residual charge to suppress ghosting, and the resulting reverse bias is diluted by the multi-junction VCSEL (the total reverse voltage is distributed across the junctions — nominally about V_R/N per junction, though the split is not necessarily equal and tends to concentrate on the weakest junction); when a channel develops a short-circuit fault, switching to MODE=L puts unselected channels into high-impedance tri-state, preventing the device from becoming a sustained leakage-emission path.

Table 4-3 MODE Pin Control of Unselected Channels

MODE	Unselected Channels	Function	Applicable
H (low-side mode)	Pull-down device pulls the anode to GND	Clears residual charge, suppresses residual-charge ghosting	Normal operation (reverse bias diluted by the multi-junction VCSEL)
L (high impedance)	Tri-state Hi-Z	Retains residual charge, avoids reverse bias, forms no leakage path	Preserves eye safety during channel short-circuit faults

4.4 Package Parasitic Inductance Comparison

In low-side pulse drive, when 50 A switches with ~1 ns edges, every 0.1 nH of parasitic inductance produces about 5 V of inductive voltage drop (the steeper the edge, the higher the drop). The integrated power-stage approach monolithically integrates the MOSFET with the drive logic, eliminating inter-die interconnect parasitics.

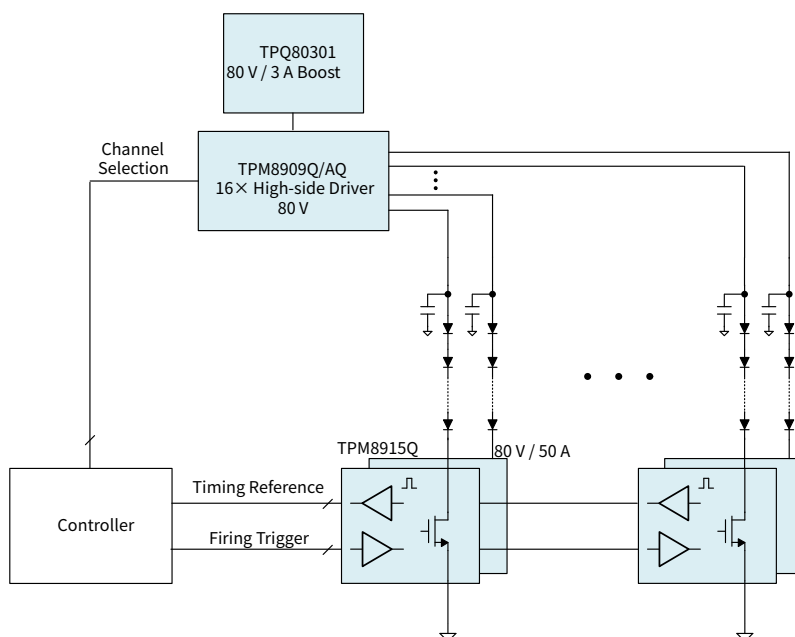


Figure 4-2 TPM8915Q Integrated Power-Stage Drive System

Table 4-4 Package Parasitic Inductance Comparison

Package Type	Typical Parasitic Inductance	Interconnect	Suitable Scenarios
WLCSP	< 0.1 nH	Copper-pillar bumps directly to the PCB, no bond wires	80 V / 50 A / ~1 ns
QFN	0.3–0.8 nH	Leadframe + bond wires	~20 A, cost-sensitive
Discrete GaN + driver IC	0.5–2 nH	Inter-die traces + bond wires	Flexible pairing with GaN of different voltage classes

4.5 Large/Small-Pulse Dual-Pulse Drive

A LiDAR system must cover both short-range (a few meters) and long-range (hundreds of meters) targets, whose demands on the drive pulse conflict with each other:

Table 4-5 Long-Range Large Pulse vs. Short-Range Small Pulse

Parameter	Long-Range Large Pulse	Short-Range Small Pulse
Peak current	30–50 A	2–5 A
Pulse width	5–10 ns	1–2 ns
Injected-charge ratio (current × pulse width)	Baseline (e.g., 30 A × 5 ns = 150 A·ns)	1/50 of baseline (e.g., 3 A × 1 ns = 3 A·ns)

The system alternates large and small pulses within each frame and fuses the two sets of echo data in post-processing. The large pulse covers the SNR needs of long-range echoes; the small pulse avoids the short-range blind zone caused by saturation of the receive-side SPAD array. The large/small-pulse scheme extends the TX-side injected-charge (current × pulse width) coverage to roughly 50:1. This is only a rough proxy for transmit dynamic range and does not equal the optical-energy ratio or the echo SNR.

4.6 The Turn-Off Speed Dilemma: Secondary Light Emission and Reverse Bias

Fast turn-off helps narrow the pulse width and improve time resolution, but faster is not always better. At the turn-off instant, the loop inductance responds to the sharp negative di/dt according to the same $V = L \cdot di/dt$, bringing two classes of risk:

- Secondary light emission: if LC loop ringing at turn-off forward-biases the VCSEL again, an unintended small optical pulse follows the main pulse, appearing as a false echo at the dToF receiver, polluting the ranging histogram and raising short-range noise.
- Overvoltage risk: the negative di/dt excites voltage spikes across the loop inductance, and two voltages warrant attention — first, the absolute voltage spike of the drive node to ground, which directly stresses the driver device's voltage rating; second, the reverse bias superimposed across the VCSEL: VCSEL reverse-voltage tolerance is very low, and excessive reverse bias can damage the device and, in 2-D row-column addressed arrays, trigger reverse leakage and crosstalk in unselected channels. Both must be kept within device ratings.

The two TPM8915Q measured waveforms below confirm these two risks respectively:

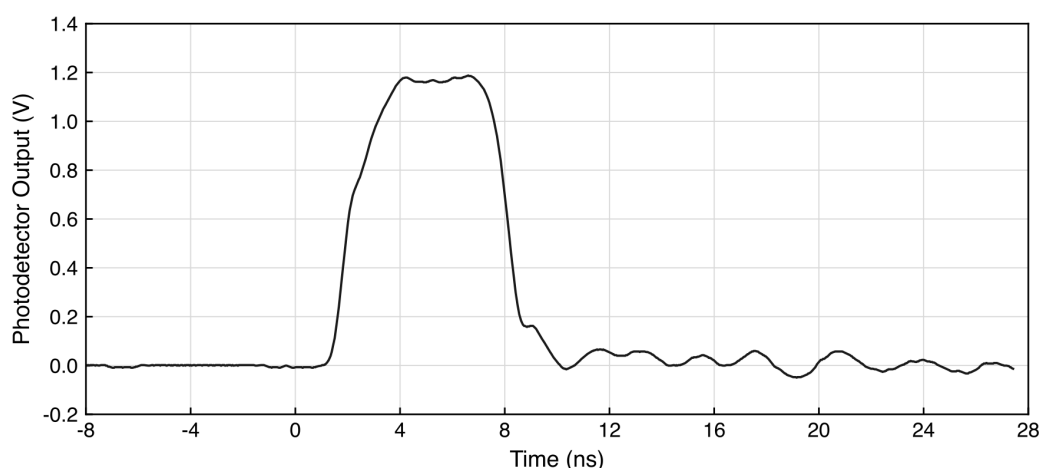


Figure 4-3 TPM8915Q Measured Optical Pulse Waveform

Main pulse width is about 6.1 ns; rise/fall times is about 1.8 ns; secondary light emission caused by ringing is visible after turn-off

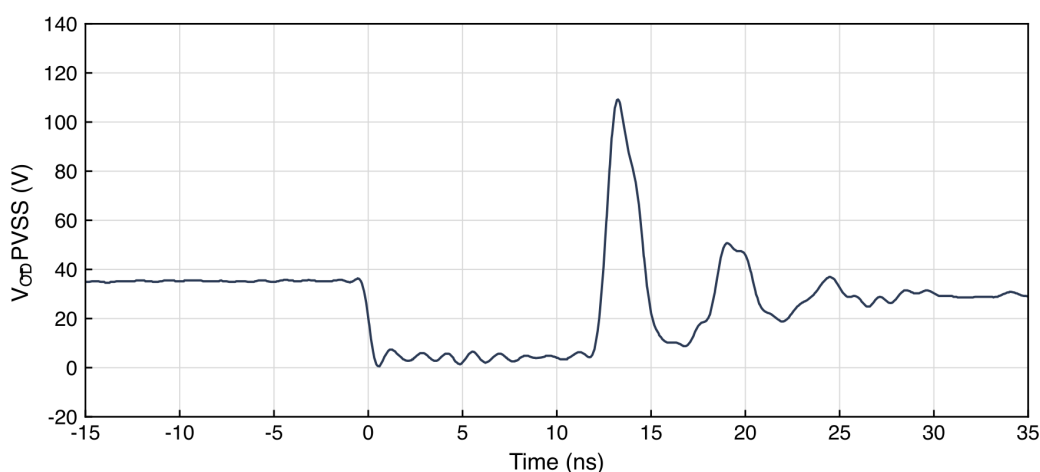


Figure 4-4 TPM8915Q Measured Turn-Off Voltage Overshoot Waveform

Room temperature, $I_D \approx 56.5$ A, loop parasitics about 3 nH; the measured node-to-ground voltage peak at the turn-off instant is about 110 V (the $L \cdot di/dt$ inductive spike plus the bus voltage and ringing) — on the high side, and must be brought below 80 V by reducing the loop parasitic inductance

Engineering practice therefore takes a multi-pronged approach: on one hand, use a programmable slew rate to moderately adjust the switching edge rate while still meeting pulse-width and ranging-accuracy targets, combined with freewheeling and clamping paths to suppress ringing; on the other hand, optimize the loop parasitics and the PCB layout — shorten the high-current loop, reduce parasitic inductance, and arrange the relative positions of the energy-storage capacitors and switches sensibly — to reduce at the source the voltage spikes that di/dt excites across the parasitic inductance, bringing the turn-off overshoot back within device ratings (the 80 V class). Only by combining both can secondary light emission, reverse-bias stress, and EMI be balanced. The figure below shows measured optical pulse waveforms with programmable slew rate — the edge slew rate of the same optical pulse can be configured as needed.

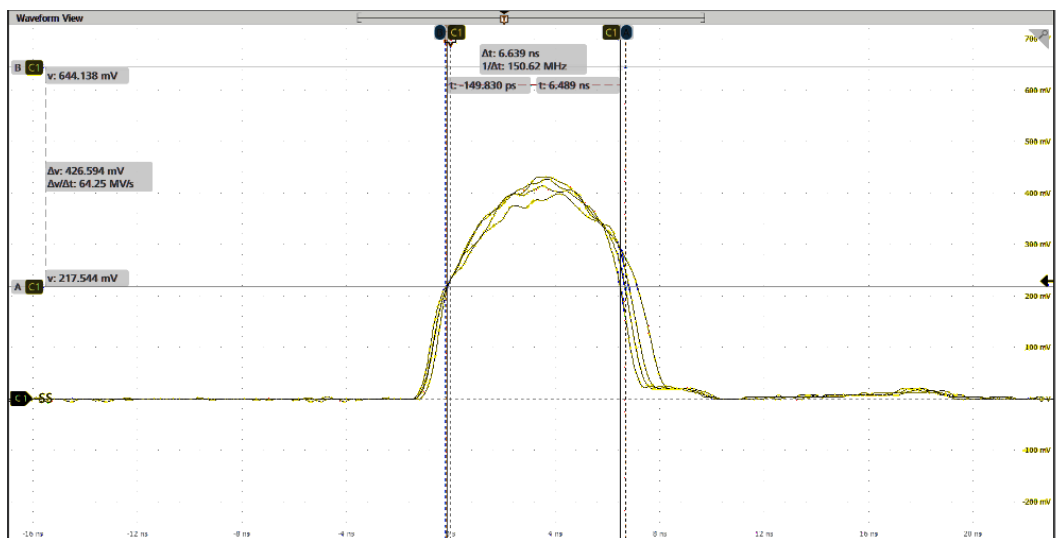


Figure 4-5 Measured Optical Pulse Waveforms With Programmable Slew Rate

Programmable Slew Rate: the optical pulse edge slew rate is programmable

4.7 Timing Reference (TREF) for Laser Emission Timing

Why is a timing reference needed? dToF ranging essentially measures the round-trip time of the optical pulse: $\text{range} = c \cdot (t_{\text{echo}} - t_0)/2$, where c is the speed of light (about 3×10^8 m/s), t_{echo} is the echo arrival instant, and t_0 is the "starting-gun" instant when the laser actually emits light. Once t_0 shifts or jitters, the entire ranging chain carries systematic error and random noise, so the system must obtain a t_0 reference that stays close to the true emission instant and is stable and calibratable.

The traditional approach derives the reference from the power stage itself: the fast edge of the switching node is capacitively coupled (AC-coupled) into an op amp or comparator, and t_0 is established by detecting the slope (the threshold-crossing edge). Its advantage is that no dedicated pin is needed and it senses the power stage's actual switching directly. The drawbacks, however, are clear. The switching node is a high-voltage, high-current, fast-slewing noisy point, and capacitive coupling inherently differentiates the signal, amplifying ringing, overshoot, and other high-frequency noise; the slope-trigger instant therefore drifts with the power-stage edge amplitude and ringing shape, jitters heavily, and triggers falsely with ease. The R and C tolerances of the coupling network and the op amp's offset and temperature drift each add their own error, so the approach undermines the very goal of a stable reference and is hard to calibrate.

The main drive stage has an inherent propagation delay from digital input to VCSEL light emission (TPM8915Q t_{PD_IN} typically about 2.5 ns), and this delay varies with temperature, so the digital trigger edge should not be used directly as t_0 . To this end, TPM8915Q integrates a TREF (Timing Reference) output: this pin is synchronized with the internal drive switch and is a push-pull logic-level output — the TPM8918Q/BQ low-side pulse drivers provide the same push-pull TREF — so it drives the timing reference directly with no external pull-up resistor required; it provides a low-voltage, low-noise timing reference ahead of the power stage's light emission, from which the system establishes t_0 .

TREF delivers value in two ways: it tracks the true emission instant, and its delay is stable and can be calibrated once. Oscilloscope persistence-mode measurements (figure below) show the deviation between TREF and the power-output edge is only about 240 ps with about 35 ps of jitter — TREF tracks the true emission instant closely; the datasheet t_{PD_TREF} and t_{PWD_TREF} are typically about 1 ns and stable over the full temperature range, so the system can calibrate once and compensate long-term for the main driver's inherent delay and temperature drift.

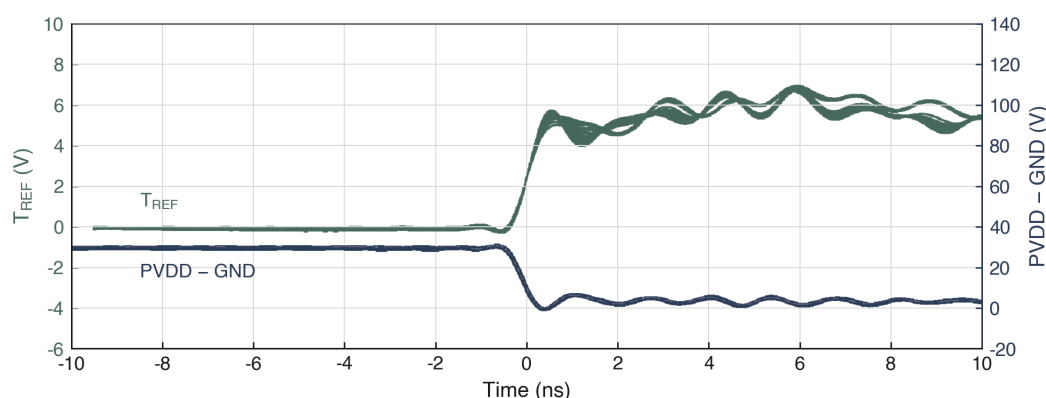


Figure 4-6 TPM8915Q TREF Measured Waveform (Persistence Mode)

Green = TREF, blue = power output; the tightly aligned edges and narrow persistence envelope indicate low jitter (TREF–output deviation about 240 ps, jitter about 35 ps)

4.8 2-D VCSEL Array Drive

The 1-D linear VCSEL array with mechanical scanning suffers three efficiency bottlenecks:

- Low photon time utilization: with a 120° horizontal FoV and 0.2° angular resolution, for example, only one horizontal azimuth (one vertical line) is illuminated at any instant — about 0.17% of the field of view (a geometric duty estimate over 600 horizontal resolution cells); transmit energy is diluted over time, and the corresponding effective echo-collection window is equally low
- Concentrated emitter thermal load: all pulse heat dissipates in the same set of emitters, limiting single-pulse peak power
- Added scanning-optics loss: mechanical scanning optics introduce about 10–15% optical-path efficiency loss plus the reliability risk of moving parts

The 2-D addressable VCSEL array (e.g., 32 rows × 16 columns) resolves these bottlenecks through row-scanned time-division multiplexing: photon energy concentrates on the target zone, per-emitter per-frame thermal load drops with the row count, and the added scanning-optics loss is eliminated.

The 2-D array also gives the TX side an active means of mitigating high-reflectivity blooming: selectively lower the drive current or reduce the number of emitters for known highly reflective regions, combined with alternating large/small-pulse patterns, achieving zone-level power control on the TX side.

Row-column addressing compresses the number of control lines to the order of rows + columns, markedly reducing drive channels and interconnect count and helping lower system BOM cost. The high-side charging IC (TPM8909Q, 16 channels) handles row gating and charges each row's energy-storage capacitors; the low-side pulse IC (TPM8918BQ, 8 channels) handles column drive, with multiple devices cascaded to cover the full array.

Because emission is row-scanned, only one row is active at any instant, so each row update reconfigures just the one row-gating IC that owns the active row plus every column-drive IC — never the whole array. The per-update configuration payload therefore scales as one row IC plus the column ICs, independent of how many row ICs the array uses. For the 32×16 example above — two row ICs (TPM8909Q, 16 channels each) and two column ICs (TPM8918BQ, 8 channels each) — a single row update writes one row IC and both column ICs, i.e. three devices' worth of configuration data rather than all four.

4.9 SPI Communication and Dual-Register-Set Architecture

The 2-D array uses row-scanned time-division multiplexing; each row points to a different azimuth in the field of view, corresponding to different target distances and reflectivities, so the drive parameters must be reconfigured row by row: on one hand, update the channel enables according to the columns actually lit in the current row, turning off channels not participating in emission to avoid wasted light and adjacent-channel crosstalk; on the other hand, adjust the peak current and edge slew rate to the row's targets — lower the current and slow the slew for near, highly reflective zones to curb receiver saturation and EMI, and raise the current and speed up the edges for distant, low-reflectivity zones to preserve echo SNR. This reconfiguration must complete within each row slot, or it becomes the frame-rate bottleneck.

The TPM8918Q and TPM8918BQ are two configurations of the same device; their configuration schemes compare as follows:

Table 4-6 Channel Configuration Scheme Comparison

Dimension	Parallel Configuration (TPM8918Q)	SPI + Dual Register Set (TPM8918BQ)
Configuration interface	CS0–CS7 (channel select) + SR0–SR2 (slew rate) parallel pins	SCLK / SDI / SDO + LATCH + REGSEL
Switchover latency	Direct combinational selection, no configuration latency	Switchover latency hidden by pre-writing (ping-pong; inter-row overhead approaches zero, bounded by REGSEL toggling / register settling time)
Row-by-row parameter update	Limited by the number of parallel-pin combinations	Pre-write the other register set via SPI; writing proceeds in parallel with emission
Multi-device expansion	Independent routing per device	SPI daisy-chain cascading, constant I/O usage

The TPM8918Q (parallel-pin) and TPM8918BQ (SPI) are two configurations of the same low-side pulse driver, not two different devices. TPM8918BQ adopts the SPI + dual-register-set architecture. The ping-pong switching of the dual register set lets SPI configuration and pulse emission execute in parallel: while the current row drives from register set A, SPI pre-writes the next row's configuration into register set B; at row switchover the REGSEL pin toggles and register set B takes effect immediately, eliminating the switchover latency introduced by serial transfer.

Multiple TPM8918BQ devices can be cascaded in an SPI daisy chain; the I/O pin count is independent of the number of cascaded devices (configuration latency grows linearly with device count and must remain shorter than the row slot), suiting row-by-row configuration of large-column-count 2-D arrays. The SPI-less TPM8918Q is configured through the CS0–CS7 channel-select and SR0–SR2 (slew rate) parallel pins — simple routing, suited to scenarios with few configuration combinations.

5. Eye-Safety Protection Essentials

Safety Requirements and Critical Fault Scenarios

The single-pulse energy of a VCSEL array can exceed the IEC 60825-1 Class 1 limit by one to two orders of magnitude (single-pulse energy relative to the maximum permissible exposure, MPE). The standard requires that laser emission never exceed the limit under any single-fault condition, and laser-emission control is typically assigned Automotive Safety Integrity Level (ASIL) B or higher — a target derived from the vehicle-level hazard analysis and risk assessment (HARA) rather than fixed by ISO 26262 itself.

The single-point fault with the most severe consequence is a low-side MOSFET short: the normal duty cycle is below 0.1%, and once shorted, the laser degrades from pulsed to continuous-wave (CW) emission with average power approaching peak power; for the average-power criterion, the factor by which the Class 1 limit is exceeded $\approx 1/\text{duty cycle}$ (a duty cycle $<0.1\%$ means more than a thousandfold).

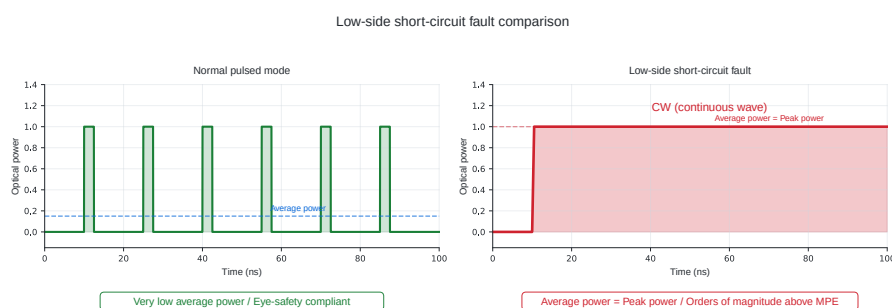


Figure 5-1 Normal Pulsed Mode vs. Low-Side Short-Circuit Fault Mode

5.1 Critical Failure Modes and Hazards

Eye-safety design starts from identifying the failure modes in the TX drive chain that can endanger eye safety, and their hazards:

Table 5-1 Critical TX Driver Failure Modes and Hazards

Failure Mode	Hazard
Low-side switch short	VCSEL cathode permanently grounded; the laser degrades from pulsed to continuous-wave (CW) emission, average power approaches peak, far exceeding eye-safety limits — the most severe consequence
Single-pulse pulse-width runaway	Single-exposure energy exceeds the MPE limit
Driver IC logic or control failure	Output out of control, possibly sustaining laser emission
Charging energy source not cut off	With charge-voltage runaway or total low-side failure, high-voltage energy keeps being injected and the fault cannot self-terminate
Turn-off ringing and reverse bias	Ringing-induced secondary light emission produces false echoes; excessive reverse bias damages the VCSEL (see the previous chapter)
IC and VCSEL module overtemperature	Device damage and thermal runaway, reliability and safety risks

In terms of hazard, the most severe consequence is sustained emission caused by an energy source that cannot be cut off. The dual-chip high-side charging + low-side pulsing architecture holds a structural advantage here: even if the low-side IC fails completely, the high side can still stop charging and actively discharge; once

the energy in the energy-storage capacitor is exhausted, the laser naturally stops — providing an independent fallback for the energy source.

6. Selection Guide and Product List

Selection Decisions

Flash solid-state multi-channel → high-side + low-side solution

The high-side charging ICs (TPM8909Q / TPM8909AQ) provide 16 channels of 80 V independent energy storage with CVD/RVD diagnostics. The low-side pulse ICs (TPM8918Q / TPM8918BQ) provide 8 channels of 20 A nanosecond-class synchronized pulses. The two cascade to cover 2-D VCSEL array drive requirements.

Scanning / MEMS → GaN driver solution

External third-party GaN FETs paired with low-side gate driver ICs — single-channel (automotive-grade TPM1025Q / industrial-grade TPM1025, plus the WLCSP-packaged TPM1020) and dual-channel (automotive-grade TPM2025Q / industrial-grade TPM2025) — suited to single- or few-channel EEL and 1-D VCSEL systems.

Single-channel high performance → integrated power stage

TPM8915Q integrates an 80 V / 50 A power stage in a WLCSP 3.35×1.65 mm package, with package parasitics < 0.1 nH and a 1 ns minimum pulse width.

6.1 Full-Portfolio Product Comparison

Table 6-1 LiDAR TX Driver Full-Portfolio Comparison

Part Number (Automotive / Industrial)	Function	Channels	Max Voltage	Peak Current	Package
TPM8909Q / TPM8909	High-side charging, constant-current	16 ch	80 V	1 A (charging)	QFN5×5-32
TPM8909AQ / TPM8909A	High-side charging, resonant	16 ch	80 V	1.6 A (charging)	QFN5×5-32
TPM8918Q / TPM8918	Low-side pulsing, multi-channel	8 ch	80 V	20 A/ch	QFN5×5-32
TPM8918BQ / TPM8918B	Low-side pulsing, multi-channel + SPI	8 ch	80 V	20 A/ch	QFN5×5-32
TPM8915Q / TPM8915	Integrated power stage	1 ch	80 V	50 A	WLCSP 3.35×1.65 mm
TPM1020	GaN gate driver, single-channel	1 ch	—	7 A (drive)	WLCSP 6-bump
TPM1025Q / TPM1025	GaN gate driver, single-channel	1 ch	—	7 A (drive)	DFN2×2-6
TPM2025Q / TPM2025	GaN gate driver, dual-channel	2 ch	—	7 A (drive)	QFN2×2-10

6.2 Technology Trends

Low cost is the decisive threshold for automotive LiDAR to move from a premium option to a high-volume standard feature, and one of the most important forces driving TX driver evolution: integrated power stages and semi-integrated multi-channel solutions compress the discrete BOM from more than 50 components down to 20–30, reducing component count, shrinking board area, and simplifying assembly and test — delivering sustained system-level cost reduction; industrial-grade versions further address cost-sensitive non-automotive markets.

Multi-junction VCSELs are evolving toward higher junction counts with correspondingly higher forward voltages, pushing driver ICs toward higher voltage ratings; system integration is also migrating from discrete toward semi-integrated and integrated solutions to compress BOM and board area. For 2-D VCSEL arrays, the direction for next-generation high-side charging ICs is more channels and higher charging current, with SPI replacing the parallel interface and support for multi-channel parallel charging.

6.3 3PEAK LiDAR System-Level Solution

At the system level, 3PEAK's device portfolio covers the complete automotive LiDAR signal chain — TX drive (VCSEL Driver / GaN Driver / Low-side Driver / Logic / temperature sensing), RX front end (TIA), interfaces (CAN / SerDes / Ethernet / RS232/485), system monitoring (voltage references / voltage supervisors / amplifiers / comparators), and the complete power chain (reverse protection, Boost, negative rail, PMIC, HV/LV BUCK, LV LDO). The blue blocks in the figure below are devices 3PEAK can supply.

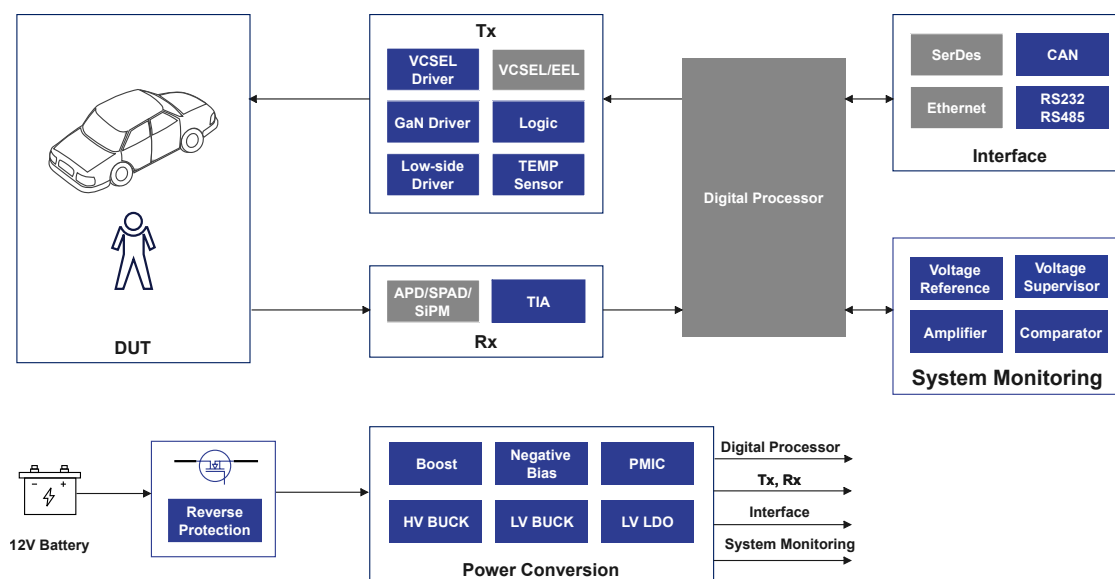


Figure 6-1 3PEAK Automotive LiDAR System-Level Chip Solution Block Diagram

7. Conclusion

The TX driver is the gating component for automotive LiDAR performance, eye-safety, and cost. Three points summarize the analysis above:

- **Physics sets the budget.** Because $V_{\text{drive}} = V_{\text{VCSEL}} + L \cdot di/dt$, every nanohenry of loop inductance and every ampere of di/dt adds to the required rail voltage; a 60–80 V rating, minimized package parasitics, and a fast edge together define the design envelope.
- **Each application class has its own architecture needs.** There is no single winning topology: Flash solid-state, scanning, and 2-D array systems place different demands on channel count, charging method,

turn-off speed, and integration. High-side charging + low-side pulsing is one well-matched answer for multi-channel systems, while an integrated power stage best fits single-channel and Flash-class drive.

- **Integration supports the cost roadmap.** Moving from a discrete TX of more than 50 components toward 20–30-component semi-integrated and integrated solutions is what makes LiDAR affordable at volume.

3PEAK's portfolio spans these needs — high-side charging (TPM8909Q/AQ), low-side pulsing (TPM8918Q/BQ), an integrated power stage (TPM8915Q), and GaN gate drivers (TPM102x/TPM202x) — letting designers match the architecture to each application rather than force-fit a single topology.

8. References and Resources

Standards

- IEC 60825-1, Safety of laser products – Part 1: Equipment classification and requirements
- ISO 26262, Road vehicles – Functional safety

Technical Literature

- D. Liang, C. Zhang, P. Zhang, et al. Evolution of laser technology for automotive LiDAR, an industrial viewpoint. Nature Communications, 2024, 15: 7660. DOI: 10.1038/s41467-024-51975-6
- D. Wang, C. Watkins, H. Xie. MEMS Mirrors for LiDAR: A Review. Micromachines, 2020, 11(5): 456. DOI: 10.3390/mi11050456
- Lumentum. High-Performance Addressable Multi-Junction VCSEL Arrays. lumentum.com

3PEAK Products and Solutions

- 3PEAK automotive LiDAR solutions
- TPM102x GaN gate drivers (TPM1020 / TPM1025 / TPM1025Q)
- TPM2025 / TPM2025Q dual-channel GaN gate drivers
- TPM8909Q / TPM8909AQ high-side multi-channel charging ICs
- TPM8915Q / TPM8915 integrated power stage
- TPM8918Q / TPM8918BQ low-side multi-channel pulse drivers

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