DDR Termination Regulator TPL 51200 Application Notes

In the memory application circuit, for data transmission with fewer Bit lines, the traditional passive bus termination resistor (Thevenin termination) is used to match the DDR transmission line impedance with the power supply impedance, which can effectively reduce the cost (as shown in Figure 1).

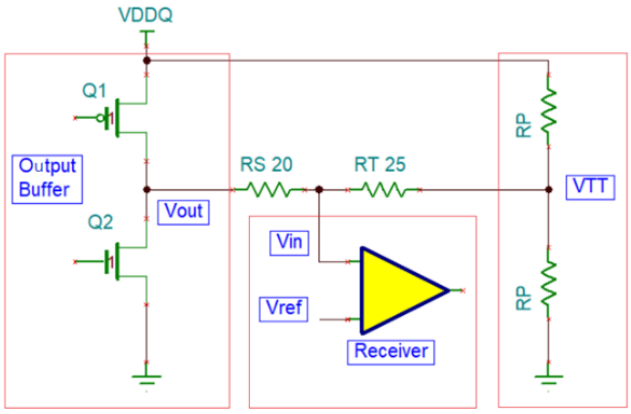


Figure 1. Source Bus Terminal Wiring Diagram

When Q1 is turned on, Q2 is turned off, and the current flows from VDDQ to VTT through resistors RS and RT. At this time, the VTT terminal sinks current, the receiver input voltage (Vin) is higher than Vref, and the receiver realizes the digital signal "1" input;

When Q2 is turned on, Q1 is turned off, the current flows from VTT to ground through RT and RS through Q2. At this time, the VTT terminal sources current, and Vin is lower than Vref, and the receiver realizes the digital signal "0" input.

1.

To obtain faster data transmission rate and ensure stable data transmission, more and more industrial, automotive, communication, and portable electronic systems use DDR memory for data transmission.

In DDR memory, multiple Bit lines share a VTT voltage. To ensure the accuracy of DDR data read and write at the receiving end, Vin must be greater than or less than the voltage Vref of 125 mV to ensure the correct flipping of the comparator.

Taking DDR4 as an example, suppose there are 50 Bit lines in total. At this time, the traditional passive terminal resistor must consider the power consumption issue, especially when the high-bit line and the low-bit line are asymmetrical, and the RP resistance has to be reduced.

Generally, the on-state impedance of Q1 and Q2 is dozens of ohms (take 20 Ω as an example). In DDR4, when the high bits are more than the low bits, VTT absorbs the current. To ensure the accuracy of data read

and write, the calculation formula is:

$$(VDDQ - VTT) \times \left[\frac{RT}{RQ1 + RS + RT}\right] + VTT = (1.2 - 0.6) \times \frac{25}{65} + 0.6 \geq 0.725$$

It can be calculated that the VTT voltage cannot be less than 0.428 V.

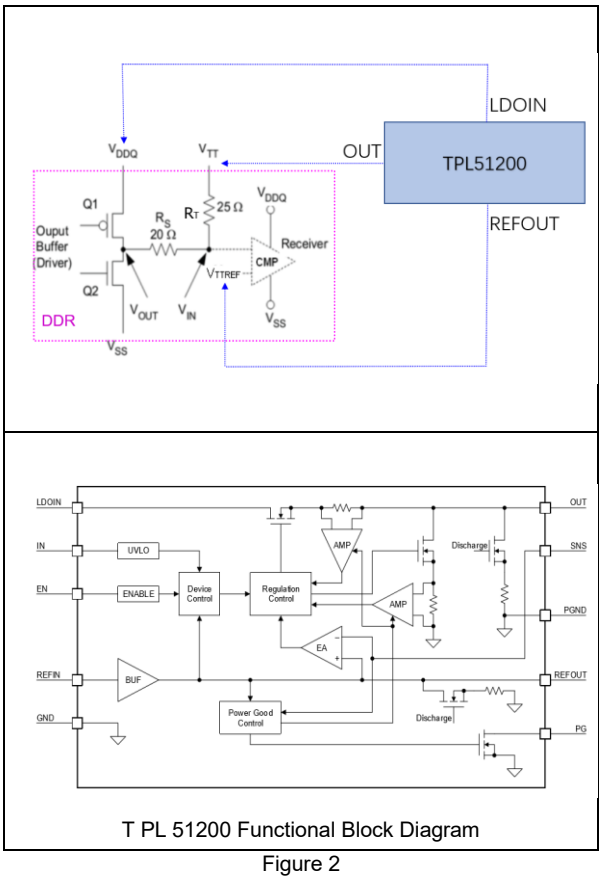
Taking DDR4 as an example, when all the bits are low, to ensure the VTT voltage, the RP resistance cannot exceed 1Ω, which will bring a power consumption of 0.92 W. The calculation formula is:

$$\frac{VDDQ2}{RP + RP//\frac{RT + RS + RQ2}{50}} = \frac{1.22}{1 + \frac{\frac{65}{50}}{1 + \frac{65}{50}}}$$

The RP resistance brings an additional 0.78 W of power consumption, which is unacceptable.

2.

Compared with passive termination, the advantage of active termination (as shown in Figure 2) is that it can provide a stable VTT voltage with high current output capability. This can avoid data read and write errors caused by impedance matching issues at the source, and greatly improve system efficiency by eliminating the Rp voltage divider.



T PL 51200 Functional Block Diagram

Figure 2

As shown in Figure 1 and Figure 2, VTT is an active terminal with both sink and source capabilities. Its working mode is the same as that of passive termination, but in the case of sink or source current, the active termination automatically adjusts the VTT voltage through an internal loop to ensure that the VTT voltage is always equal to 1/2*VDDQ.

The TPL51200 designed by 3PEAK is a high-performance linear regulator suitable for DDR memory bus terminal power supply.

Compared with other DCDC solutions, the TPL51200 reduces the number of components, saving board space and system

cost. It requires less MLCC capacitance and has good load regulation over the full temperature range (-40 ºC to +85 ºC), as shown in Figure 3.

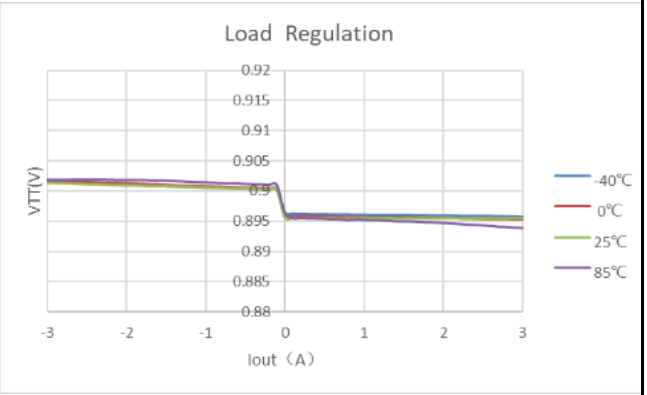


Figure 3

At the same time, the TPL51200 also has a good transient adjustment capability, as shown in Figure 4.

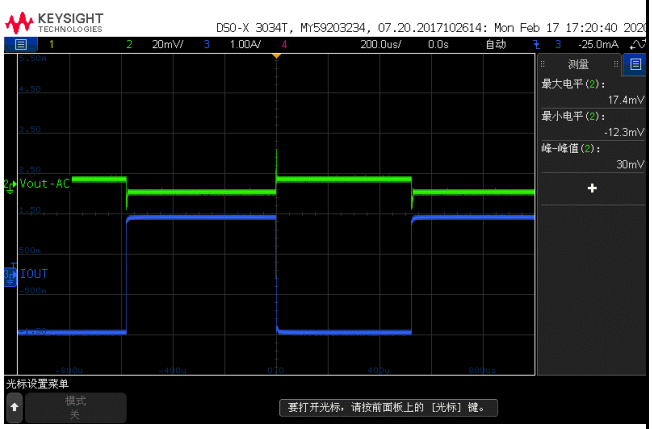


Figure 4

The TPL51200 has built-in functions such as soft start (as shown in Figure 5), short-circuit protection (as shown in Figure 6), over-current protection, and over-temperature protection, and other functions. It can also monitor the PGOOD pin to help confirm the establishment of VTT and ensure the accuracy of data read and write.

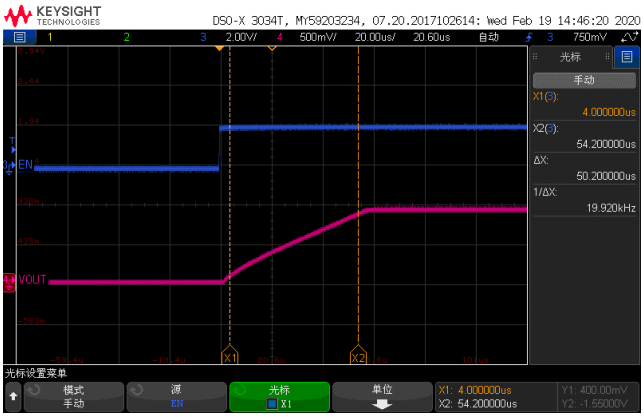


Figure 5

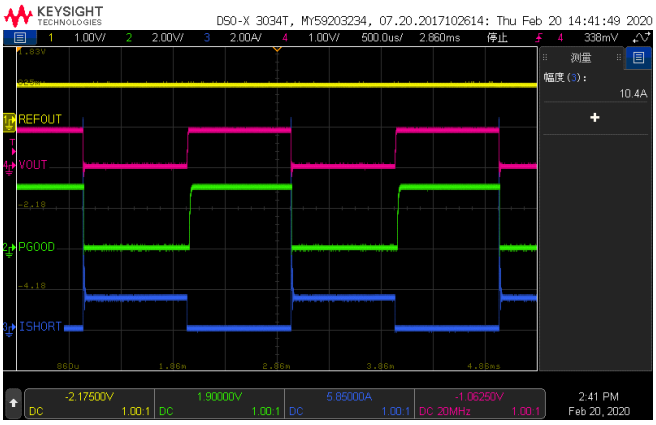


Figure 6

The DDR terminal power supply regulator TPL51200 can meet the power requirements of all VTT bus terminals such as DDR, DDR2, DDR3, DDR3L, DDR4, and LPDDR4, etc.