An Ultra-low Temperature Coefficient Application Circuit of the TPR70ULTC

ABSTRACT

With the continuous advancement of testing and measurement technology, the demand for high-performance power supply voltage references in the instrument and meter industry is increasing rapidly. Specifically, voltage references with low temperature drift are essential for precision applications. This paper introduces a novel circuit architecture designed to precisely control the surface temperature of voltage reference chips, achieving exceptionally low temperature drift.

The underlying principles of the TPR70ULTC's ultra-low temperature coefficient are analyzed, and the corresponding test results are presented to validate its performance.

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1. TPR70ULTC Introduction

1.1 Description

The TPR70ULTC is an ultra-low temperature drift voltage reference module that can operate within an environment temperature range of -40°C to 80°C while maintaining precise control of the chip surface temperature to achieve its ultra-low temperature coefficient performance.

1.2 Typical Application Circuit

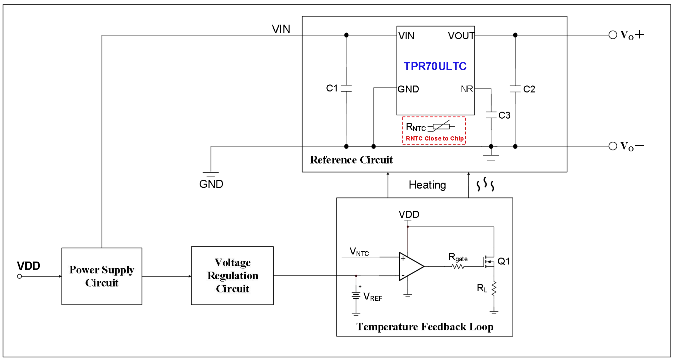

Figure 1-1 Closed-Loop Temperature Control Circuit

Voltage reference chips are sensitive to temperature. To further optimize its drift characteristics, this circuit utilizes a power BJT to heat the PCB, creating a "constant-temperature environment" for the reference chip and thereby achieving ultra-low drift performance.

1.3 TPR70ULTC Application Configuration

The TPR70ULTC supports operating with 9V to 16V and operating in the ambient temperature range from -40°C to 80°C. The temperature of the TPR70ULTC can be set to achieve a temperature drift target of 0.2 ppm/°C (With 80°C setting temperature in this experiment).

Table 1-1 TPR70ULTC Application Configuration

Part Number	Supply Voltage (V)	Setting Temperature (℃)	TC Target (ppm)	Ambient Temperature (℃)
TPR70ULTC	9~16	80	0.2	-40~80

2. TPR70ULTC Circuit Test Setup

2.1 Test Set Up

The main components of the test control system include the TPR70ULTC control board, heating board, power supply equipment, monitoring instruments, and oven, as shown in Figure 2-1. Figures 2-2 and 2-3 present the layout of the TPR70ULTC control board and heating board, respectively. Figure 2-4 shows the PCB hardware of the TPR70ULTC Circuit.

Figure 2-1 TPR70ULTC Temperature Coefficient Test Environment

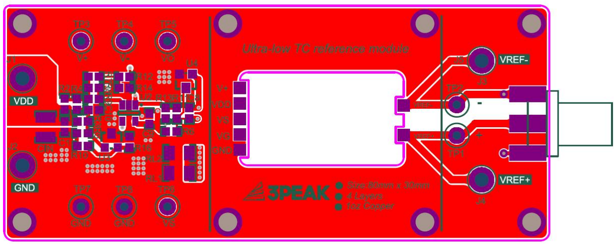

Figure 2-2 Layout of the TPR70ULTC Control Board

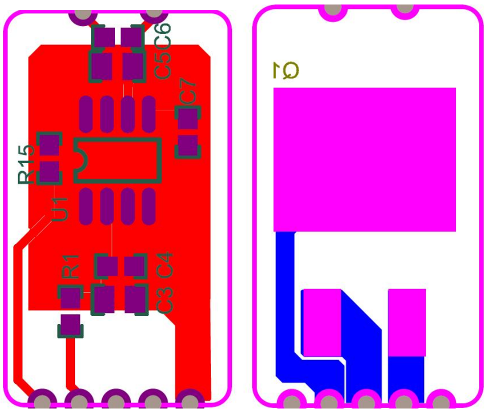

Figure 2-3 Layout of the TPR70ULTC Heating Board

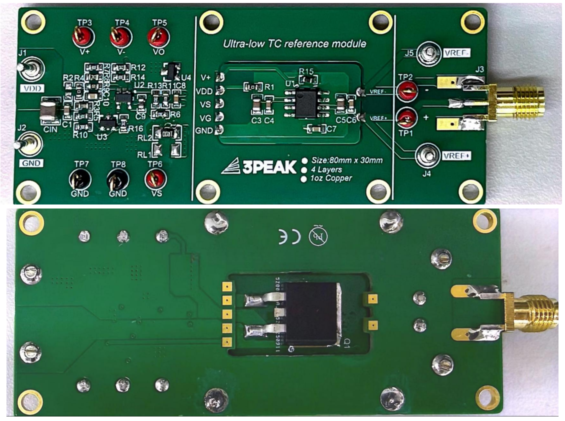

Figure 2-4 Hardware of TPR70ULTC

3. TPR70ULTC Specifications

3.1 Temperature Coefficient

Temperature Coefficient is defined as the variation in output voltage under different operating temperature conditions which has units of parts-per-million per degree Celsius (ppm/°C). The temperature coefficient is typically calculated by using the difference between the maximum and minimum values of the reference voltage (V_{REF}) over the entire operating temperature range.

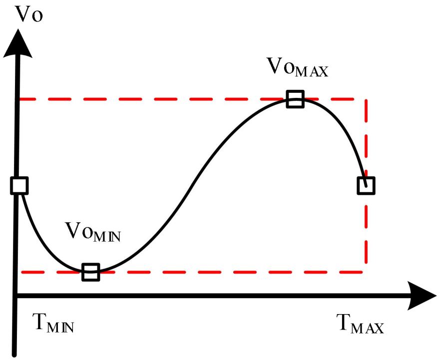

Figure 3-1 V_{REF} Variation in Different Temperatures

The equation for calculating the temperature coefficient is as **Equation 1:**

$$TC = \left(\frac{VOUT_{MAX} - VOUT_{MIN}}{VOUT_{TYP} \times \text{Temprature Range}}\right) \times 10^{6}\,(ppm) \qquad (1)$$

The TPR70ULTC exhibits a low temperature coefficient of 0.2 ppm/°C over the temperature range from –40°C to +80°C.

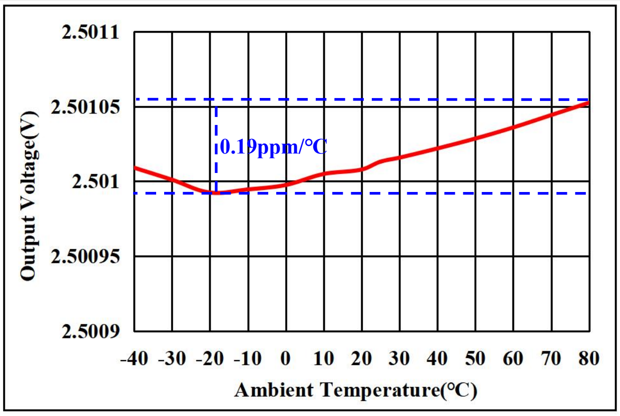

Figure 3-2 Output Voltage VS Ambient Temperature

3.2 Thermal Hysteresis

Thermal Hysteresis is defined as the shift in output voltage after the device undergoes one or more thermal excursions and is specified in parts-per-million(ppm). A thermal excursion is defined as a complete process from room temperature to a minimum temperature, then rising to a maximum temperature and finally back to room temperature (25°C to -40°C to 80°C and return to 25°C). Typically, a wider range of thermal excursion leads to a greater shift in the V_{REF}. The Thermal Hysteresis calculation equation is shown in **Equation 2:**

$$HYST = \left(\frac{VOUT_{T1} - VOUT_{T2}}{VOUT_{TYP}}\right) \times 10^{6}\,(ppm) \qquad (2)$$

where:

HYST is the thermal hysteresis.

$VOUT_{T1}$ is defined as the output voltage measured at +25°C before the device undergoes a temperature excursion from -40°C to +80°C.

$VOUT_{T2}$ is defined as the output voltage measured at +25°C after the device undergoes a temperature excursion from -40°C to +80°C.

$VOUT_{TYP}$ is the output voltage which is specified.

In the TPR70ULTC thermal hysteresis test, the device is first cooled to -40°C, then heated to +80°C, and finally returned to +25°C. The output voltage shift may be either positive or negative. Generally, the stress stabilizes to a minimum after two or more thermal cycles. For the TPR70ULTC, the output voltage stabilizes as early as the second cycle, as illustrated in Figure 3-4.

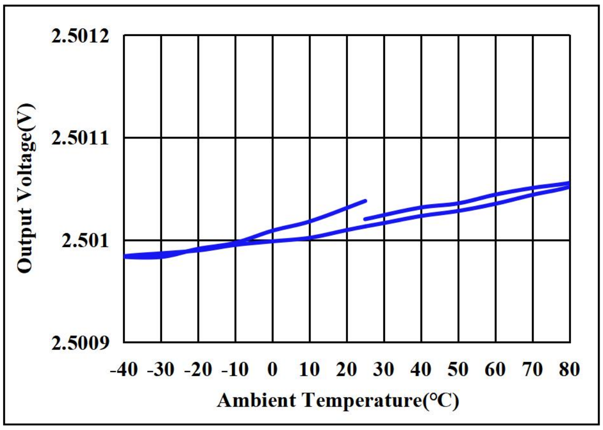

Figure 3-3 Thermal Hysteresis VS Temperature (25℃ to -40℃ to 80℃ and return to 25℃, first cycle)

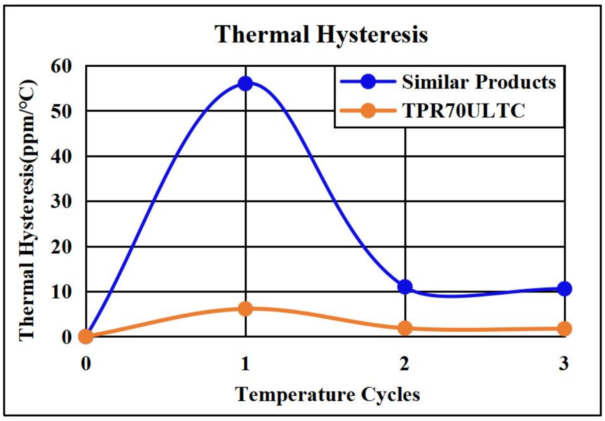

Figure 3-4 Thermal Hysteresis VS Temperature Cycling

3.3 Output Noise

0.1-10Hz noise. Low-frequency V_{REF} noise is specified over the 0.1-10Hz bandwidth as a peak-to-peak value (in µV or ppm). The 0.1-10Hz noise is mainly due to the flicker (1/f) noise of the devices and resistors in the bandgap cell, and therefore its amplitude is linearly associated with V_{REF}. 0.1-10Hz noise of TPR70ULTC is illustrated in Figure 3-5.

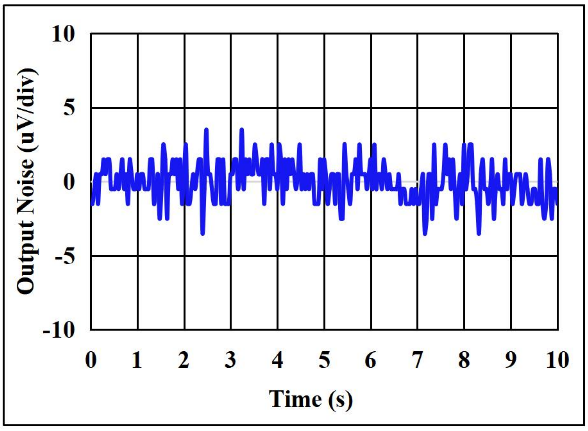

Figure 3-5 0.1-10Hz Voltage Noise

In most cases, this is solved by adding an RC filter to the bandgap output so that a little of the noise is conducted into the gain stage.

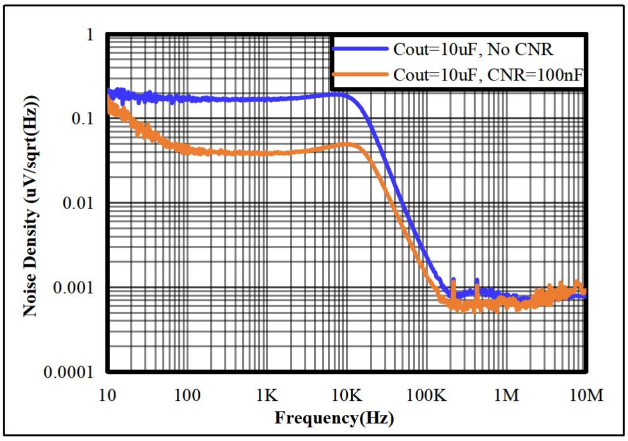

Figure 3-6 Noise Performance Affected by RC Filter

Broadband noise is typically specified as an RMS value in micro-volts over the 10 Hz to 10 kHz bandwidth. TPR70ULTC of the two types of noise, broadband noise is less troublesome as it can be mitigated by using a large bypass capacitor on the VOUT pin.

Broadband noise of TPR70ULTC is illustrated in Figure 3-7.

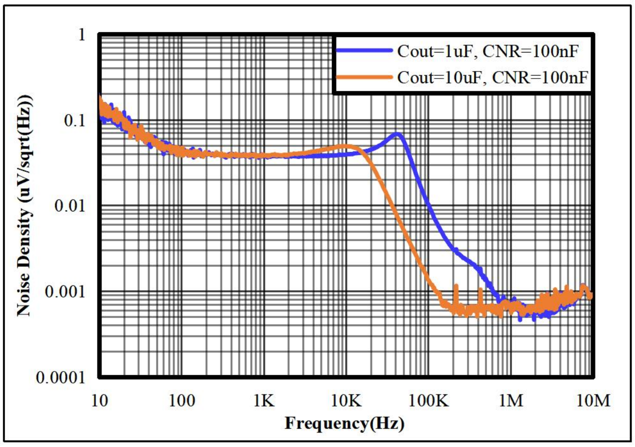

Figure 3-7 Noise Performance Affected by Output Capacitor

3.4 TPR70ULTC Test Waveform

The operational waveforms of the TPL70ULTC system are illustrated in Figures 3-8 and 3-9. Figure 3-10 shows the surface temperature of TPR70ULTC. During the startup phase, the input current of the system is effectively limited to below 300 mA, reducing the inrush current on the system. In steady-state operation, the heating current keeps stable and the temperature of the TPR70ULTC can be precisely controlled around 80°C.

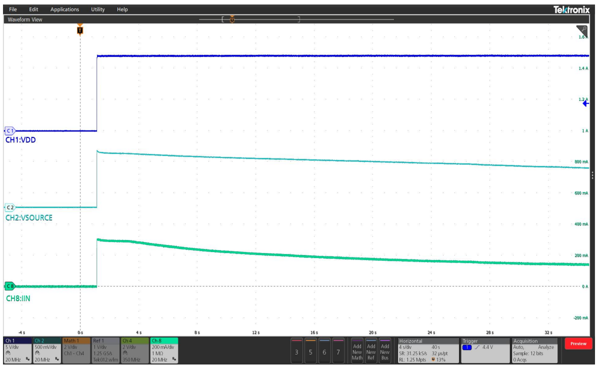

Figure 3-8 Startup Waveform

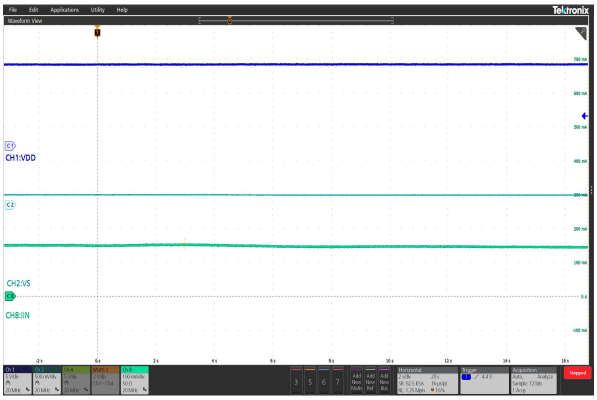

Figure 3-9 Stabilized Operating Waveform

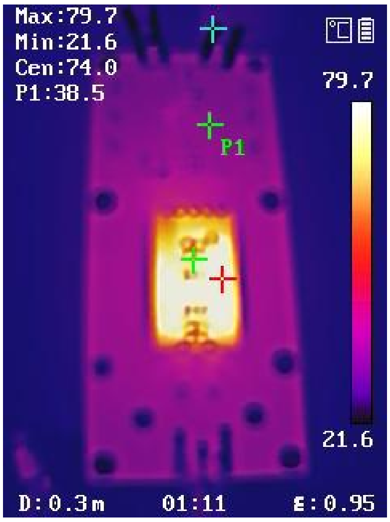

Figure 3-10 Stabilized Operating Temperature

4. Results and Conclusion

This paper presents a temperature coefficient-optimized design based on the TPR70ULTC circuit architecture. This design achieves an extremely low temperature drift of approximately 0.2 ppm/°C while simultaneously maintaining excellent overall performance. We can also offer a higher-performance solution with a coefficient of 0.1 ppm/°C. For further support, please contact the relevant 3PEAK sales representative or email us directly.

5. References

- TPR70 Low-Noise, Low-Drift, Precision Voltage Reference Data Sheet