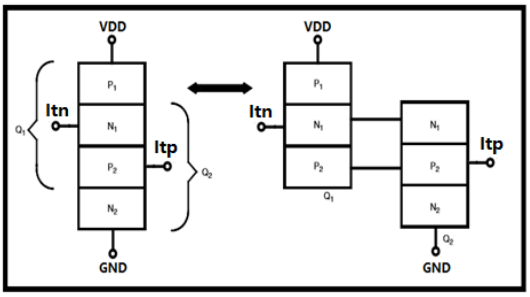
Introduction to Latch-up and the Preventive Measures

The SCR structure (PNPN structure) is one of the inherent structures of the CMOS process. Due to the built-in positive feedback mechanism, once triggered, it is easy to cause the so-called latch-up effect. Once latch-up occurs, it can easily lead to chip burning. Since the SCR structure is a parasitic device structure, there is usually no SPICE model to support its simulation verification. Circuit designers often find latch-up difficult to understand, like a ghost that occasionally comes out to make trouble, making it difficult to prevent and causing headaches. Therefore, latch-up often causes panic among chip design engineers and even system design engineers. They are often overly sensitive to latch-up.

This article attempts to provide a detailed understanding of the SCR structure and the mechanism of latch-up, to uncover its mysterious veil. Then, it provides solutions for preventing latch-up at the chip and system levels. This will enable chip design engineers and system design engineers to have a clear understanding of latch-up. Thus, they will take corresponding measures in the circuit and layout design process to improve the ability of chips and systems to resist latch-up.

1. Latch-up Principle

The SCR structure, that is, the PNPN four-layer device structure. As shown in Figure 1, the SCR structure consists of two bipolar devices (Q1: PNP, Q2: NPN). The base of the PNP is also the collector of the NPN, and the collector of the PNP is also the base of the NPN. If a trigger current Itn flows into the base of Q2 and causes Q2 to enter the amplification working area, the collector current of Q2, which is also the base current of Q1, will be further amplified by Q1. The amplified current flows into the base of Q2 and is further amplified, thus forming a continuously amplifying forward loop. Similarly, if a trigger current Itp flows from the base of Q1 and causes Q1 to work in the amplification area, the collector current of Q1, which is also the base current of Q2, will be further amplified by Q2. The amplified current flows into the base of Q1 and is further amplified, forming a forward loop, resulting in the so-called latch-up. Once the latch-up occurs, even if the trigger current Itn or Itp is removed, the latch-up will continue until the chip burns out.



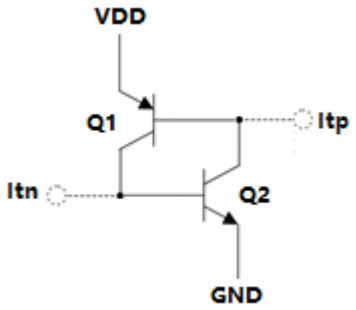


Figure 1. Four-Layer PNPN (SCR) Structure and Its Equivalent Circuit Diagram

In addition that the base current Itn and Itp may trigger the parasitic SCR structure of CMOS to cause latch-up. Rapid changes in power supply (VDD) or ground (GND) can also trigger latch-up, which is commonly referred to as the "dv/dt" effect. In Figure 1, the N1-P2 junction is in the reverse-bias state, but the rapid change of the reverse-bias voltage can cause a junction current. The value of the junction current is shown in the below equation.

$$\frac{\mathrm{d}(C_j V)}{\mathrm{dt}} = C_j \frac{dV}{\mathrm{dt}} + V \frac{dC_j}{\mathrm{dt}}$$

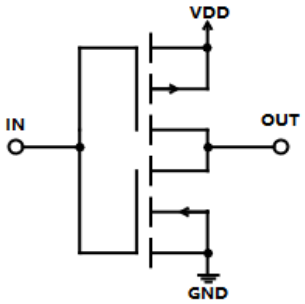
In the above equation, Cj is the junction capacitance of N1-P2. If the slew rate of the reverse-bias voltage across the junction is fast enough, the first term on the right side of the equation will dominate and the current flowing through the junction will increase. When the current flowing through the junction is large enough, a latch-up will be triggered.

We have discussed the current-triggered mode of latch-up. In addition to the current, exceeding the breakdown voltage of the SCR structure can also trigger latch-up. As the voltage at both ends of the SCR structure (VDD-GND) increases, the collector-emitter leakage current of the two bipolar transistors Q1 and Q2 in the SCR structure also increases. When the leakage current becomes large enough, the SCR structure enters latch-up. It is worth noting that both continuous and transient overvoltage pulses can trigger latch-up.

In addition, regardless of the current-triggered mode or overvoltage-triggered mode, the rise in temperature will increase the leakage current flowing through the SCR, making it easier for the SCR structure to be triggered into latch-up.

2. SCR Structure of CMOS and its Latch-Up Trigger Mode

The CMOS output circuit connection and its parasitic SCR structure are shown in Figure 2. The Source and Bulk of the PMOS are connected to the power supply VDD. The Source and Bulk of the NMOS are connected to the ground GND. The Drain of the PMOS and NMOS are connected as the output terminals and the Gate is connected as the input terminal.



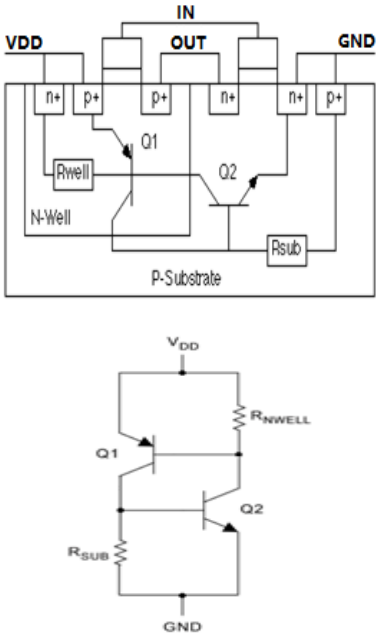


Figure 2. CMOS Output Circuit and Its Parasitic SCR Structure

Usually, exceeding the power supply or ground voltage is the most common latch-up triggering mode in the CMOS output structure. Assume that Vlatch and Ilatch are used to respectively represent the voltage and current conditions that trigger latch-up. Ilatch stands for the minimum current flowing through the output circuit that triggers latch-up, and Vlatch indicates the minimum voltage that triggers latch-up by exceeding the power supply or ground. Vlatch also indicates the voltage when the current flows through the output circuit to reach Ilatch and exceeds the power supply or ground. If the output voltage is lower than the ground (GND) and reaches or exceeds Vlatch, it will cause the base-emitter of the parasitic NPN (Nwell-Psub-Ndrain) to conduct forwardly, thereby triggering the SCR structure in Figure 2 to enter latch-up. Similarly, if the output voltage is higher than the power supply (VDD) and reaches or exceeds vlatch, it will cause the emitter-base forward conduction of the parasitic PNP (Pdrain-Nwell-Psub) to trigger the SCR structure in Figure 2 to enter the latch-up.

It is worth mentioning that there are usually voltage and current limits of 0.3 V and 10 mA for the input and output pins in the product datasheet. Among them, the values of 0.3 V and 10 mA are used for mass production testing and are written into the datasheet. In actual use, the voltage (Vlatch) required to trigger latch-up typically exceeds the power supply or ground by 0.6 V to 2 V, and the current (Ilatch) required to trigger latch-up ranges from 50 mA to several hundred mA.

The above discussion is all about situations where the output voltage is higher than the power supply voltage or lower than the ground voltage. Those situations can cause the base-emitter of the parasitic bipolar to be positively biased, thus triggering the latch-up. There are two other situations that may not occur frequently but also deserve attention. One situation is that if the power supply voltage (VDD-GND) of the output circuit itself is too high, such as exceeding the absolute maximum rating voltage, it may cause avalanche breakdown and trigger latch-up. Another situation is that if there is a very fast peak pulse in the power supply voltage, as mentioned earlier, the "dV/dt" may trigger the SCR structure to enter latch-up.

3. Solution to Chip-Level Latch-up

As mentioned earlier, current flowing through the SCR structure may trigger latch-up, so the device-level or chip-level method to suppress latch-up is to let the holes from P1 and electrons from N2 in the SCR structure (see the P1N1P2N2 structure in Figure 1) be recombined in the N1 (PNP base region) and P2 (NPN base region) regions as much as possible, reducing the current from P1 to N2. Just remember that electrons and holes are actually very simple. They go wherever it is easy to go, just like they originally want to see their friends, but halfway through they see a beautiful woman greeting them, so they naturally run over to her. The solution to chip-level latch-up is either to prevent (increase the distance between N+, P+, STI, SOI) electrons or holes from going to see the beauty or to find a more beautiful woman (guard ring) to attract them. In short, do not let them reach P1 or N2.

1. Increase the distance between P1 and N2, which is the easiest way. Although beautiful men and women are attracted to each other. If they are too far apart, the chance for them to come for each other is slim. The same goes for electrons and holes. However, increasing the distance between P1 and N2 will inevitably reduce the integration density of the chip.

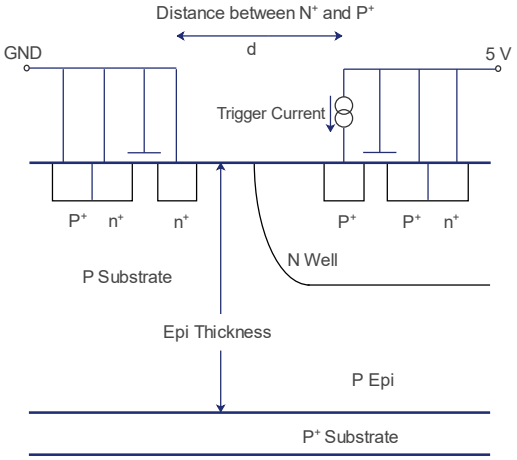
2. Add isolation between NMOS and PMOS, such as STI (Shallow Trench Isolation, process below 0.25 μm) and FOI (Field Oxide Isolation, process above 0.35 μm). Beautiful men and women feel that the road is bumpy and full of obstacles, so they are not willing to run around.

3. Deep isolation—SOI (Silicon on Insulator), is to completely isolate NMOS and PMOS on individual silicon (Si) islands. This completely separates the electrons from the holes. The Cowherd and the Weaver Girl are separated from each other, so they can only miss each other without a chance to meet again.

4. In the retrograded well process, high-energy ion implantation is used to inject impurities into the bottom of the well. The retrograded well is not like the conventional well with the highest concentration on the surface and the lowest concentration at the bottom of the well, but the opposite. Thus, it is called a retrograded well, and the concentration at the bottom of the well is the highest. After the electrons and holes reach the base, the high concentration deep well can effectively increase recombination. Men and women linger here and are not willing to go elsewhere.

5. Epitaxial (Epi) Wafer is a lightly doped epitaxial layer added to a heavily doped substrate as the substrate for the CMOS process. Therefore, CMOS is directly built on the lightly doped Epi layer. When this epitaxial layer is thin enough, the carrier of the PNP does not want to go to the NPN. However, it runs to the more comfortable heavily doped substrate because the concentration of the heavily doped substrate is higher than that of the epitaxial layer.

As shown in Figure 3, it is obvious that the thinner the epitaxial layer, the better. However, it can't be too thin, otherwise, the ions of the heavily doped substrate will diffuse into the epitaxial layer, causing a change in ion concentration. In Figure 3, the 3-μm epitaxial layer has the largest trigger current (the current that triggers the latch-up) and is the least likely to cause latch-up. The epitaxial layer can effectively suppress latch-up, which is the main reason for using the epitaxial layer. However, the disadvantage of the Epi wafer is that it is expensive.



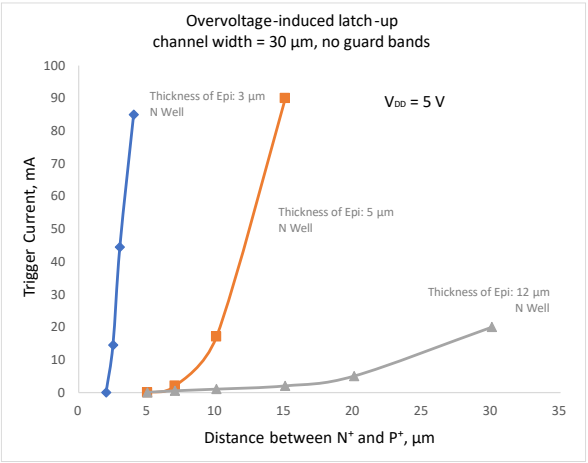
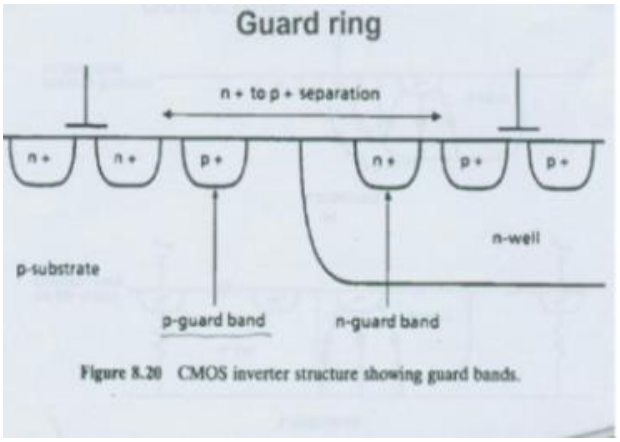


Figure 3. Epitaxial Layer Process and Its Influence on Latch-Up Trigger Current

6. Guard Ring, add a guard ring between P1 and N2, the purpose is to absorb electrons and holes at the guard ring. As shown in Figure 4.



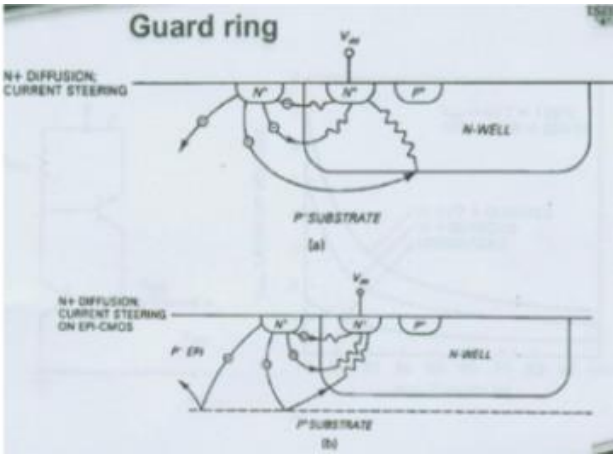


Figure 4. Schematic Diagram of Guard Ring and the Influence of N-Guard Ring on Carrier Travel

7. Design Rule, which is relatively easy to understand, is to specify the distance between P1 and N2. The width of the guard ring, the distance between the guard ring and P1 and N2, etc., when drawing the layout.

But with so many solutions, which one should be used? The answer is actually very simple, use as many as possible! But also consider the chip size and cost.

4. System-Level Latch-up

The main potential situations that cause latch-up at the system level are:

1) During the system operation or maintenance process, the PCB board is unplugged or plugged into the charged system.

2) The system has multiple power supplies, such as ±12 V, 5 V, and ground, or although the voltage is the same, they are powered by different voltage groups, such as 5-V regulated power supply and 5-V unregulated power supply.

3) The various power sources on the circuit board use complex decoupling methods, especially in multi-power systems.

4) Integrated chips on different PCBs are connected through backplanes or ribbon cables.

5) A chip drives a large capacitive load, such as long data lines or address buses.

6) The inductance introduced by the high-speed and long data or address bus leads to over voltage.

7) The system has I/O ports easily accessible to end users.

8) Digital ICs and analog ICs are in the same system.

The following will analyze the reasons that may cause latch-up in each of the above eight situations one by one. Corresponding solutions will be proposed, so that system design engineers can respond calmly to problems without being at a loss.

5. Support for Hot-Swappable PCB Board

If not handled in advance, the hot-swappable PCB board may trigger latch-up in several ways. One potential hazard is that input-output (I/O) pins may come into contact with the charged motherboard before the power pins. The circuits connected to the system will power on the I/O pins of the PCB board before the power pins. Although the difference in power-on time is very short, as long as the voltage of the I/O pins exceeds the power supply voltage and reaches Vlatch, it may trigger the parasitic SCR structure of the I/O terminal to enter latch-up. It should be noted that even tri-state output pins are prone to latch up. The output pins are in a high-impedance state, which only indicates that the output pins to the power supply or ground are in a high-impedance state. However, as long as the voltage of the output pins exceeds the power supply voltage or is lower than the ground voltage to reach Vlatch, latch-up may be triggered. One solution is to place the power supply and the ground on both sides of the PCB,

which ensures that the power supply and the ground are always powered on the motherboard before the I/O is inserted. As shown in Figure 5.

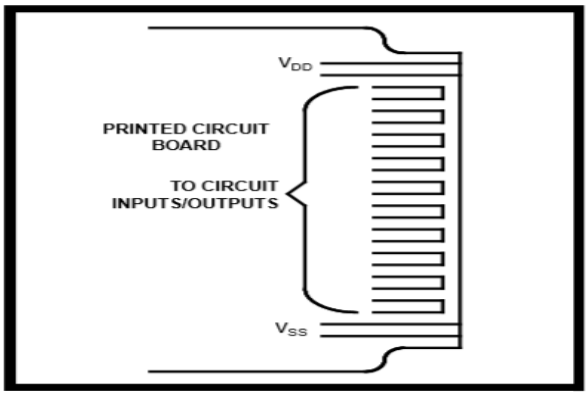


Figure 5. Put the Power Supply and Ground at both Ends of the Plug Board to Prevent I/O from being Connected to the Power Supply and Ground.

6. Multi-Power System Board

Another hot-swappable case is a multi-power system board, where the decoupling capacitance values of each power supply may differ greatly. As shown in Figure 6. Assuming that the 12-V power supply, ground, and 5-V power supply are connected to the motherboard successively, and C1>>C2. When the ground is connected, the voltage on the 5-V power supply line may be pumped up to 12 V. If the voltage exceeds the breakdown voltage of the avalanche connected to each component on the 5-V power supply line, latch-up may be triggered. The greater the difference between the various power sources in a multi-power system, the more obvious this problem becomes. The reason is that the possibility of overvoltage in components connected to lower power sources is higher. A typical example is a telephone exchange system, which includes -48 V, +5 V, and other supply voltages.

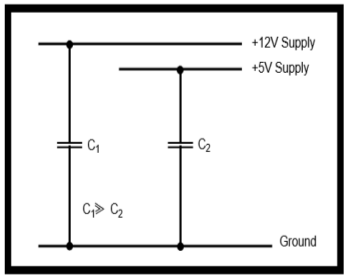


Figure 6. Multiple Power Supplies and Quite Different Decoupling Capacitors

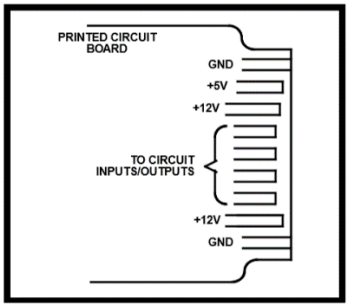


Figure 7. The Order of Distribution of Multiple Power Supplies on the Plug Board

This problem can also be solved by optimizing the PCB design. The safest solution is to connect the lower voltage power supply to the motherboard first. As shown in Figure 7, for +5 V, +12 V, -12 V, and ground, the connection sequence should be ground, +5 V, and then +12 V and -12 V should be connected to the power supply at the same time. The reverse connection can ensure that each power supply will not cause overvoltage due to decoupling capacitors. Remember, the ground should

always be the first pin to connect to the motherboard, ensuring that the positive power supply is not pulled negatively, and the negative power supply is not pulled positively.

In addition, on multi-power supply system boards, it is necessary to use decoupling capacitors with the same capacitance value for each power supply pin as much as possible.

If all these precautions have been taken and the system still has overvoltage, it is necessary to take current limiting measures. The simplest measure is to connect a resistor in series with the power supply (Vdd or Vss). The resistance value can be calculated by the following equation.

$$R = (Vsupply - Vddmax)/Iddmax$$

Where,

- Vsupply is the highest overvoltage that occurs on the system.
- Vddmax is the highest voltage that the power supply can withstand, and Iddmax is the current at Vddmax.

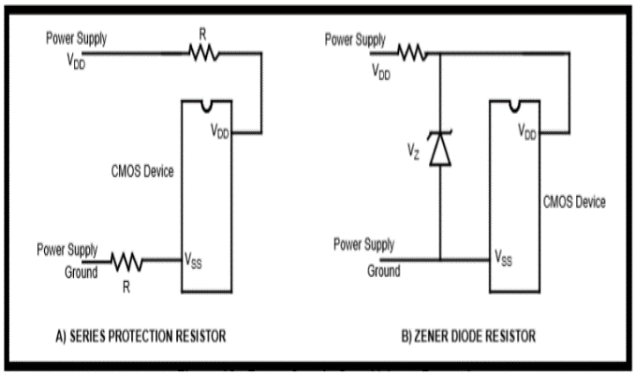


Figure 8. Connect a Current-Limiting Resistor in Series with the Power Supply or Add a Clamping Diode

If the current limiting resistance is too large, which affects the drive capability, speed, or noise immunity of the output circuit (output drive, speed, or noise immunity), as shown in Figure 8, a zener diode can be used to connect between Vdd and Vss to prevent overvoltage. Despite the use of a zener diode, a current-limiting resistor may still be required to protect the zener diode itself. However, the added resistance may not need to be too large.

For hot-swappable PCB boards, there is also a risk that the decoupling capacitor is too small. Inserting or removing PCB boards may cause transient pulses of the power supply voltage. As mentioned earlier, fast dv/dt may trigger latch-up. The solution is to add a large enough decoupling capacitor. However, it is also necessary to consider matching decoupling capacitors on other power supplies on the PCB to avoid decoupling capacitor-related issues.

In addition to the transient pulses caused by

hot-swappable on the power line, there are many other factors that cause transient pulses, such as high-speed switching and high-current ICs (such as ECL, Schottky TLL) driving heavy current loads. In addition, the back EMF generated by inductive loads may also generate severe voltage pulses. At this time, as shown in Figure 9, high-frequency capacitors, such as 0.01~0.1-μF ceramic capacitors ~~(ceramic capacitors)~~ can be used to connect to the IC power supply. At the same time, it is better to add a flyback diode to clamp the magnitude of the back EMF surge.

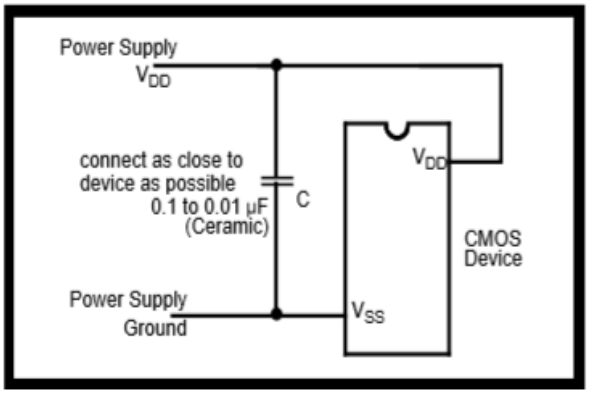


Figure 9: Adding a High-Frequency Decoupling Capacitor to the Power Supply to Filter Out Power Supply Glitches

7. Multiple Power Supplies and the Decoupling Circuits

As mentioned earlier, in a multi-power supply system, it is necessary to pay attention to the power-on and power-off sequences of each power supply. The ground needs to be connected first, and then the power should be turned on starting from the power supply with the lower voltage. The purpose is to prevent overvoltage at the input and output pins of the PCB board from the design stage. For example, if a device is powered by +5 V and is connected to a device powered by +7 V, under stable conditions, the output voltage from the 5-V power domain will be lower than the 7-V power domain. However, during the power-on process, the 5-V power domain may be higher than the 7-V power domain, as shown in Figure 10. The output voltage of the device connected to the 5-V power domain may exceed the power supply voltage of the 7-V power domain for a short time, leading to a latch-up in the device connected to the 7-V power supply.

Even if the power supply voltage is the same, similar situations may occur if they are powered by different power supplies. During power-up, even a very short overvoltage pulse may trigger a latch-up problem.

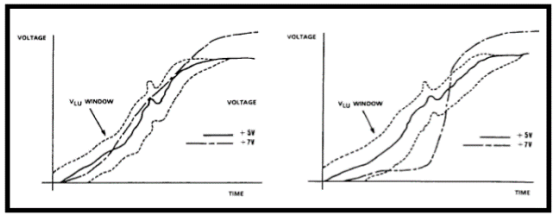


Figure 10 The Risk of Latch-Up during Power-On of Multiple Power Supplies

As shown in Figure 11, adding a diode between the two sets of power supplies can ensure that before the higher voltage power source is established, the higher voltage power source will only differ from the lower voltage power

source by the voltage of a diode. If the voltages of the two sets of power supplies are equal, connect them with back-to-back diodes.

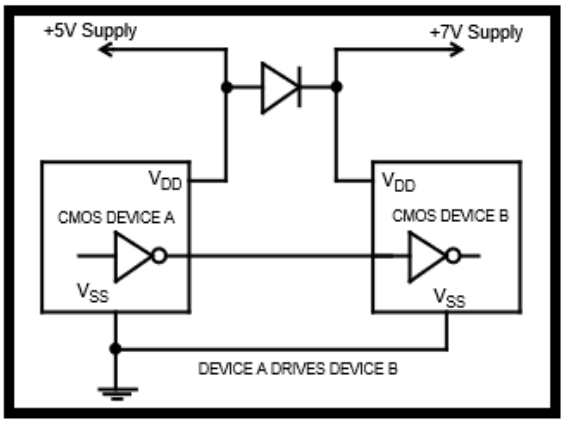


Figure 11 Diode Coupling Circuit between Multiple Power Supplies

8. The Connection between Different PCB Boards

In the same system, the consideration of the drive connection between different PCB boards, as mentioned in the previous sections on hot-swappable PCB boards, multiple power supplies, and their decoupling circuits. The potential risk of I/O pins is when the power supply has not yet been turned on yet, the I/O circuit has been connected to the energized motherboard or other PCB board, which triggers a latch-up. The solution is to connect the ground and power supply in order from low to high voltage near the edge of the PCB board and place the input and output pins in the middle of the PCB. However, for different PCB boards, even if each PCB board has only one set of power supplies, the decoupling capacitors of the power supplies on each PCB board should be carefully considered. If one PCB board has a larger capacitor than another PCB board, it may cause different power-up speeds. PCB boards with smaller decoupling capacitors will power on faster. Thus, it may cause their output voltage to be higher than the power voltage of the next PCB board, leading to a latch-up as described in the multi-power supply and decoupling circuit section.

Therefore, whenever possible, the decoupling capacitors on each PCB board in the entire system should use the same capacitance value as much as possible. If possible, all output pins should remain in a high-impedance state during the power-on and power-off processes, so even if there is a voltage difference between PCB boards, no output current triggers the latch-up.

In addition, a current-limiting resistor can also be connected in series on the input and output pin where overvoltage may occur. The size of the resistor can be calculated by the following equation.

$$R = \frac{Vdiff - 0.3\,V}{10\,mA}$$

Where,

- Vdiff is the maximum voltage difference that may occur between two power supplies.

Of course, increasing the current-limiting resistor brings negative effects as mentioned

before, such as current drive capability, speed, and noise immunity. As mentioned earlier, there are usually 0.3-V voltage and 10-mA current limits for input and output pins in the product datasheet, where 0.3 V and 10 mA are for mass production testing and are written into the datasheet. In practice, the voltage (Vlatch) that triggers latch-up usually exceeds the power supply or ground by 0.6 V~2 V, and the current (Ilatch) that triggers latch-up ranges from 50 mA to several hundred mA.

9. Large Capacitance Load

A long address or data bus can introduce very large parasitic capacitances. A chip driving long address or data buses may encounter an overvoltage condition, triggering a latch-up. Especially on the same PCB board. When large current loads are switched at the same time, for example, when a group of LEDs is doing a lamp test, overvoltage may occur. Changes in the power supply current can cause a local voltage to drop on the power supply pins. This is because a large current flows through the resistance of parasitic traces on the power supply line and the contact resistance of the connector to generate a voltage drop. At the same time, the capacitance on the line keeps the voltage at the I/O terminal from changing, as shown in Figure 12. If the voltage difference between the power supply and the I/O terminals is large enough, the bus capacitance will be discharged through the I/O structure. The discharge current may reach tens of milliamps, which may trigger latch-up.

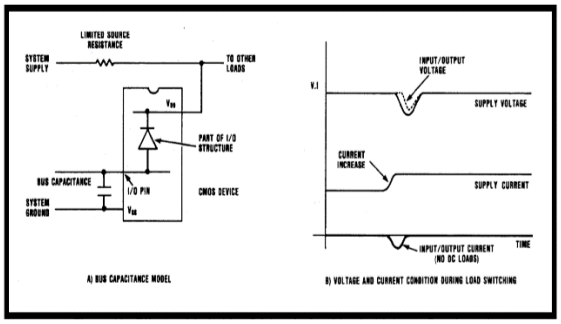


Figure 12. Voltage Difference between I/O and Power Supply caused by Power Line Resistance and Large Capacitive Load

Therefore, at the beginning of the PCB board design, it should be considered to minimize the trace resistance on the power supply line and the parasitic capacitance on the bus as much as possible. Such as using wider power traces and lower contact resistance of the connector. The address and data buses should be as short as possible, and the distance between them should be as far apart as possible. After taking these measures, if latch-up still occurs, decoupling capacitors can be added between the power supplies to reduce voltage fluctuations on the power supplies. The value of the capacitance depends on the value of the local current and the trace resistance on the power supply line, usually, a 10-μF capacitor is sufficient.

10. Inductive Load

Ribbon Cables, as long-distance buses, in addition to paying attention to the problem of large capacitance load mentioned in the previous section, also introduce strong inductance. A sufficiently large capacitance and

inductance form a second-order circuit. When outputting faster signals, it may cause oscillations. As shown in Figure 13, if the oscillation amplitude is large enough, the voltage of the output signal may exceed the power supply voltage. If it reaches Vlatch, a latch-up will be triggered.

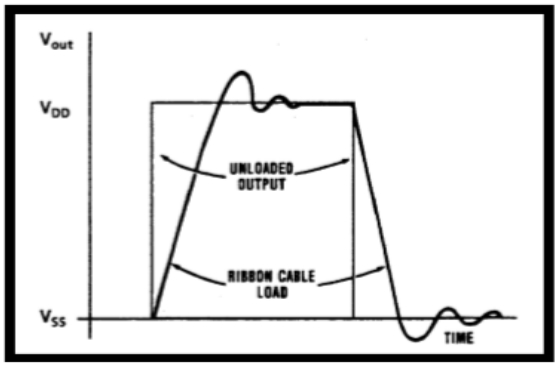


Figure 13. Capacitance and Inductance Causing the Output Signal to Superimpose a Large Amplitude Oscillation

The solution is to add appropriate resistors at both ends of the ribbon cable. However, the added resistors cause additional power dissipation. Another solution, as shown in Figure 14, is to add a protection diode at the I/O end, which can clamp the overvoltage pulse. If a common diode still causes latch-up, a Schottky diode may be needed to ensure a sufficiently fast and low clamping voltage. Thus, the I/O voltage does not exceed the power supply voltage and reaches Vlatch, thereby avoiding triggering the latch-up of the I/O port circuit.

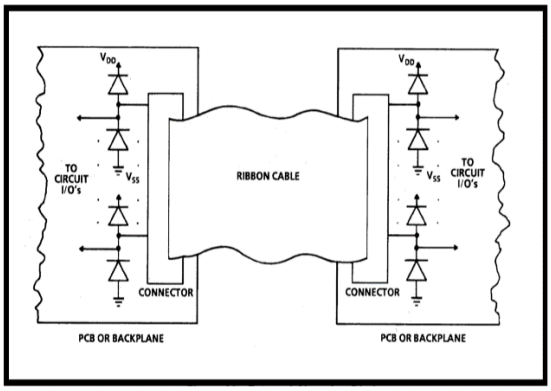


Figure 14 Adding a Diode to the I/O Terminal to Clamp the Voltage Difference between the I/O and the Power Supply

11. Easy Access to I/O Ports

Ports that are easily accessible to end users are prone to latch-up caused by electrostatic discharge or abnormal power-on by users. If the I/O voltage is powered on before the power supply, the voltage of I/O port will be higher than the power supply voltage, which may trigger latch-up in the I/O port circuit.

One of the solutions is to connect a current limiting resistor in series with the port circuit. However, as mentioned earlier, the current limiting resistor may affect the speed and noise immunity of the port.

12. Digital IC and Analog IC are on the Same System Board

In the same system board, there are analog and digital power pins, especially with different power supply voltages, which may have

potential risks of overvoltage that may trigger latch-up. For example, an analog comparator with a power supply voltage of ± 10 V drives a digital circuit with a power supply of +10 V. When the output of the comparator is low, i.e., -10 V, its potential is much lower than the lowest potential VSS (0 V) of the digital circuit. If the driving current of the comparator is large enough, it may trigger the latch-up of the I/O port in the digital circuit. Of course, a current-limiting resistor can be added to the digital input to limit the triggering of the latch-up. However, a more recommended solution is to use a resistor divider at the digital input, as shown in Figure 15. When the output of the comparator is low, there is a voltage of 20 V (+10 V~-10 V) on the resistor divider. Thus, the input voltage of the digital circuit is half of the voltage on the voltage dividing resistor, that is, 0 V. When the output voltage of the comparator is high, no current flows through the voltage divider. Therefore, the input of the digital circuit is VDD. The input impedance of CMOS inputs is generally very high, so a very large resistor can be used as a resistor divider to reduce power consumption.

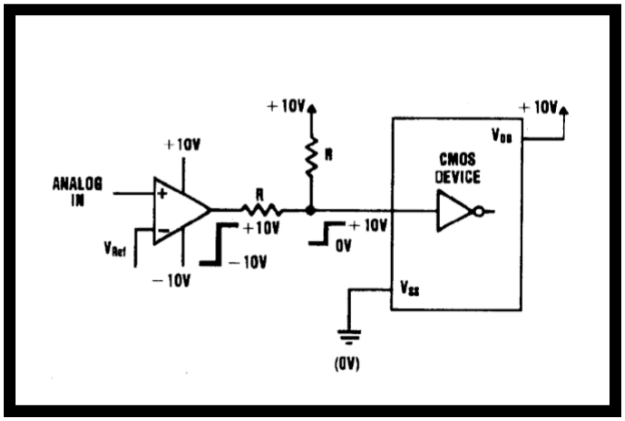


Figure 15 Connection between Analog IC and Digital IC

Finally, the author hopes that through this article, chip design engineers, chip layout design engineers, system design engineers, and application engineers can understand the SCR structure and the mechanism of latch-up. Thus, they can deal with latch-up problems calmly without being at a loss.