# TPS325M51C5 Errata

## Introduction

This document applies to TPS325M51 product series, as shown in Table 1-1.

**Table 1-1 Applicable Devices**

| Product Series | Part Number |
|---|---|
| TPS325M51 | TPS325M5177Q-QP7T |
| | TPS325M5165Q-QP7T |
| | TPS325M5166Q-QP7T |
| | TPS325M5167Q-QP7T |
| | TPS325M5155Q-QP7T |
| | TPS325M5156Q-QP7T |
| | TPS325M5177Q-QP5T |
| | TPS325M5166Q-QP5T |
| | TPS325M5155Q-QP5T |
| | TPS325M5177Q-QP6T |
| | TPS325M5166Q-QP6T |
| | TPS325M5177Q-FSDR |
| | TPS325M5177I-FSDR |
| | TPS325M5166I-FSDR |
| | TPS325M5156I-FSDR |

## Summary of Device Errata

**Table 1-2 Errata and Information Summary**

| Errata ID | Errata Title |
|---|---|
| ERR0001 | RTC: RTC CR register configuration issue due to short time frame between two consecutive CR register writes |
| ERR0002 | RTC: RTC timestamp interrupt is generated by RTC wakeup or RTC alarm if they are enabled |
| ERR0003 | PMU: stop retention bit does not work as expected |
| ERR0004 | SPI: SPI Overflow flag will be cleared by reading STAT register following by DATA register |
| ERR0005 | SPI: MISO line glitch when using SPI as slave with FIFO mode |
| ERR0006 | EXTI: Event trigger for certain peripherals does not work |
| ERR0007 | ADC: Timer might fail to trigger ADC when using HCLK as ADC clock source |
| ERR0008 | I2C: I2C DMA request issue |
| ERR0009 | DMA: DMA interrupt flags set issue for polling mode |

## Revision History

| Date | Revision | Changes |
|---|---|---|
| 2023-11 | Rev.A.0 | Initial revision. |

# Errata Description

## ERR0001: RTC: RTC CR register configuration issue due to short time frame between two consecutive CR register writes

### Description

Two consecutive RTC CR register writes to set time stamp function (with first write to configure RTC time, second write to enable time stamp function) do not work if these two steps occur in a time frame less than 4ms. There is no problem if above two steps RTC CR writes are combined in one register write.

### Workaround

Software must make sure at least 4ms delay between RTC CR writes.

## ERR0002: RTC: RTC timestamp interrupt is generated by RTC wakeup or RTC alarm if they are enabled

### Description

Both RTC alarm event and RTC wakeup event can trigger RTC timestamp interrupt when their corresponding interrupt enable is opened, so it needs additional operation to identify which event(RTC wakeup or RTC alarm) happens even when the RTC timestamp interrupt is triggered.

### Workaround

If RTC alarm interrupt or wakeup timer interrupt is enabled together with timestamp interrupt, make sure to set time stamp IRQ priority lower than the other two interrupt events, and clear alarm or wakeup timer flag in their ISR first, then handle remaining time stamp interrupt event in timestamp ISR.

## ERR0003: PMU: stop retention bit does not work as expected

### Description

PMU CR01.STOPSRAM* bits do not power down associated SRAM when configured to ‘0’ for power down function.

### Workaround

No, will be fixed in next revision silicon.

## ERR0004: SPI: SPI Overflow flag will be cleared by reading STAT register following by DATA register

### Description

Current SPI RX overflow clearing sequence implemented as reading STAT register followed by DATA register, it has risk to wrongly clear overflow flag in user implemented SPI ISR code.

### Workaround

Add additional register access in between reading STAT and DATA register in user ISR routine to avoid clearing overflow flag.

## ERR0005: SPI: MISO line glitch when using SPI as slave with FIFO mode

### Description

There are glitches on MISO line when configuring SPI in slave and FIFO mode, this would potentially cause wrong SPI data transfer.

### Workaround

Only use SPI in buffer mode when configuring SPI as slave.

## ERR0006: EXTI: Event trigger for certain peripherals does not work

### Description

Event trigger for several peripherals does not work, including EXTI event trigger TPSensor® conversion, EXTI event trigger ADC conversion and timer compare event trigger ADC conversion.

### Workaround

For above mentioned scenario, use EXTI interrupt instead.

## ERR0007: ADC: Timer might fail to trigger ADC when using HCLK as ADC clock source

### Description

ADC triggering with timer sometimes fails when using HCLK as ADC clock source.

### Workaround

Use dedicated PLL clock for ADC.

## ERR0008: I2C: I2C DMA request issue

### Description

DMA transfer starts once after configuring DMA channel for I2C but having not set I2C TXDMAEN or RXDMAEN.

### Workaround

Follow the sequence below to avoid the issue:

1. Initialize DMA with channel disabled.
2. Initial I2C initial with I2C TX or RX DMA enabled.
3. Enable DMA channel.

## ERR0009: DMA: DMA interrupt flags set issue for polling mode

### Description

DMA interrupt flags are not set as expected when DMA works in polling mode.

### Workaround

Set DMA interrupt enable bits but not enable DMA IRQ in NVIC when using DMA in polling mode.

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