

TPS325M5 Series

Mainstream Line of TPS32 ARM-based Industrial Microcontrollers

Built-in TPSensor® Capacitive Sensing Technology



The TPS325M5 Series adopt Arm®v8-M Architecture based STAR-MC1 core compatible with Cortex®-M33 instruction set. The TPS325M5 Series belongs to Mainstream Line of TPS32 mixed-signal industrial microcontroller family with built-in 3PEAK TPSensor® Capacitive Sensing technology, offering comprehensive portfolios with 3PEAK powered rich integrated analog and peripherals to fulfill wide spectrum of application needs.

3PEAK TPSensor® – BEST IN CLASS CAPACITIVE SENSING TECHNOLOGY

PERFORMANCE

TPSensor® offers 10fF resolution and up to 120x SNR

- ◆ High Sensitivity, support thick overlay
- ◆ Parasitic capacitance compensation
- ◆ Hardware oversampling
- ◆ Sliders and wheels up to 10-bit useable resolution

RELIABILITY

Support for IEC61000-4-x noise immunity compliance

- ◆ Features frequency hopping technology
- ◆ On-chip calibration capacitors for self-test and calibration
- ◆ Moisture and spill reference designs

FLEXIBILITY

Supports Multi Modes

- ◆ Various combinations and permutations of button, slider, wheel sensors
- ◆ Self and Mutual Capacitance electrodes on same design

LOW POWER CONSUMPTION

Optimized for Lower Power Operation

- ◆ 5 uA with wake on touch state machine
- ◆ Wake-on-Touch hardware state machine while CPU in low power modes

EASE OF USE

TPSensor® ecosystem for easy BSW (Button, Slider, Wheel) design and development

- ◆ Easy to use TPSensor® Designer GUI, source code generation.
- ◆ Software library with a PDL, basic touch layer, advanced feature layer and communications layer
- ◆ Variety of documentation resources

TARGET APPLICATIONS

- ◆ Smart Lock
- ◆ Smart Home
- ◆ Home Appliances
- ◆ Human Machine Interface

SMART LOCK SOLUTION BASED ON TPS325M51 SUB SERIES



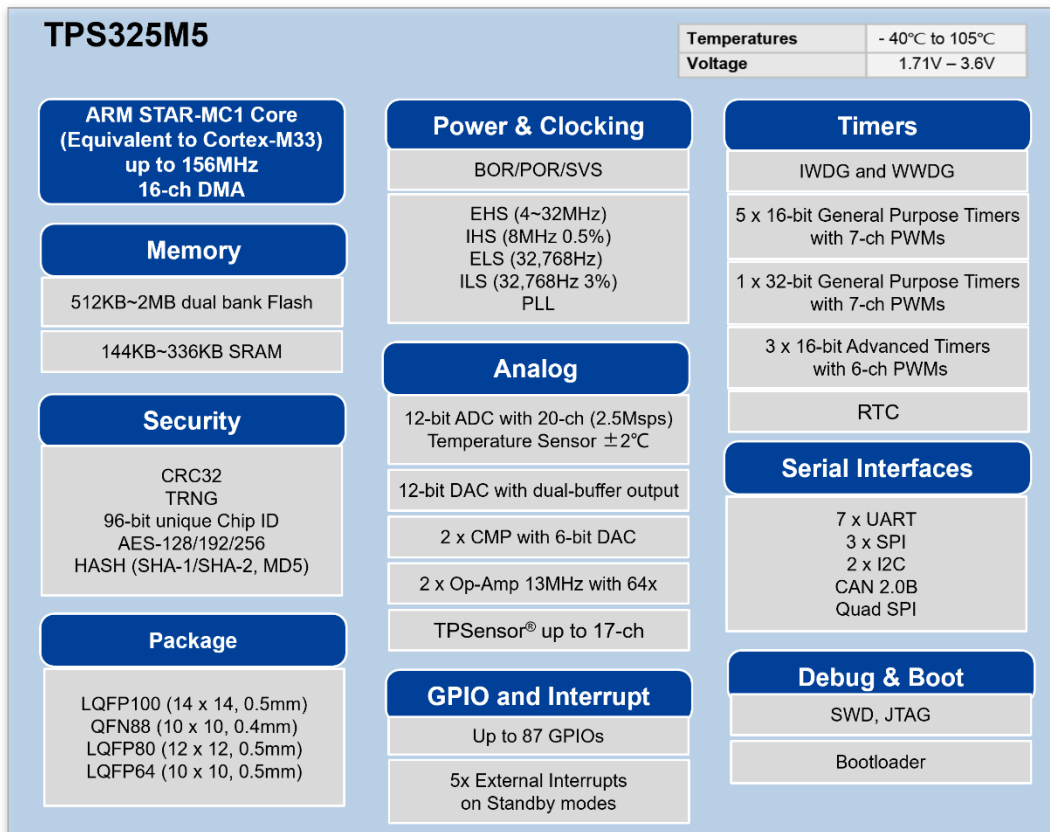
- ◆ 5 all 1 Solution (TPSensor®, 2ch Audio output, FP algorithms, NFC RFID, OLED Display)
- ◆ High performance/Noise immunity on TPSensor® active in Standby mode @ 5µA
- ◆ Up to 7 UARTs, 3 SPI, 2 I2C for easy expansion to support extra feature recognition such as face recognition, wireless connectivity etc.
- ◆ Ultra-low power, support battery change mode (1min @47uF)
- ◆ Easy PCB Layout for 2-Layer board
- ◆ QFN88 with up to 79 GPIOs in 10x10 small footprint

HUMAN MACHINE INTERFACE SOLUTION BASED ON TPS325M5A SUB SERIES



- ◆ High performance/Noise immunity on TPSensor®
 - Up to 13 touch inputs in self mode and 42 touch inputs in mutual mode
 - Water tolerance TPSensor® to avoid false detection.
- ◆ Support both SPI and 16-bit 8080 interface
- ◆ Up to 336KB larger SRAM for display buffer

TPS325M5 SERIES BLOCK DIAGRAM



KEY FEATURES

Performance

- ◆ 32-bit STAR-MC1 core with FPU based on Arm[®] v8-M architecture
- ◆ Compatible with Cortex[®]-M33 instruction set
- ◆ Operation frequency up to 156 MHz
- ◆ 8KB Data Cache /Instruction Cache
- ◆ 64KB ITCM/ 32KB x 2 DTCM
- ◆ Dual DMA with eight channels each

Analog

- ◆ One 12-bit ADC with 14-external and 6-internal channels. Resolution up to 12-bit at 2.5Msps.
- ◆ One 12-bit DAC channels, up to 1 Msps, 2 x buffered external channels
- ◆ Two fast rail-to-rail analog comparators (CMP) with built-in 6-bit DAC for internal voltage reference
- ◆ Two operational amplifiers (OA) that can be used in PGA/buffer/GP mode

Memory

- ◆ 512KB to 2MB Dual Bank Flash memory with allows a read-while-write capability
- ◆ Readout protection (RDP) and Write protection (WRP) for Flash memory
- ◆ 144KB~336KB SRAM memory
- ◆ 32K systems memory with integrated bootloader

HMI

- ◆ TPSensor[®] capacitive sensing interface supports up to 17 external channels (including one Guard channel)
 - ◆ Support self and mutual mode
 - ◆ Support button, slider, wheel sensors
 - ◆ Moisture and spill tolerance
 - ◆ High noise immunity with high SNR
 - ◆ Quick response time with ultra-low power

Serial Interfaces

- ◆ Two I2C fast mode plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from stop mode
- ◆ Seven UARTs(LIN, MODBUS) with DMA support
- ◆ Three SPI with DMA support
- ◆ Quad SPI Interface
- ◆ CAN 2.0B

Timers

- ◆ Five 16-bit and one 32-bit general purpose timers, each with 7 x PWM channels
- ◆ Three 16-bit advanced timer for motor control with up to 6 x PWM channels per each, dead time regeneration and emergency stop
- ◆ IWDG and WWDG
- ◆ SysTick Timer
- ◆ Real Time Clock with Calendar

Security

- ◆ 96-bit unique Chip ID
- ◆ Cyclic Redundancy Check (CRC32)
- ◆ True random number generator (TRNG)
- ◆ AES: 128/192/256-bit key encryption hardware accelerator
- ◆ HASH: SHA-1/SHA-2, MD5

Low Power Consumption

- ◆ Ultra-low static and dynamic power consumption by fine tune multiple low power modes:
 - ◆ sleep, stop, standby and shutdown modes
 - ◆ up to 2.6µA@shutdown mode with RTC
 - ◆ up to 3µA @ standby mode with RTC and 16KB retention RAM
 - ◆ <5µA in standby/stop mode can be awoken by TPSensor® touch event

Supply Voltage, Temperature and Package

- ◆ Supply Voltage: 1.71~3.63V
- ◆ -40 ~ 85°C and -40 ~105°C
- ◆ LQFP100, LQFP80, LQFP64, QFN88

TPS325M5 PORTFOLIO

There are two sub series included in TPS325M5 Portfolio. The differentiation list can be found as follows:

| TPS325M5 Portfolio | Description | Memory | | GPIOs | Analog | Package | Temperature Range(°C) |
|--------------------|---|-----------|---------|-------|-----------------|------------------------------|-----------------------|
| | | Flash(KB) | RAM(KB) | | | | |
| TPS325M5I | Rich analog functions for both industrial and consumer applications | 512-2048 | 144-336 | 55-87 | ADC,DAC,OPA,CMP | LQFP64;LQFP80; QFN88;LQFP100 | -40-85;-40-105 |
| TPS325M5A | HMI Application Specific Standard Product | 512K | 336 | 56 | ADC,DAC,OPA,CMP | LQFP64 | -40-105 |

TPS325M5A Sub Series Options

| TPS325M5A Sub Series Part Number | Max CPU Frequency(MHz) | Memory | | HMI TPSensor® Capacitive Sensing [Number x Channels] | Communication | | | | | Timers | | | | Analog | | | Additional Key Features | Total GPIO | Package | | | | Temperature Range(°C) | | |
|--|------------------------|-----------|---------|---|---------------|------|-----|-----|-------|--------|----------------|----------------|------------------|--------|---|--------------------|-------------------------|------------|--------------------------|-----|-----|-----|-----------------------|-----|---------|
| | | Flash(KB) | RAM(KB) | | CAN | QSPI | SPI | I2C | USART | I2S | General Timers | Advance Timers | Watchdog Timer/s | RTC | ADC[Number x Bits] @ [Conversion Rate] | DAC[Number x Bits] | | | OPA | CMP | QP5 | QP6 | | FSD | QP7 |
| | | | | | | | | | | | | | | | | | | | | | | | | | |
| TPS325M5A57 | 156 | 512 | 336 | 1x17ch | 1 x CAN 2.0B | 1 | 3 | 2 | 6 | 3 | 6 | 3 | 2 | 1 | 1 x 12bit @ 1MSPS SAR ADC | 1 x 12bit | 2 | 1 | TRNG; MD5; SHA; AES-256; | 56 | ✓ | - | - | - | -40-105 |

TPS325M51 Sub Series Options

| TPS325M51 Sub Series Part Number | Max CPU Frequency(MHz) | Memory | | HMI TPSensor® Capacitive Sensing [Number x Channels] | Communication | | | | | | | Timers | | | | Analog | | | Additional Key Features | Package | | | | Temperature Range(°C) | | | |
|--|------------------------|-----------|---------|---|---------------|------|-----|-----|-------|-----|----------------|----------------|-----------------|-----|---|--------------------|-----|-----|--------------------------|--------------------------|--------|--------|---------|-----------------------|---------|---------|---------|
| | | Flash(KB) | RAM(KB) | | CAN | QSPI | SPI | I2C | USART | I2S | General Timers | Advance Timers | Watchdog Timers | RTC | ADC(Number x Bits) @ [Conversion Rate] | DAC(Number x Bits) | OPA | CMP | | Total GPIO | QP5 | QP6 | FSD | | QP7 | | |
| | | | | | | | | | | | | | | | | | | | | | LQFP64 | LQFP80 | QFN68 | | LQFP100 | | |
| TPS325M5155 | 156 | 512 | 144 | 1x13ch | 1 x CAN 2.0B | 1 | 3 | 2 | 6 | 3 | 6 | 3 | 2 | 1 | 1 x 12bit @ 1Mps SAR ADC | 1 x 12bit | 2 | 1 | TRNG; MD5; SHA; AES-256; | 55 | ✓ | - | - | - | -40-105 | | |
| | | | | 1x17ch | 1 | 3 | 2 | 7 | 3 | 6 | 3 | 2 | 1 | 2 | TRNG; MD5; SHA; AES-256; | | | 87 | - | - | - | ✓ | | | | | |
| TPS325M5156 | 156 | 512 | 208 | 1x17ch | 1 x CAN 2.0B | 1 | 3 | 2 | 7 | 3 | 6 | 3 | 2 | 1 | 1 x 12bit @ 1Mps SAR ADC | 1 x 12bit | 2 | 2 | TRNG; MD5; SHA; AES-256; | 79 | - | - | ✓ | - | -40-85 | | |
| | | | | 1x17ch | 1 | 3 | 2 | 7 | 3 | 6 | 3 | 2 | 1 | 2 | TRNG; MD5; SHA; AES-256; | | | 87 | - | - | - | ✓ | -40-105 | | | | |
| TPS325M5165 | 156 | 1024 | 144 | 1x17ch | 1 x CAN 2.0B | 1 | 3 | 2 | 7 | 3 | 6 | 3 | 2 | 1 | 1 x 12bit @ 1Mps SAR ADC | 1 x 12bit | 2 | 2 | TRNG; MD5; SHA; AES-256; | 87 | - | - | - | ✓ | -40-105 | | |
| TPS325M5166 | 156 | 1024 | 208 | 1x17ch | 1 x CAN 2.0B | 1 | 3 | 2 | 7 | 3 | 6 | 3 | 2 | 1 | 1 x 12bit @ 1Mps SAR ADC | 1 x 12bit | 2 | 2 | TRNG; MD5; SHA; AES-256; | 79 | - | - | ✓ | - | -40-85 | | |
| | | | | 1x13ch | | 1 | 3 | 2 | 6 | 3 | 6 | 3 | 2 | 1 | | | | 1 | | TRNG; MD5; SHA; AES-256; | 55 | ✓ | - | - | - | -40-105 | |
| | | | | 1x17ch | | 1 | 3 | 2 | 7 | 3 | 6 | 3 | 2 | 1 | | | | 2 | | TRNG; MD5; SHA; AES-256; | 71 | - | ✓ | - | - | - | -40-105 |
| | | | | 1x17ch | | 1 | 3 | 2 | 7 | 3 | 6 | 3 | 2 | 1 | | | | 2 | | TRNG; MD5; SHA; AES-256; | 87 | - | - | - | ✓ | -40-105 | |
| TPS325M5167 | 156 | 1024 | 336 | 1x13ch | 1 x CAN 2.0B | 1 | 3 | 2 | 6 | 3 | 6 | 3 | 2 | 1 | 1 x 12bit @ 1Mps SAR ADC | 1 x 12bit | 2 | 1 | TRNG; MD5; SHA; AES-256; | 87 | - | - | - | ✓ | -40-105 | | |
| TPS325M5177 | 156 | 2048 | 336 | 1x17ch | 1 x CAN 2.0B | 1 | 3 | 2 | 7 | 3 | 6 | 3 | 2 | 1 | 1 x 12bit @ 1Mps SAR ADC | 1 x 12bit | 2 | 2 | TRNG; MD5; SHA; AES-256; | 79 | - | - | ✓ | - | -40-85 | | |
| | | | | 1x17ch | | 1 | 3 | 2 | 7 | 3 | 6 | 3 | 2 | 1 | | | | 2 | | TRNG; MD5; SHA; AES-256; | 79 | - | - | ✓ | - | -40-105 | |
| | | | | 1x13ch | | 1 | 3 | 2 | 6 | 3 | 6 | 3 | 2 | 1 | | | | 1 | | TRNG; MD5; SHA; AES-256; | 55 | ✓ | - | - | - | -40-105 | |
| | | | | 1x17ch | | 1 | 3 | 2 | 7 | 3 | 6 | 3 | 2 | 1 | | | | 2 | | TRNG; MD5; SHA; AES-256; | 71 | - | ✓ | - | - | -40-105 | |
| | | | | 1x17ch | | 1 | 3 | 2 | 7 | 3 | 6 | 3 | 2 | 1 | | | | 2 | | TRNG; MD5; SHA; AES-256; | 87 | - | - | - | ✓ | -40-105 | |

TPS325M5 SERIES DEVELOPMENT RESOURCES

Evaluation Boards

Prime Boards: TPSP-5M51A-EVM1

Prime Boards are perfect appropriate for fast prototyping with TPS32 microcontrollers' feature sets. These prime boards are easy to use with user guide, design files, development tools, and comprehensive software code examples. Prime Boards can be flexible used as standalone, with expansion boards for more functionalities, and varies additional ARDUINO® compatible shields.



TPS325M51-A Prime Board

Expansion Boards: TPSX-SER-EVM1

Expansion Boards allow the possibility for more functionality exploration. These boards can work with multiple prime boards with standard expansion connector. Complimentary documentation and software libraries and code examples are provided accordingly.



Serial Communication Expansion Board

Embedded Software

- ◆ TPS32 software development kit (SDK)
- ◆ Run-Time OS: FreeRTOS;
- ◆ TPSensor® library

Development Tools

- ◆ Integrated development environment (IDE):
Arm Keil MDK; IAR Embedded Workbench;
- ◆ Emulator: Segger J-Link; DAP-Link
- ◆ TPS32 Programmer
- ◆ TPSensor® Designer

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