SD 3.0-compatible memory card integrated auto-direction control and level translator

Features

- Supports up to 208 MHz clock rate
- SD 3.0 specification-compatible voltage translation to support: SDR104, SDR50, DDR50, SDR25, SDR12, High-Speed and Default-Speed modes
- Auto-direction sensing
- Voltage-Level Translation Between:
  - V_{CCA} Range: 1.1 V to 1.95 V
  - V_{CCB} Range: 1.7 V to 3.6 V
- Integrated pull-up resistors: no external resistors required
- Latch-up performance exceeds 100 mA per JESD78 Class II.A
- No Power-up Sequency Required for V_{CCA}, V_{CCB}
- ESD Protection:
  - HBM: All PIN ANSI/ESDA/JEDEC JS-001 class 2 exceeds 8000 V
  - CDM: All PIN ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
  - IEC: Card-side ±4000-V IEC 61000-4-2 Contact Discharge
- Specified from -40 °C to +85 °C

Applications

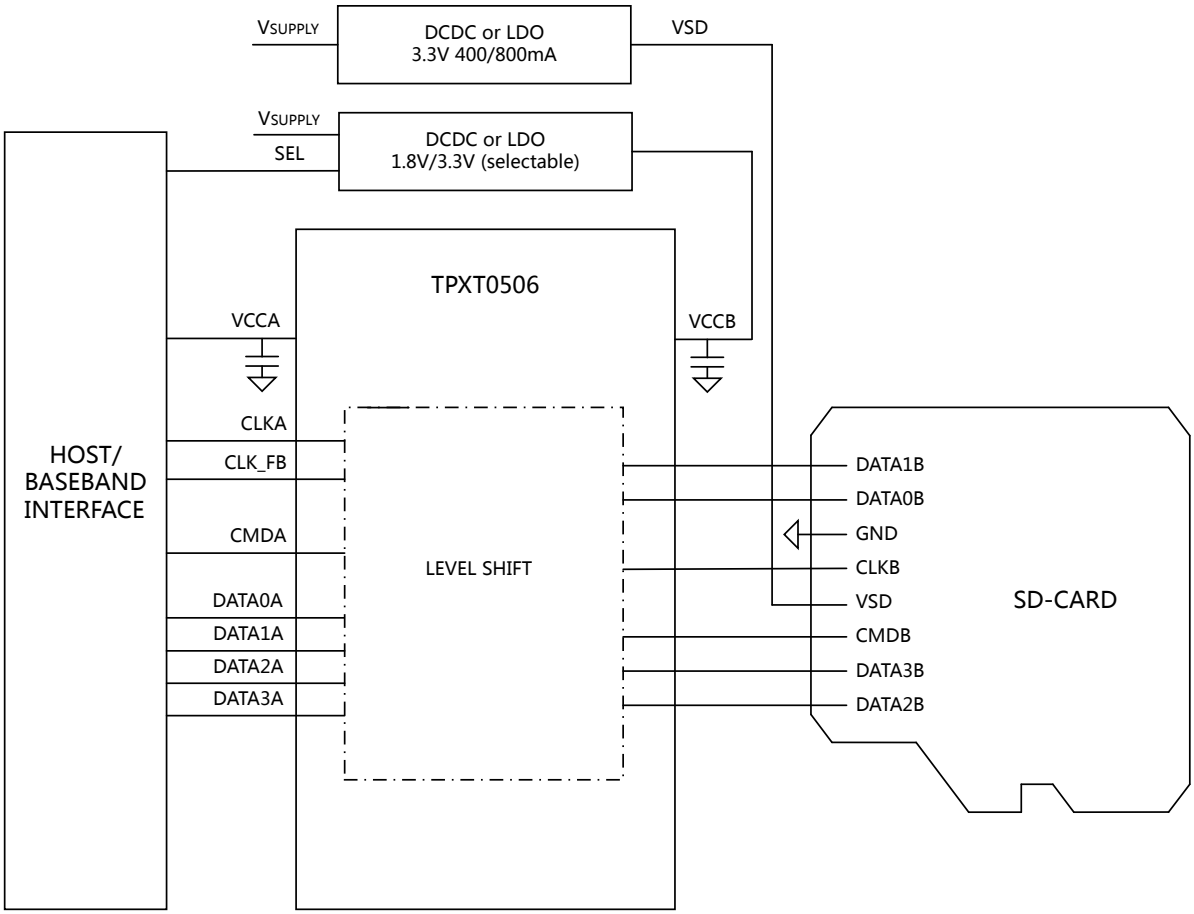
- Smartphone
- SD, MMC or microSD card readers
- Laptop computers
- Tablet PCs
- Digital cameras
- Mobile handsets

Description

The TPXT0506 is an SD 3.0-compatible bidirectional dual supply level translator with auto-direction control. It is designed to interface between a memory card operating at 1.7 V to 3.6 V signal levels and a host with a nominal supply voltage of 1.1 V to 1.95 V. The device supports SD 3.0: SDR104, SDR50, DDR50, SDR25, SDR12 and SD 2.0 High-Speed (50 MHz) and Default-Speed (25 MHz) modes.

TPXT0506 is available in WLCSP-16 package and is characterized from −40°C to + 85°C

Typical Application



SD 3.0-compatible memory card integrated auto-direction control and level translator

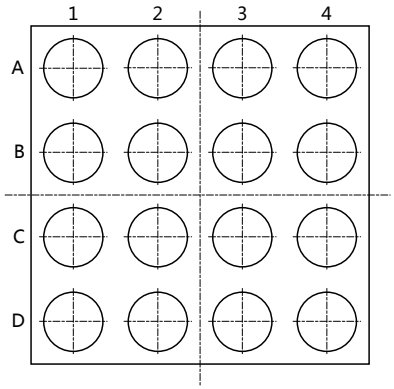
Table of Contents

Revision History

Date	Revision	Notes
2025-10-20	Pre.P.0	Initial version
2025-12-23	Pre.A.0	Released version

Pin Configuration and Functions

TPXT0506-WLPR
WLCSP-16 Package
Top View



	1	2	3	4
A	DAT2A	VCCA	VCCB	DAT2B
B	DAT3A	CMDA	CMDB	DAT3B
C	DAT0A	CLKFB	GND	DAT0B
D	DAT1A	CLKA	CLKB	DAT1B

Table 1. Pin Functions: TPXT0506-WLPR

Pin		I/O	Description
No.	Name		
A1	DAT2A	I/O	Input/output DAT2A. Referenced to V_{CCA}
B1	DAT3A	I/O	Input/output DAT3A. Referenced to V_{CCA}
C1	DAT0A	I/O	Input/output DAT0A. Referenced to V_{CCA}
D1	DAT1A	I/O	Input/output DAT1A. Referenced to V_{CCA}
A2	V_{CCA}	P	Side-A supply voltage
B2	CMDA	I/O	Command input or output on host side
C2	CLKFB	O	Clock feedback signal on host side
D2	CLKA	I	Clock signal input on host side
A3	V_{CCB}	P	Side-B supply voltage
B3	CMDB	I/O	Command input or output on memory card side
C3	GND	P	Supply ground
D3	CLKB	O	Clock signal output on memory card side
A4	DAT2B	I/O	Input/output DAT2B. Referenced to V_{CCB}
B4	DAT3B	I/O	Input/output DAT3B. Referenced to V_{CCB}
C4	DAT0B	I/O	Input/output DAT0B. Referenced to V_{CCB}
D4	DAT1B	I/O	Input/output DAT1B. Referenced to V_{CCB}

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CCA}	4 ms Transient, on Pin V_{CCA}	−0.5	4.6	V
V_{CCB}	4 ms Transient, on Pin V_{CCB}	−0.5	4.6	V
V_I	4 ms Transient, at I/0 Pins Supplied by V	−0.5	V_{CCA} + 0.3	V
	4 ms Transient, at I/0 pins supplied by VCCB	−0.5	V_{CCB} + 0.3	V
I_{IK}	Input Clamp Current, V_I< −0.3 V or V_I > VCC + 0.3 V	−20	20	mA
I_{OK}	Port A, Output Clamping Current, V_O < −0.3 V or V_O > V_{CCA} +0.3 V	−20	20	mA
	Port B, Output Clamping Current, V_O < −0.3 V or V_O > V_{CCB} +0.3 V	−50	50	mA
P_{tot}	Total Power Sissipation, Tamb = −40 °C to +85 °C		250	mW
T_{STG}	Storage Temperature Range	−55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD, Host-side and Card-side	ANSI/ESDA/JEDEC JS-001 class 3B(1)	±8	kV
CDM	Charged Device Model ESD, Host-side and Card-side	ANSI/ESDA/JEDEC JS-002 class C3(2)	±1	kV
IEC	IEC Contact Discharge	IEC-61000-4-2, Card-side	±4	kV
LU	Latch-up Performance	LU, per JESD78, All Pins	±800	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{CCA}	Supply Voltage, on Pin V_{CCA}	1.1	1.95	V
V_{CCB}	Supply Voltage, on Pin V_{CCB}	1.7	3.6	V
V_I	Host Side Input Voltage	−0.3	V_{CCA} + 0.3	V
	Memory Card Side Ports Input Voltage	−0.3	V_{CCB} + 0.3	V
T_{amb}	Operating Ambient Temperature	−40	85	°C

(1) V_{CCA} should be less than or equal to V_{CCB}.

Electrical Characteristics

All test conditions: V_{CCA} = 1.1 V to 1.95 V, V_{CCB} = 1.7 V to 3.6 V, T_A = −40°C to + 85°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
V_{en}	Device Enable Voltage Level, Automatic Enable Feature: V_{CCB}	V_{CCA} ≥ 1.0 V V_{CCB} Rising Edge	0.9	1.2	1..5	V
V_{dis}	Device Disable Voltage Level, Automatic Enable Feature: V_{CCB}	V_{CCA} ≥ 1.0 V V_{CCB} Falling Edge	0.65	1	1.3	V
V_{IH}	CMDA, DAT0A to DAT3A and CLKA, HIGH-level Input Voltage	1.1 V ≤ V_{CCA} ≤ 1.95 V	0.65 * V_{CCA}		V_{CCA} + 0.3	V
	CMDB and DAT0B to DAT3B, HIGH-level Input Voltage	1.7 V ≤ V_{CCB} ≤ 3.6V	0.625 * V_{CCB}		V_{CCB} + 0.3	V
V_{IL}	CMDA and DAT0A to DAT3A and CLKA, LOW-level Input Voltage	1.7 V ≤ V_{CCA} ≤ 1.95 V	−0.3		0.35 * V_{CCA}	V
	CMDB and DAT0B to DAT3B, LOW-level Input Voltage	2.7 V ≤ V_{CCB} ≤ 3.6 V	−0.3		0.3 * V_{CCB}	V
	CMDB and DAT0B to DAT3B, LOW-level Input Voltage	1.7 V ≤ V_{CCB} ≤ 1.95 V	−0.3		0.35 * V_{CCB}	V
V_{OH}	CMDA and DAT0A to DAT3A, HIGH-level Output Voltage	IO = −2 μA VI = VIH (card side) 1.1 V ≤ V_{CCA} ≤ 1.95 V	0.75 * V_{CCA}			V
	CLKFB, HIGH-level Output Voltage	IO = −2 mA VI = VIH (card side) 1.1 V ≤ V_{CCA} ≤ 1.95 V	0.8 * V_{CCA}			V
	CLKB, HIGH-level Output Voltage	V_{CCB} = 1.7 V IO = −2 mA VI = VIH (host side)	0.75 * V_{CCB}			V
	CLKB, HIGH-level Output Voltage	V_{CCB} = 2.7 V IO = −4 mA VI = VIH (host side)	0.85 * V_{CCB}			V
	CMDB, DAT0B to DAT3B and CLKB, HIGH-level output voltage	V_{CCB} = 1.7 V IO = −2 uA VI = VIH (host side)	0.85 * V_{CCA}			V
V_{OL}	CMDA and DAT0A to DAT3A, LOW-level Output Voltage	IO = 2 mA VI = VIL (card side) 1.1 V ≤ V_{CCA} ≤ 1.95 V			0.15 * V_{CCA}	V
	CLKFB, LOW-level Output Voltage	IO = 2 mA VI = VIL (host side) 1.1 V ≤ V_{CCA} ≤ 1.95 V			0.15 * V_{CCA}	V
	CMDB, DAT0B to DAT3B and CLKB, LOW-level Output Voltage	IO = 2 mA VI = VIL (host side) V_{CCB}= 1.7 V			0.125 * V_{CCA}	V

Parameter		Conditions	Min	Typ	Max	Unit
	CMDB, DAT0B to DAT3B and CLKB, LOW-level Output Voltage	IO = 4 mA VI = VIL (host side) V_{CCB} = 2.7 V			0.125 * V_{CCB}	V
I_I	Input Leakage Current, CMDA, DAT0A to DAT3A and CLKA	V_{CCA} = 1.95 V VI = 0 V to 1.95 V			1	μA
I_{CC}	Supply Current, Host side	All inputs = HIGH VI = V_{CCA} V_{CCA} = 1.95 V, V_{CCB} = 3.6 V			50	μA
	Supply Current, Card side	All inputs = HIGH VI = V_{CCB} V_{CCA}= 1.7 V, V_{CCB} = 1.7 V			7	μA
		All inputs = HIGH VI = V_{CCB} V_{CCA} = 1.95 V, V_{CCB} = 3.6 V			20	μA
C_{IO}(1)	Input/output Capacitance , Host Side	V_I = 0 V f_I = 10 MHz V_{CCA} = 1.8 V		5		pF
	Input/output Capacitance , Card Side	V_I = 0 V f_I = 10 MHz V_{CCA} = 1.8 V		12		pF
R_{PU}(1)	Pull-up Resistance			70		kΩ
R_S(1)	Series Resistance	Host side, R1		22.5		Ω
		Card side, R2		15		Ω

(1) Test data based on bench tests and design simulation.

AC Timing Requirements

All test conditions: V_{CCA} = 1.1 V to 1.95 V, V_{CCB} = 1.7 V to 3.6 V, T_A = −40°C to + 85°C, the data is based on bench test and design simulation, unless otherwise noted.

Parameter		Condition	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
t_{pd}	Propagation Delay	Card-side to host-side	1.2V	1.8 V		3.1	5.4	ns
			1.2 V	3.3 V		2.2	4	ns
			1.8 V	1.8 V		2.7	4.8	ns
			1.8 V	3.3 V		1.7	3.1	ns
		Host-side to card-side	1.2V	1.8 V		2.7	4.6	ns
			1.2 V	3.3 V		1.7	3	ns
			1.8 V	1.8 V		2.7	4.6	ns
			1.8 V	3.3 V		1.6	2.7	ns
		CLKA to CLKFB	1.2V	1.8 V		5.8	10	ns
			1.2 V	3.3 V		3.9	7	ns
			1.8 V	1.8 V		5.4	9.4	ns
			1.8 V	3.3 V		3.3	5.8	ns
t_r	Card-side Input Rise Time	Input rise time between 0.58 V and 1.27 V		1.8 V		0.5	0.96	ns
	Host-side Input Rise Time	Input rise time between VX = 0.35*V_{CCA} and VY = 0.65*V_{CCA}	1.2 V to 1.8 V			0.4	1	ns
t_f	Card-side Input Fall Time	Input fall time between 0.58 V and 1.27 V		1.8 V		0.45	0.96	ns
	Host-side Input Fall Time	Input fall time between VX = 0.35*V_{CCA} and VY = 0.65*V_{CCA}	1.2 V to 1.8 V			0.4	1	ns
t_t	Host-side Output Transition Time	Output transition time between VX = 0.35 *V_{CCA} and VY = 0.65*V_{CCA}	1.2 V to 1.8 V			0.3	1	ns
	Card-side Output Transition Time	Output transition time between VX = 0.45 V and VY = 1.4 V		1.8 V	0.4	0.88	1.32	ns
$t_{SK(O)}$	Skew (time), output	Host-side to card-side	1.2V	1.8 V			200	ps
			1.2 V	3.3 V			200	ps
			1.8 V	1.8 V			200	ps
			1.8 V	3.3 V			200	ps
		Card-side to host-side	1.2V	1.8 V			200	ps
			1.2 V	3.3 V			200	ps
			1.8 V	1.8 V			200	ps

Parameter		Condition	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
			1.8 V	3.3 V			200	ps

Parameter Measurement Waveforms

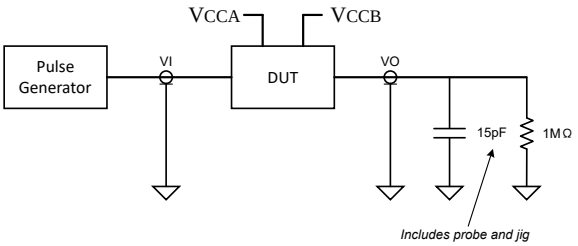


Figure 1. Load Circuitry for Measuring Switching Time, Data Rate, Pulse Duration, Propagation Delay, Output Rise and Fall Time

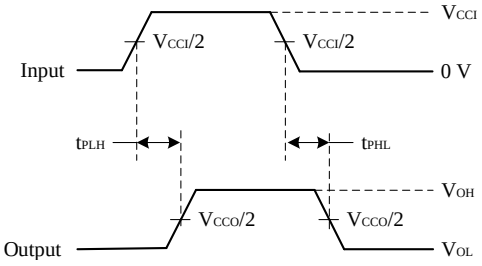


Figure 2. Output Delay Timing

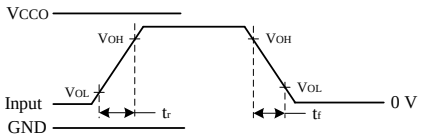


Figure 3. Output Rise and Fall Time

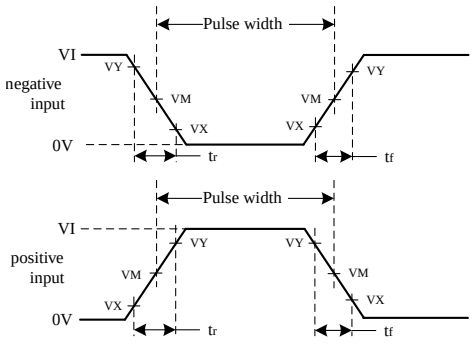


Figure 4. Output and Input Time

Detailed Description

Overview

The bidirectional level translator shifts the data between the I/O supply levels of the host and the memory card. Auto direction sensing circuitry determines if a command and data signals are transferred from the memory card to the host (card read mode) or from the host to the memory card (card write mode). The voltage translator has to support several clock and data transfer rates at the signaling levels specified in the SD 3.0 standard specification.

Functional Block Diagram

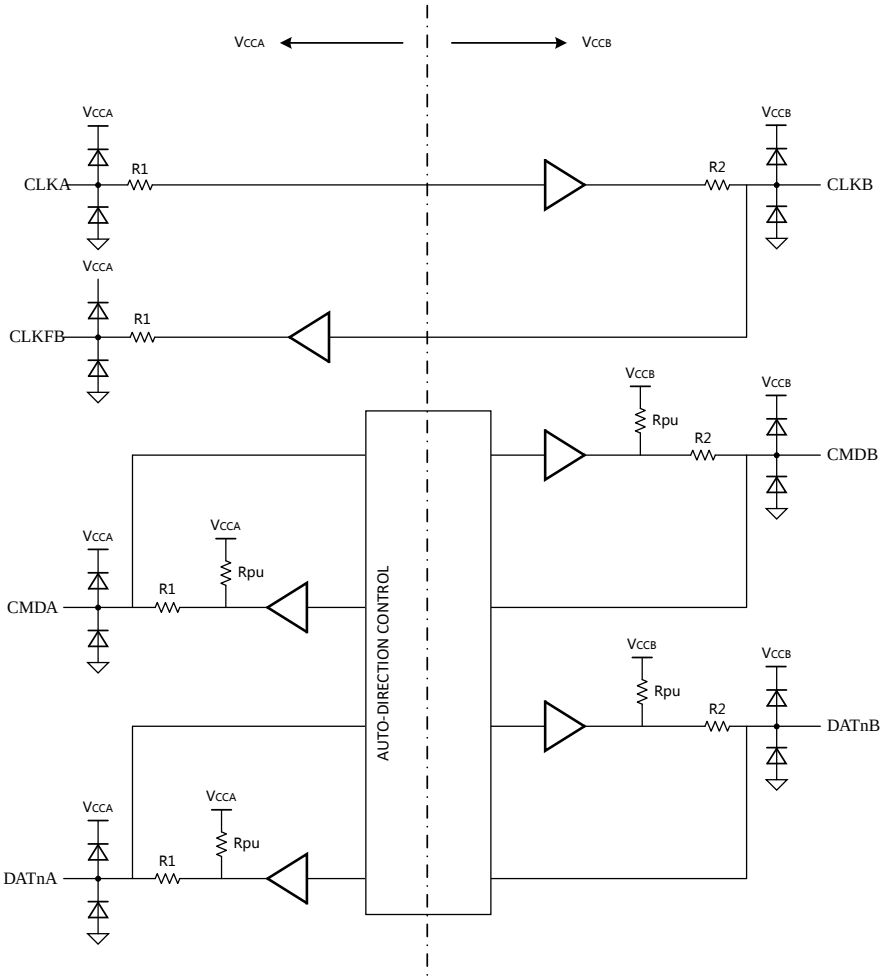


Figure 5. Functional Block Diagram

Feature Description

Enable and Direction Control

The device contains an auto-enable feature. If V_{CCB} rises above 1.5 V, the level translator logic is enabled automatically. As soon as V_{CCB} drops below 0.65 V, the memory card side drivers and the level translator logic are disabled. All pins on the host side, excluding CLKA are configured as inputs with a 70 kΩ resistor pulled up to V_{CCA}.

The device features an auto direction control for all data channels except CLK. For these pins the direction of data flow is sensed by the direction control logic and the output drivers are controlled accordingly. There is no need for the host interface to indicate the direction of data flow.

Feedback Clock Channel

The clock is transmitted from the host to the memory card side. The voltage translator and the Printed-Circuit Board (PCB) tracks introduce some amount of delay. It reduces timing margin for data read back from memory card, especially at higher data rates. Therefore, a feedback path is provided to compensate the delay. The reasoning behind this approach is the fact that the clock is always delivered by the host, while the data in the timing critical read mode comes from the card.

Pin and Channel Naming

The sequence of the channels is chosen to easily connect to SD-card connectors. As the internal design of channels DAT0 (pins DAT0A and DAT0B), DAT1 (pins DAT1A and DAT1B), DAT2 (pins DAT2A and DAT2B), DAT3 (pins DAT3A and DAT3B) and CMD (pins CMDA and CMDB) is identical, these channels can be exchanged. Swapping channels in the above mentioned group can help ease PCB layout issues. E.g. DAT0 can be swapped with DAT1 or DAT3 with CMD without impact on functionality of TPXT0506.

Supported modes

Bus Speed Mode	Signal Level (V)	Clock Rate (MHz)	Data Rate (MB/s)
Default-Speed	3.3	25	12.5
High-Speed	3.3	50	25
SDR12	1.8	25	12
SDR25	1.8	50	23
SDR50	1.8	100	50
SDR104	1.8	208	104
DDR50	1.8	50	50

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPXT0506 is an SD 3.0-compatible bidirectional dual supply level translator with auto-direction control. It is designed to interface between a memory card operating at 1.7 V to 3.6 V signal levels and a host with a nominal supply voltage of 1.1 V to 1.95 V. The device supports SD 3.0: SDR104, SDR50, DDR50, SDR25, SDR12 and SD 2.0 High-Speed (50 MHz) and Default-Speed (25 MHz) modes.

- Smartphone
- SD, MMC or microSD card readers
- Laptop computers
- Tablet PCs
- Digital cameras
- Mobile handsets

Typical Application

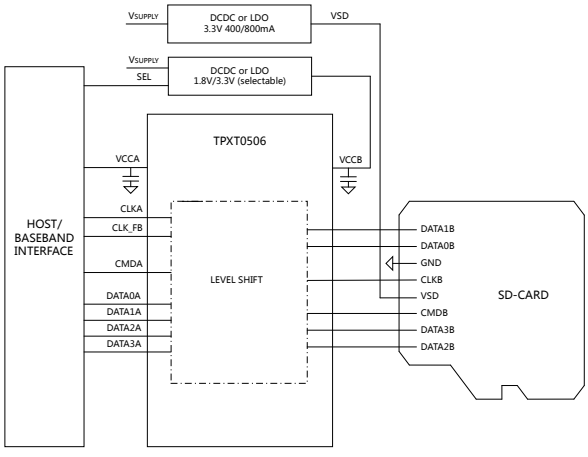


Figure 6. Typical Application Circuit

Layout

Layout Example

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they have to turn corners. The following shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

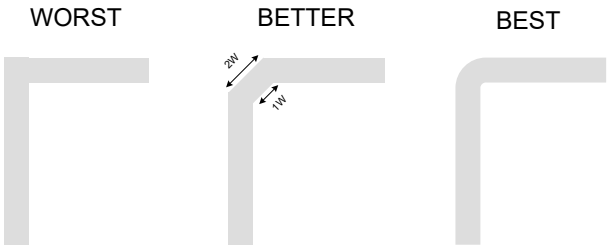


Figure 7. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

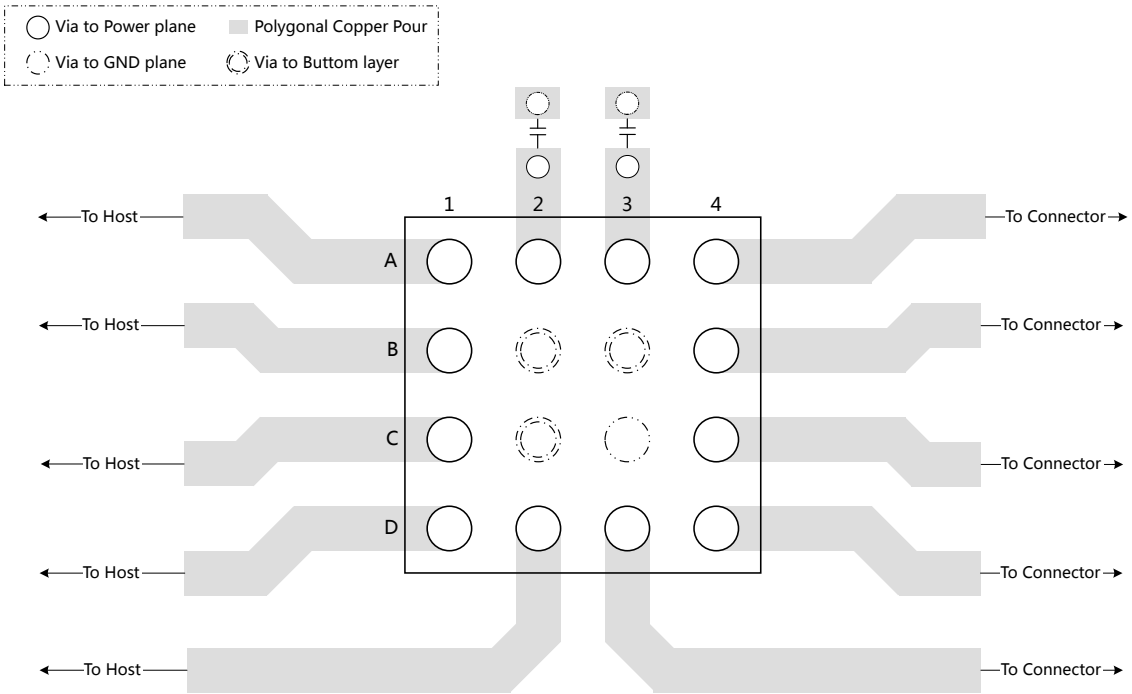


Figure 8. TPXT0506 Example Layout (Top Layer)

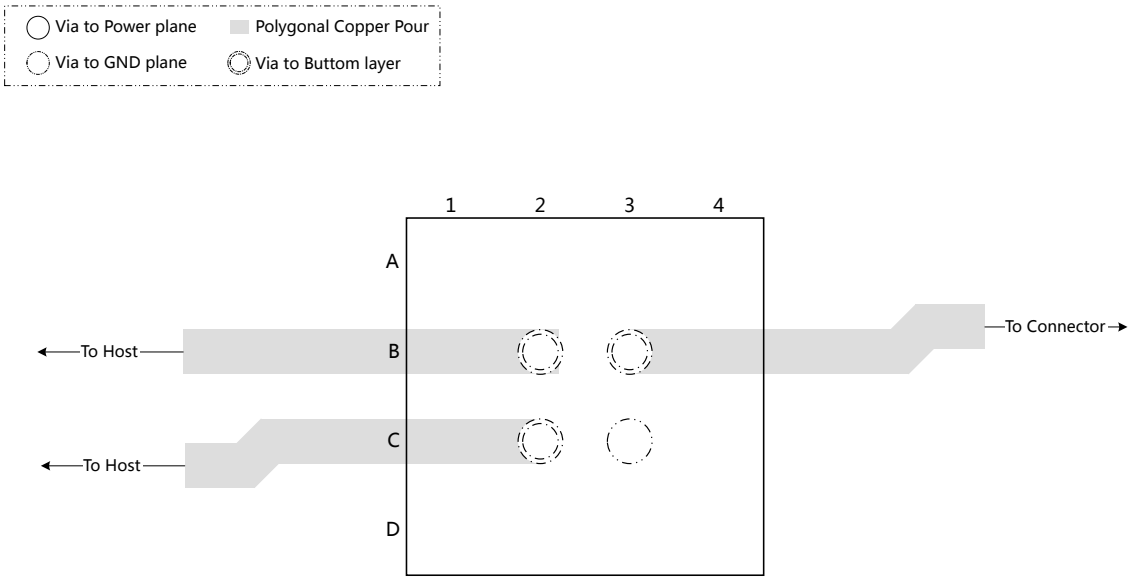
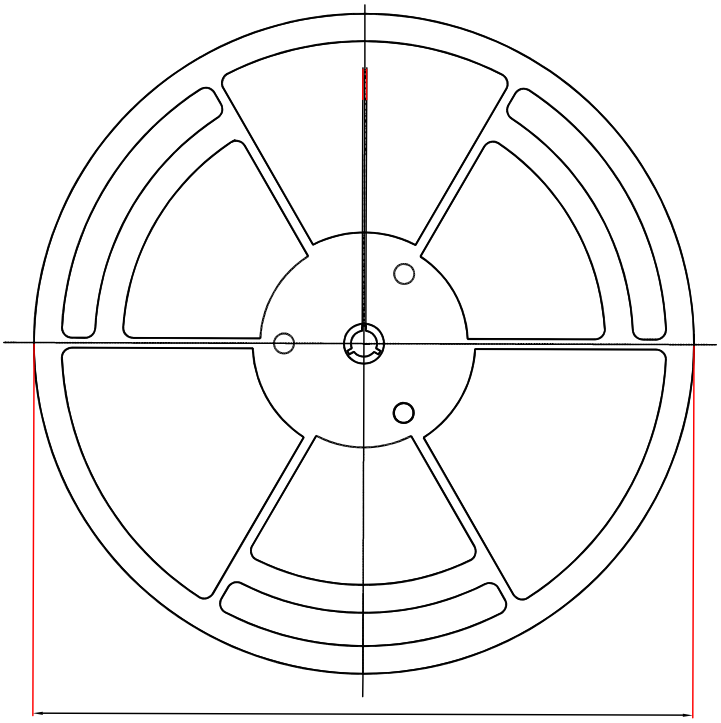
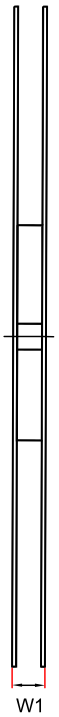
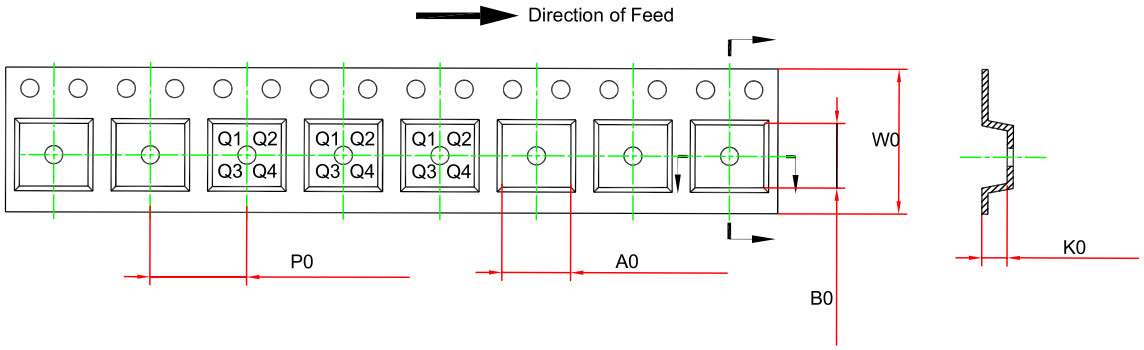


Figure 9. TPXT0506 Example Layout (Buttom Layer)

Tape and Reel Information





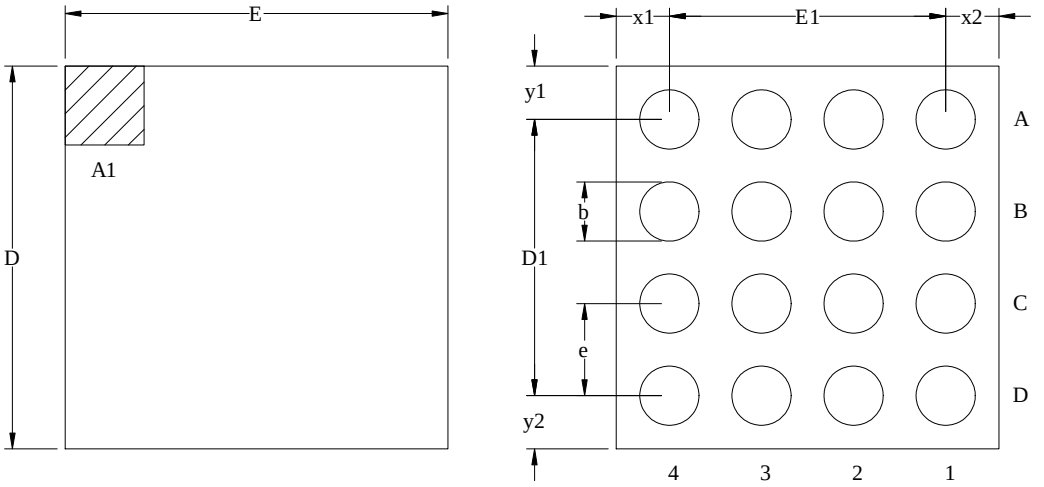


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPXT0506-WLPR	WLCSP-16	178.0	1.75	0.75	8.0	12.5	2.3	4.0	Q1

Package Outline Dimensions

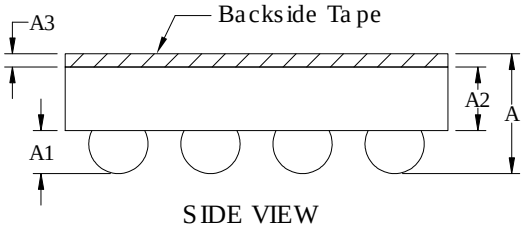
WLCSP-16

Package Outline Dimensions WLP(WLCSP-A)



TOP VIEW
(MARK SIDE)

BOTTOM VIEW
(BALL SIDE)



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.3925	0.4675	0.015	0.018
A1	0.136	0.176	0.005	0.007
A2	0.2365	0.2615	0.009	0.010
A3	0.020	0.030	0.001	0.001
D	1.420	1.470	0.056	0.058
D1	1.050BSC		0.041BSC	
E	1.420	1.470	0.056	0.058
E1	1.050BSC		0.041BSC	
b	0.194	0.234	0.008	0.009
e	0.350BSC		0.014BSC	
x1	0.1975REF		0.008REF	
x2	0.1975REF		0.008REF	
y1	0.1975REF		0.008REF	
y2	0.1975REF		0.008REF	

NOTES:
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPXT0506-WLPR	−40 to 85°C	WLCSP-16	506	MSL1	Tape and Reel,3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

Disclaimer. 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.