24V General Purpose Analog Switch

Features

- Supply Voltage Range: 4.5 V to 24 V
- Dual Supply Range: up to ±12 V
- Low ON-State Resistance: Typical 55 Ω at V_S = 24 V
- Bandwidth: 500 MHz
- Bidirectional Signal Path
- Rail-to-Rail Operation
- 1.8-V Logic Compatible
- Fast Switching Times:
  t_{ON} = 30 ns
  t_{OFF} = 100 ns
- Break-Before-Making Switching
- Operation Temperature Range: –40°C to 125°C

Applications

- Industry Control Systems
- Battery-powered Systems
- Audio Signal Routing
- Instrumentation

Description

The TPWH4051 is a single-pole octal-throw, 1-channel analog switch (SP8T) suitable for use in analog or digital 8:1 multiplexer/demultiplexer applications. The TPWH4052 is a single-pole quadrillion-throw, two-channel analog switch (SP4T) suitable for use in analog or digital 4:1 multiplexer/demultiplexer applications. The TPWH4053 is a single-pole binary-throw, three-channel analog switch (SP2T) suitable for use in analog or digital 2:1 multiplexer/demultiplexer applications. The switches support bidirectional analog signals on the source (S_X) and drain (D_X) pins ranging from V_{EE} to V_{CC}. The switches feature a digital enable input ($\overline{EN}$). When $\overline{EN}$ is HIGH, the switches are turned off. The switches are designed on an enhanced process that provides lower power dissipation yet gives high switching speeds. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels.

Table of Contents

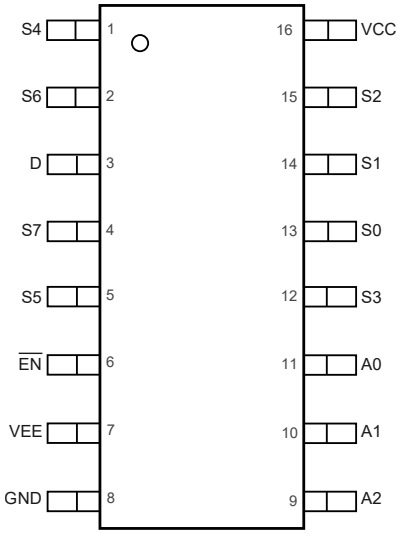
Revision History

Date	Revision	Notes
2025-07-08	Rev.A.0	Initial Version.

Pin Configuration and Functions

TPWH4051 Pin Configuration and Function Table

TPWH4051
SOP16
Top View



TPWH4051
TSSOP16
Top View

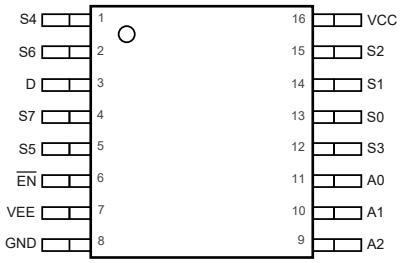


Table 1. Pin Functions: TPWH4051

Pin No.	Name	I/O	Description
1	S4	I/O	Channel 4 input or output.
2	S6	I/O	Channel 6 input or output.
3	D	I/O	Common input or output.
4	S7	I/O	Channel 7 input or output.
5	S5	I/O	Channel 5 input or output.
6	$\overline{EN}$	I	Enable switches, active low.
7	VEE		Negative Power Input.
8	GND		Ground (0 V) reference.
9	A2	I	Control Input.
10	A1	I	Control Input.
11	A0	I	Control Input.
12	S3	I/O	Channel 3 input or output.
13	S0	I/O	Channel 0 input or output.
41	S1	I/O	Channel 1 input or output.
15	S2	I/O	Channel 2 input or output.
16	VCC		Positive Power Input.

Table 2. Function Table: TPWH4051

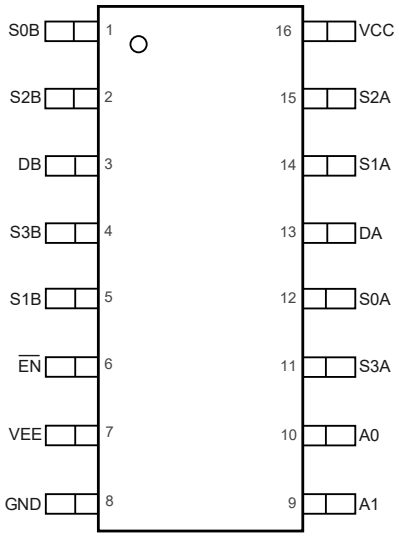
$\overline{EN}$	A2	A1	A0	Selected Signal Path Connected to Drain (D) Pin
0	0	0	0	S0
0	0	0	1	S1
0	0	1	0	S2
0	0	1	1	S3
0	1	0	0	S4
0	1	0	1	S5
0	1	1	0	S6
0	1	1	1	S7
1	X (1)	X (1)	X (1)	All inputs are unselected (HI-Z)

(1) X denotes do not care.

(2) The Enable pin, $\overline{EN}$, of the TPWH4051 has a weak internal pull-up resistor to put the devices into a disabled state upon power up. The Address pins (Ax) have weak internal pull-down resistors to put the switch into a defined logic state.

TPWH4052 Pin Configuration and Function Table

TPWH4052
SOP16
Top View



TPWH4052
TSSOP16
Top View

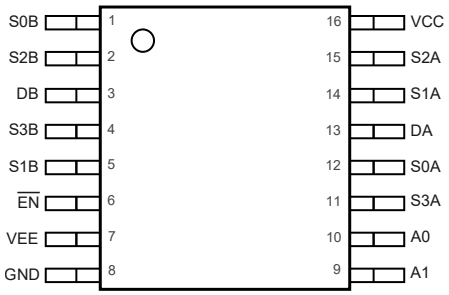


Table 3. Pin Functions: TPWH4052

Pin No.	Name	I/O	Description
1	S0B	I/O	Channel 0 input or output of mux B.
2	S2B	I/O	Channel 2 input or output of mux B.
3	DB	I/O	Common input or output of mux B.
4	S3B	I/O	Channel 3 input or output of mux B.
5	S1B	I/O	Channel 1 input or output of mux B.
6	$\overline{EN}$	I	Enable switches, active low.
7	VEE		Negative Power Input.
8	GND		Ground (0 V) reference.
9	A1	I	Control Input.
10	A0	I	Control Input.
11	S3A	I/O	Channel 3 input or output of mux A.
12	S0A	I/O	Channel 0 input or output of mux A.
13	DA	I/O	Common input or output of mux A.
41	S1A	I/O	Channel 1 input or output of mux A.
15	S2A	I/O	Channel 2 input or output of mux A.
16	VCC		Positive Power Input.

Table 4. Function Table: TPWH4052

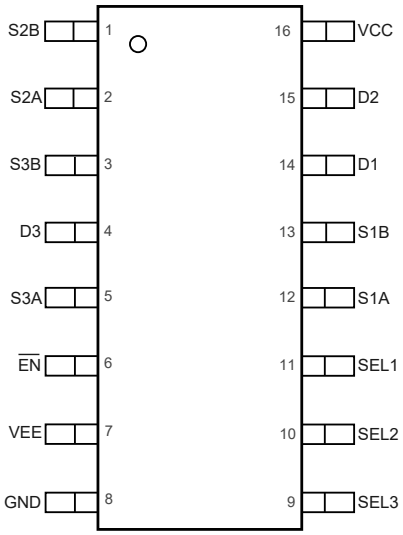
$\overline{EN}$	A1	A0	Selected Signal Path Connected to Drain (D) Pin
0	0	0	S0A to DA S0B to DB
0	0	1	S1A to DA S1B to DB
0	1	0	S2A to DA S2B to DB
0	1	1	S3A to DA S3B to DB
1	X (1)	X (1)	All inputs are unselected (HI-Z)

(1) X denotes do not care.

(2) The Enable pin, $\overline{EN}$, of the TPWH4052 has a weak internal pull-up resistor to put the devices into a disabled state upon power up. The Address pins (Ax) have weak internal pull-down resistors to put the switch into a defined logic state.

TPWH4053 Pin Configuration and Function Table

TPWH4053
SOP16
Top View



TPWH4053
TSSOP16
Top View

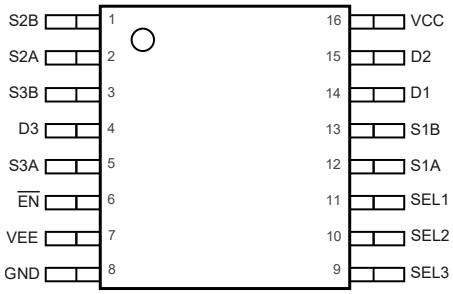


Table 5. Pin Functions: TPWH4053

Pin No.	Name	I/O	Description
1	S2B	I/O	Channel B input or output of mux 2.
2	S2A	I/O	Channel A input or output of mux 2.
3	S3B	I/O	Channel B input or output of mux 3.
4	D3	I/O	Common input or output of mux 3.
5	S3A	I/O	Channel A input or output of mux 3.
6	$\overline{EN}$	I	Enable switches, active low.
7	VEE		Negative Power Input.
8	GND		Ground (0 V) reference.
9	SEL3	I	Control Input.
10	SEL2	I	Control Input.
11	SEL1	I	Control Input.
12	S1A	I/O	Channel A input or output of mux 1.
13	S1B	I/O	Channel B input or output of mux 1.
41	D1	I/O	Common input or output of mux 1.
15	D2	I/O	Common input or output of mux 2.
16	VCC		Positive Power Input.

Table 6. Function Table: TPWH4053

$\overline{EN}$	SEL1	SEL2	SEL3	Selected Signal Path Connected to Drain (D) Pin
0	0	X	X	S1A to D1
0	1	X	X	S1B to D1
0	X	0	X	S2A to D2
0	X	1	X	S2B to D2
0	X	X	0	S3A to D3
0	X	X	1	S3B to D3
1	X (1)	X (1)	X (1)	All inputs are unselected (HI-Z)

(1) X denotes do not care.

(2) The Enable pin, $\overline{EN}$, of the TPWH4053 has a weak internal pull-up resistor to put the devices into a disabled state upon power up. The SEL pins (SELx) have weak internal pull-down resistors to put the switch into a defined logic state.

Specifications

Absolute Maximum Ratings (1)(3)

Parameter		Min	Max	Unit
V_{CC} - V_{EE}	Supply Voltage	–0.5	28	V
V_{CC} - GND		–0.5	28	V
V_{EE} - GND		–28	0.5	V
V_{AX} or $V_{\overline{EN}}$	Logic Control Input Voltage ($\overline{EN}$, A_X)	GND	V_{CC} + 0.5	V
I_{SEL} or $I_{\overline{EN}}$	Logic Control Input Diode Current ($\overline{EN}$, A_X)	–30	+30	mA
V_S or V_D	Analog Switch Voltage (S_X, D)	V_{EE} - 0.5	V_{CC} + 0.5	V
I_S or $I_{D\ (CONT)}$	Analog Switch Current (S_X, D)	–25	25	mA
I_{IK}	Analog Switch Diode Current (2)	–30	30	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	–65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(3) To avoid drawing excess current from V_{CC}, or into V_{EE}, the voltage drop across the bidirectional switch path (ΔV_{switch}) must not exceed 1.2 V (600 mV for high temperature).

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions (1)

Parameter	Min	Max	Unit
Supply Voltage, V_{CC} - V_{EE}	4.5	24	V
Supply Voltage, V_{CC} - GND (2)	4.5	24	V
Supply Voltage, V_{EE} - GND (2)	–15	0	V
Select Input Voltage	0	V_{CC}	V
Input Transition Rise and Fall Rate		100	ns/V
Switch I/O Port Voltage	V_{EE}	V_{CC}	V
Ambient Temperature	–40	125	°C

(1) Input select must be held HIGH or LOW and it shouldn' t float.
(2) The voltage of V_{CC} and V_{EE} needs to be in the range of V_{CC} - V_{EE}.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP16	100	50	°C/W
TSSOP16	150	60	°C/W

Electrical Characteristics

All test conditions: over ambient temperature range, typical at T_A = 25℃, unless otherwise noted.

Symbol	Parameter	Conditions	V_{CC} (V)	V_{EE} (V)	GPN	Min	Typ	Max	Unit
Power Supply									
I_{CC}	Supply Current	$\overline{EN}$ = 0 V	5	0	All		23	40	μA
			10	0			24	46	μA
			24	0			26	50	μA
			5	–5			25	50	μA
			12	–12			27	55	μA
I_{EE}	Negative Supply Current	$\overline{EN}$ = 0 V	5	–5	TPWH4051		11	25	μA
			12	–12			12	25	μA
			5	–5	TPWH4052		15	27	μA
			12	–12			16	27	μA
			5	–5	TPWH4053 (2)		18	29	μA
			12	–12			19	29	μA
I_{CC} disable		$\overline{EN}$ = 5 V or V_{CC}	All		All		12	25	μA
Logic Input (A2, A1, A0, $\overline{EN}$)									
V_{IH}	Input Voltage High		All		All	1.4		V_{CC}	V
V_{IL}	Input Voltage Low		All		All	0		0.8	V
I_{IH}, I_{IL}	Logic Input Current	V_{Logic} = 0 V, 5 V or V_{CC}	All		All	–1.5	±0.6	1.5	μA
C_{IN}			All		All		2		pF
Analog Switch									
R_{ON}	On Resisitance	V_S = V_{EE} to V_{CC}, I_D = −1 mA, Figure 9	5	0	All		65	210	Ω
			10	0			55	210	Ω
			24	0			55	210	Ω
			5	–5			60	210	Ω
			12	–12			55	210	Ω
ΔR_{ON}	On Resistance Match Between Channels	V_S = V_{EE} to V_{CC}, I_D = −1 mA	All		All		2		Ω
$R_{FLAT(ON)}$	On Resistance Flatness	V_S = V_{EE} to V_{CC}, I_D = −1 mA	All		All		56	120	Ω
I_S(Off) I_D(Off)	Source/Drain Off Leakage	Switch state is off, V_S = V_{EE}, V_{CC}, V_D = V_{CC}, V_{EE}, Figure 10	24	0	All	–1000	±0.5	1000	nA

Symbol	Parameter	Conditions	V_{CC} (V)	V_{EE} (V)	GPN	Min	Typ	Max	Unit
I_{ON}	Channel On Leakage	Switch state is on, V_S = V_D = V_{EE} or V_{CC}, Figure 11	24	0	All	–1000	±0.5	1000	nA

AC Performance Characteristics

All test conditions: over ambient temperature range, typical at T_A = 25℃, unless otherwise noted.

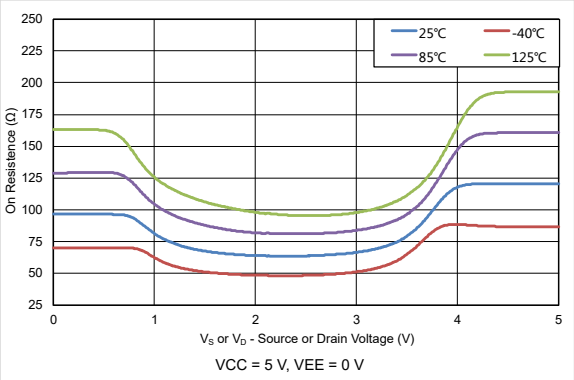
Symbol	Parameter	Conditions	V_{CC} (V)	V_{EE} (V)	GPN	Min	Typ	Max	Unit
Capacitance									
C_S(Off)	Source Off Capacitance	V_S = (V_{CC} + V_{EE}) / 2, f = 1 MHz	5	–5	All		2		pF
			24	0			2		pF
C_D(Off)	Drain Off Capacitance	V_S = (V_{CC} + V_{EE}) / 2, f = 1 MHz	5	–5	TPWH4051		7		pF
			24	0			7		pF
			5	–5	TPWH4052 (2)		6		pF
			24	0			5		pF
			5	–5	TPWH4053 (2)		4		pF
			24	0			3		pF
C_S(On) C_D(On)	Switch On Capacitance	V_S = (V_{CC} + V_{EE}) / 2, f = 1 MHz	5	–5	TPWH4051		9		pF
			24	0			9		pF
			5	–5	TPWH4052 (2)		8		pF
			24	0			7		pF
			5	–5	TPWH4053 (2)		6		pF
			24	0			5		pF
Dynamic Characteristics									
BW (Sine Wave Input)	Bandwidth	V_{BIAS} = (V_{CC} + V_{EE}) / 2 (1), V_S = 200 mV_{PP}, R_L = 50 Ω, C_L = 5 pF, Figure 19	5	–5	TPWH4051		500		MHz
			12	–12			600		MHz
			5	–5	TPWH4052		600		MHz
			12	–12			700		MHz
			5	–5	TPWH4053 (2)		550		MHz
			12	–12			590		MHz
OISO (Sine Wave Input)	Off Isolation (Channel Off)	V_{BIAS} = (V_{CC} + V_{EE}) / 2 (1), V_S = 200 mV_{PP}, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, Figure 17	5	–5	All		–95		dB
			12	–12			–95		dB
XTALK (Sine Wave Input)	Crosstalk	V_{BIAS} = (V_{CC} + V_{EE}) / 2 (1), V_S = 200 mV_{PP}, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, Figure 18	5	–5	All		–90		dB
			12	–12			–90		dB
QINJ	Charge Injection	V_S = (V_{CC} + V_{EE}) / 2, R_S = 0 Ω, C_L = 100 pF, Figure 16	5	–5	All		3		pC
			24	0			4		pC
t_{PD}	Signal Input to Signal Output	V_S = V_{EE} to V_{CC}, C_L = 20 pF,	5	0	All		3	15	ns
			10	0			3	15	ns

Symbol	Parameter	Conditions	V_{CC} (V)	V_{EE} (V)	GPN	Min	Typ	Max	Unit
		R_L = 10 kΩ, T_A = 25℃, Figure 15	24	0			3	15	ns
			5	–5			3	15	ns
			12	–12			3	15	ns
t_{TRAN}	Address-to-Signal OUT Transition Time Between Inputs	t_r, t_f = 20 ns, C_L = 50 pF, R_L = 10 kΩ, Figure 14	5	0	All		130	200	ns
			10	0			120	170	ns
			24	0			120	170	ns
			5	–5			124	180	ns
			12	–12			110	170	ns
$t_{ON(\overline{EN})}$	Enable-to-Signal OUT Channel Turning ON	t_r, t_f = 20 ns, C_L = 50 pF, R_L = 10 kΩ, Figure 12	5	0	All		40	60	ns
			10	0			40	60	ns
			24	0			40	60	ns
			5	–5			30	50	ns
			12	–12			30	50	ns
$t_{OFF(\overline{EN})}$	Enable-to-Signal OUT Channel Turning OFF	t_r, t_f = 20 ns, C_L = 50 pF, R_L = 10 kΩ, Figure 12	5	0	All		103	126	ns
			10	0			100	116	ns
			24	0			100	121	ns
			5	–5			100	123	ns
			12	–12			100	120	ns
t_B	Break-Before-Make Time	C_L = 20 pF, R_L = 10 kΩ, Figure 13	5	0	All	1	78		ns
			10	0		1	58		ns
			24	0		1	58		ns
			5	–5		1	70		ns
			12	–12		1	52		ns

(1) Peak-to-Peak voltage symmetrical about (V_{CC} + V_{EE}) / 2.

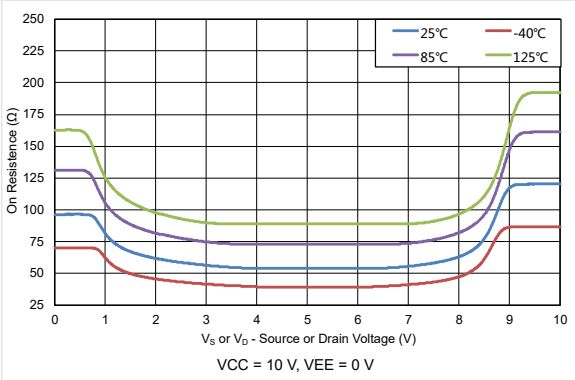
(2) Provided by design simulation.

Typical Performance Characteristics



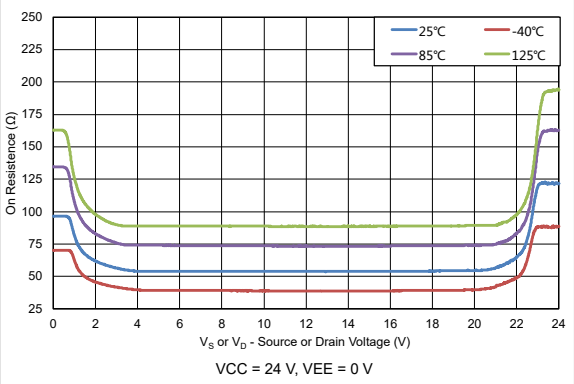
V_{CC} = 5 V, V_{EE} = 0 V

Figure 1. On-Resistance vs. Temperature



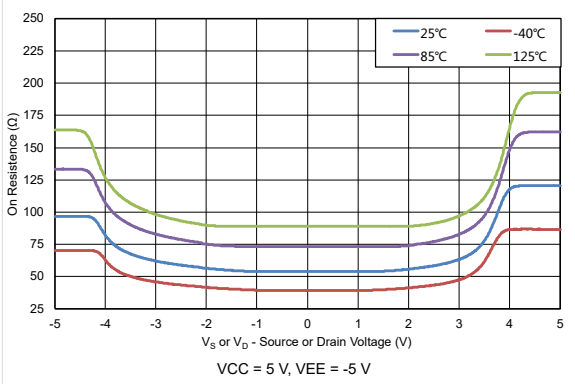
V_{CC} = 10 V, V_{EE} = 0 V

Figure 2. On-Resistance vs. Temperature,



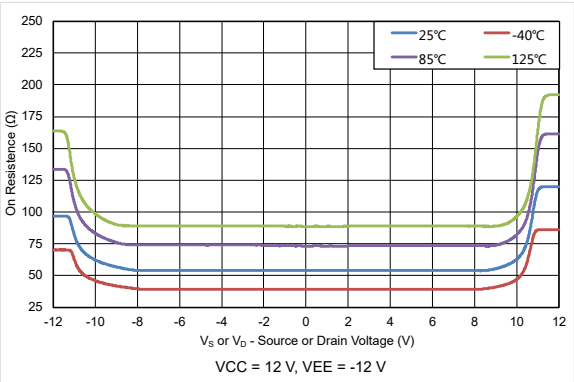
V_{CC} = 24 V, V_{EE} = 0 V

Figure 3. On-Resistance vs. Temperature



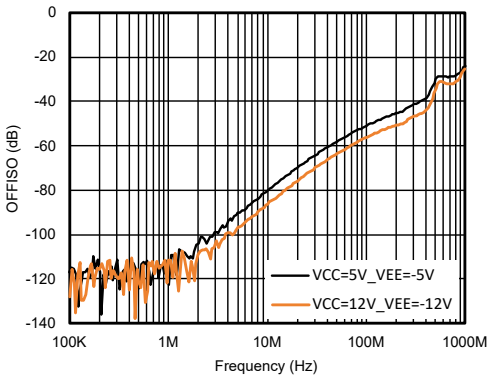
V_{CC} = 5 V, V_{EE} = -5 V

Figure 4. On-Resistance vs. Temperature



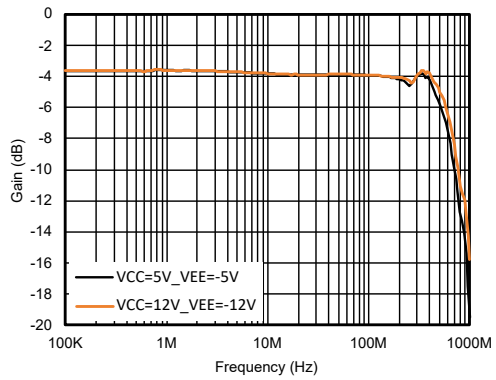
V_{CC} = 12 V, V_{EE} = -12 V

Figure 5. On-Resistance vs. Temperature



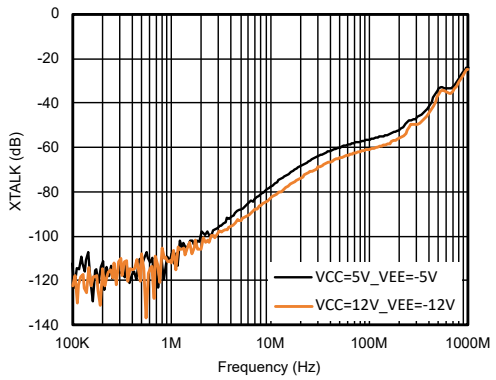
V_{CC} = 5 V / 12 V, V_{EE} = -5 V / -12 V

Figure 6. OFFISO



V_{CC} = 5 V / 12 V, V_{EE} = -5 V / -12 V

Figure 7. Bandwidth



V_{CC} = 5 V / 12 V, V_{EE} = -5 V / -12 V

Figure 8. Crosstalk

Test Circuit and Waveforms

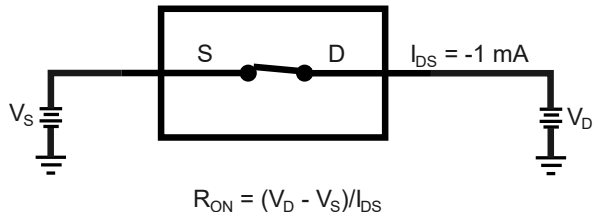


Figure 9. On Resistance

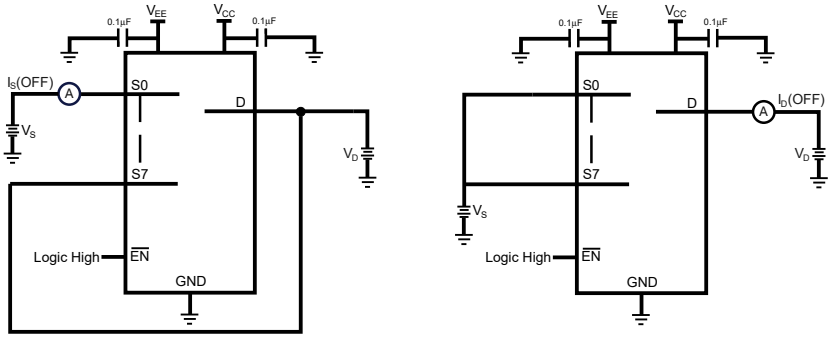


Figure 10. Off Leakage

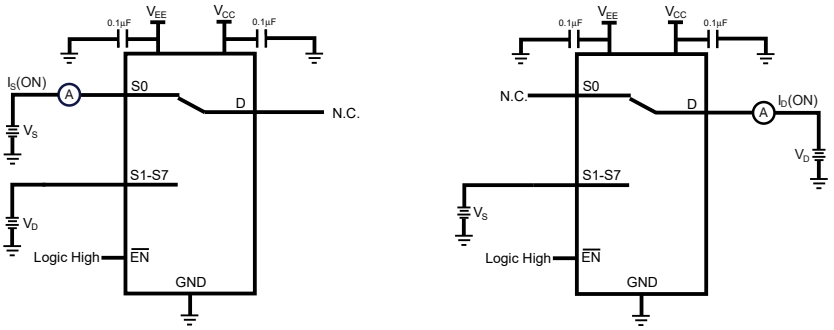


Figure 11. On Leakage

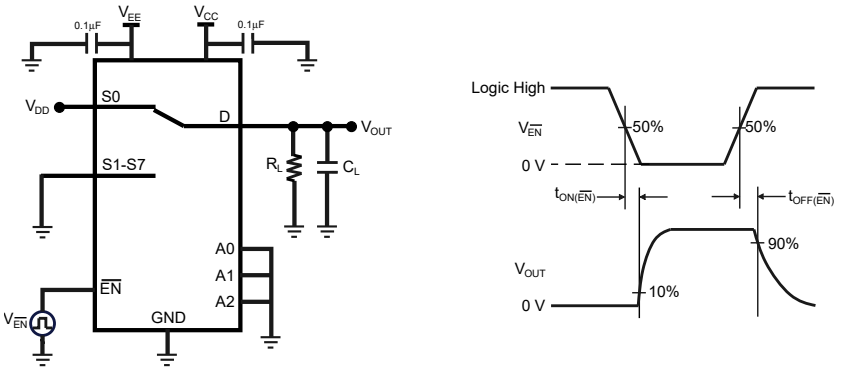


Figure 12. Turn-On and Turn-Off Time

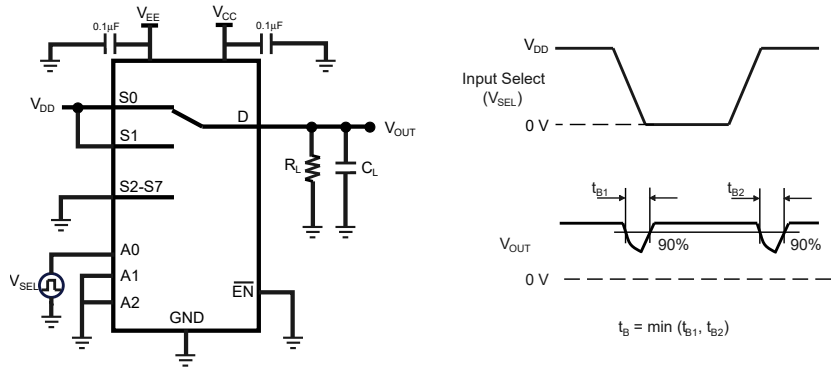


Figure 13. Switch Break Time

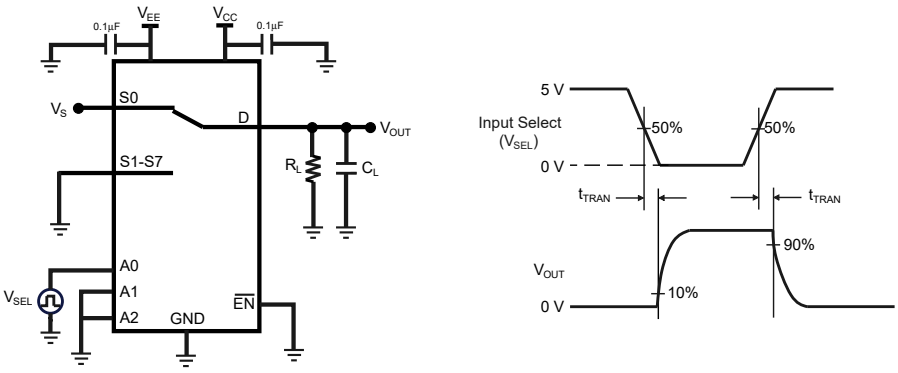


Figure 14. Transition Time

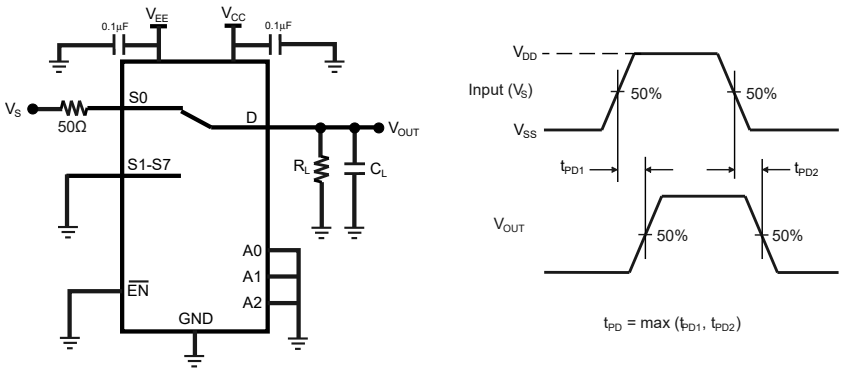


Figure 15. Propagation Delay

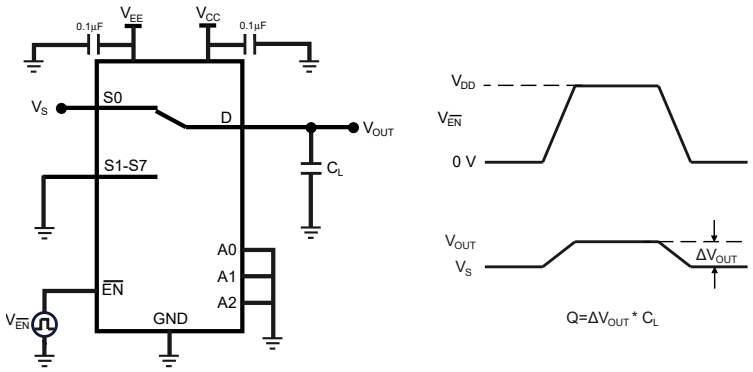


Figure 16. Charge Injection

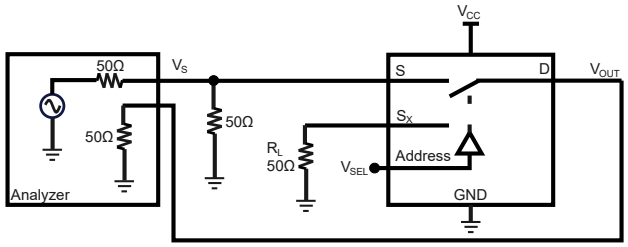


Figure 17. Off Isolation

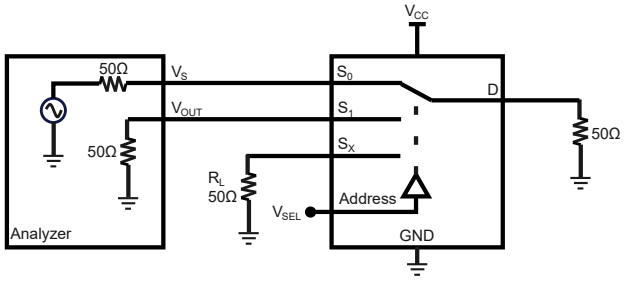


Figure 18. Crosstalk

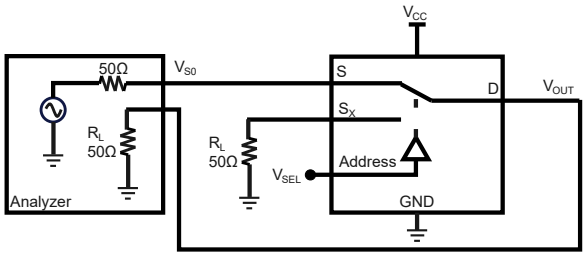


Figure 19. Bandwidth

Application and Implementation

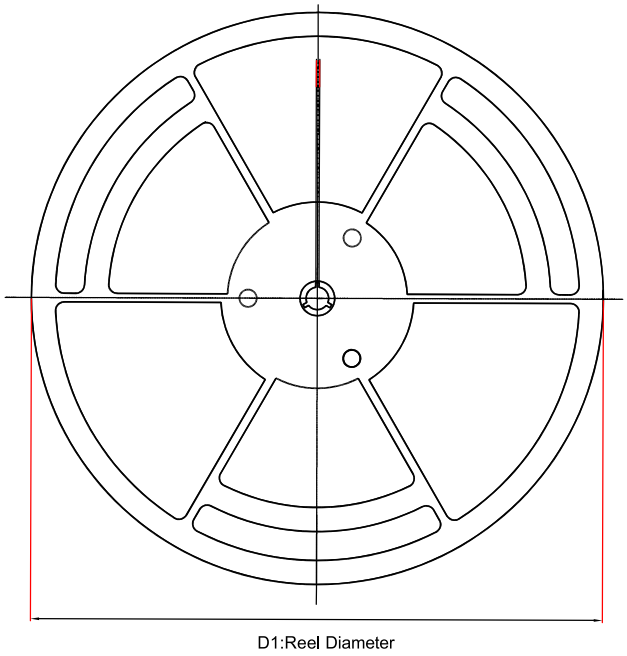
Note

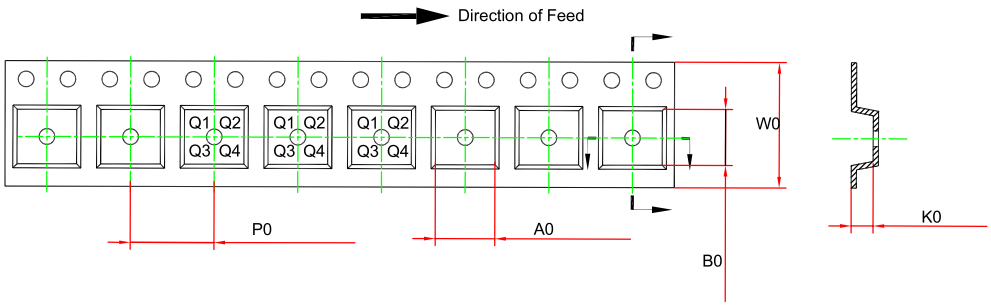
Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

A 0.1-μF bypass capacitor on V_{CC} and GND is recommended to prevent power disturbance, another 0.1-μF bypass capacitor on V_{EE} and GND is also recommended if the V_{EE} is not connected to GND.

Tape and Reel Information





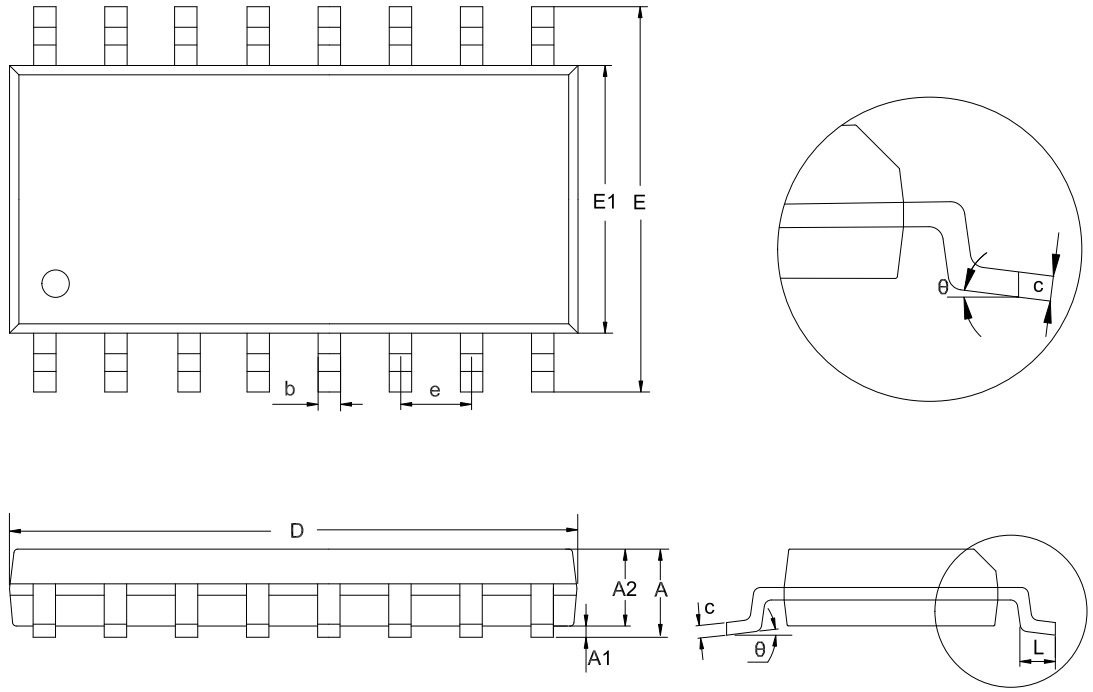
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) (1)	B0 (mm) (1)	K0 (mm) (1)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPWH4051-SO3R	SOP16	330	21.6	6.6	10.4	2.1	8	16	Q1
TPWH4051-TS3R	TSSOP16	330	17.6	6.8	5.5	1.5	8	12	Q1
TPWH4052-SO3R	SOP16	330	21.6	6.6	10.4	2.1	8	16	Q1
TPWH4052-TS3R	TSSOP16	330	17.6	6.8	5.5	1.5	8	12	Q1
TPWH4053-SO3R	SOP16	330	21.6	6.6	10.4	2.1	8	16	Q1
TPWH4053-TS3R	TSSOP16	330	17.6	6.8	5.5	1.5	8	12	Q1

(1) The value is for reference only. Contact the 3PEAK factory for more information.

Package Outline Dimensions

SOP16

Package Outline Dimensions SO3(SOP-16-A)



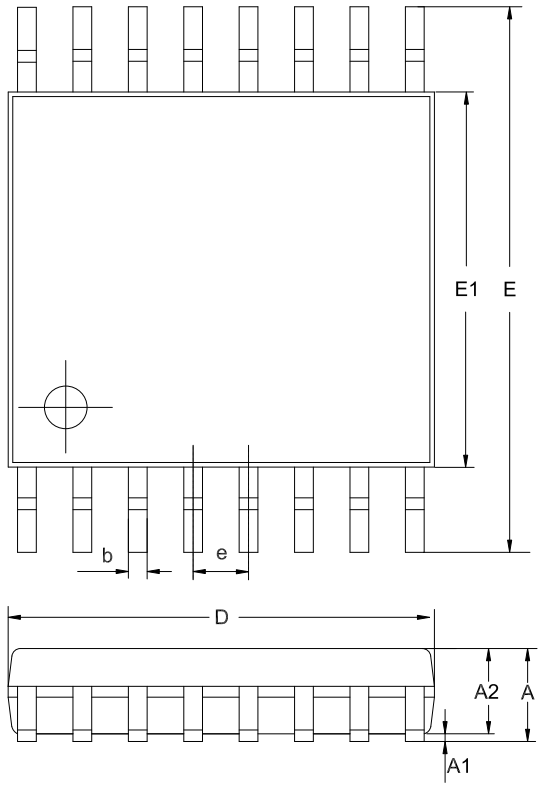
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.300	1.600	0.051	0.063
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.000	0.386	0.394
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

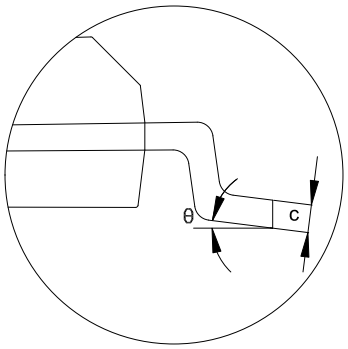
NOTES

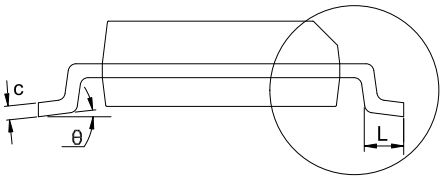
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

TSSOP16

Package Outline Dimensions TS3(TSSOP-16-A)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPWH4051-SO3R	−40 to 125°C	SOP16	WH4051	MSL3	Tape and Reel,2500	Green
TPWH4051-TS3R	−40 to 125°C	TSSOP16	WH4051	MSL3	Tape and Reel,3000	Green
TPWH4052-SO3R (1)	−40 to 125°C	SOP16	WH4052	MSL3	Tape and Reel,2500	Green
TPWH4052-TS3R (1)	−40 to 125°C	TSSOP16	WH4052	MSL3	Tape and Reel,3000	Green
TPWH4053-SO3R (1)	−40 to 125°C	SOP16	WH4053	MSL3	Tape and Reel,2500	Green
TPWH4053-TS3R (1)	−40 to 125°C	TSSOP16	WH4053	MSL3	Tape and Reel,3000	Green

(1) For future products, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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