

Features

- Supply Voltage: 4.5 V to 40 V
- Dual Supply Voltage: Up to ± 20 V
- Low Leakage: Maximum 1.3 nA at -40°C to 85°C
- Low ON-State Resistance: Typical $4\ \Omega$ at ± 15 V
- Low On-State Resistance Flatness
- -3 dB Bandwidth: 500 MHz at ± 15 V
- 1.8-V Logic Compatible
- Rail-to-Rail Operation
- Break-Before-Making Switching
- Operation Temperature Range: -40°C to 125°C

Applications

- Industry Control Systems
- Battery-Powered Systems
- Audio Signal Routing
- Portable Instruments and Mobile Devices

Description

The TPW6414R is a monolithic CMOS SPST switch. This switch comprises four single-pole single-throw (SPST) analog switches controlled by four digital logic independently. The TPW6414R features low on resistance, low resistance flatness, and low leakage current. The TPW6414R can operate from a single-supply range of 4.5 V to 40 V.

The TPW6414R is available in the SOP16/TSSOP16 package, and is characterized from -40°C to $+125^{\circ}\text{C}$.

Functional Block Diagram

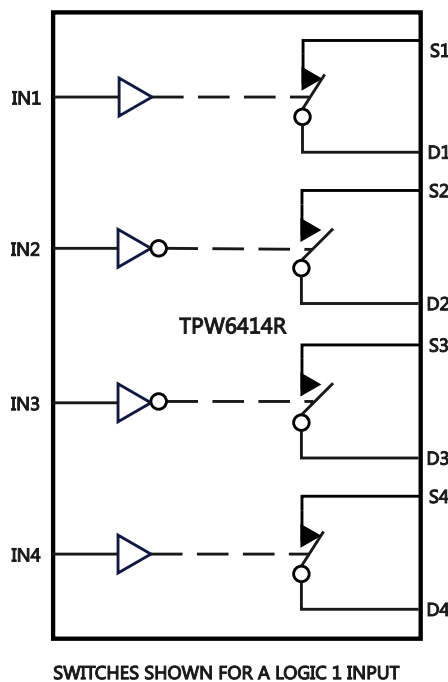


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Revision History

Date	Revision	Notes
2026-04-08	Rev.A.0	Initial Version.

Pin Configuration and Functions

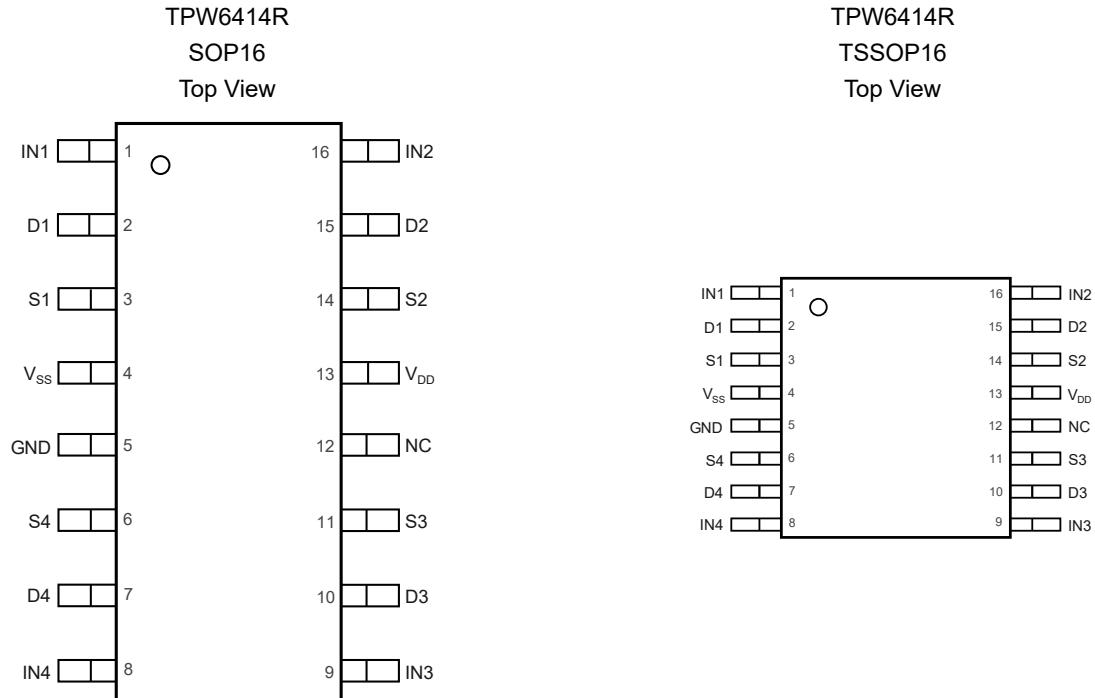


Table 1. Pin Functions

Pin No.	Name	I/O	Description
1	IN1	I	Logic control input 1.
2	D1	I/O	Drain pin 1. Can be used as input or output.
3	S1	I/O	Source pin 1. Can be used as input or output.
4	V _{SS}		Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{SS} and GND. V _{SS} must be connected to ground for single supply voltage applications.
5	GND		Ground (0 V) reference pin.
6	S4	I/O	Source pin 4. Can be used as input or output.
7	D4	I/O	Drain pin 4. Can be used as input or output.
8	IN4	I	Logic control input 4.
9	IN3	I	Logic control input 3.
10	D3	I/O	Drain pin 3. Can be used as input or output.
11	S3	I/O	Source pin 3. Can be used as input or output.
12	NC		Not Connected
13	V _{DD}		Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{DD} and GND.

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Pin No.	Name	I/O	Description
14	S2	I/O	Source pin 2. Can be used as input or output.
15	D2	I/O	Drain pin 2. Can be used as input or output.
16	IN2	I	Logic control input 2.

Table 2. Functional Table

IN1	IN2	IN3	IN4	Function
0	X	X	X	Switch 1 Off
1	X	X	X	Switch 1 On
X	0	X	X	Switch 2 On
X	1	X	X	Switch 2 Off
X	X	0	X	Switch 3 On
X	X	1	X	Switch 3 Off
X	X	X	0	Switch 4 Off
X	X	X	1	Switch 4 On

X denotes do not care.

Specifications

Absolute Maximum Ratings ⁽¹⁾

Parameter		Min	Max	Unit
$V_{DD} - V_{SS}$	Supply Voltage	-0.3	44	V
V_{DD}		-0.3	44	V
V_{SS}		-44	-0.3	V
V_{IN}	Logic Control Input Pin Voltage (IN_X)	-0.3	$V_{DD} + 0.3$	V
V_S or V_D	Switch I/O Port Voltage	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
I_S or $I_{D(CONT)}$	Switch I/O Continuous Current	-30	30	mA
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	-65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±5	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions ⁽¹⁾

Parameter	Min	Max	Unit
Positive Power Supply Voltage (single), V_{DD}	4.5	40	V
Negative Power Supply Voltage (dual), V_{SS}	-20	0	V
Supply Rail Voltage Difference, $V_{DD} - V_{SS}$	4.5	40	V
V_{IN}	0	V_{DD}	V
V_S or V_D	V_{SS}	V_{DD}	V
Operating Temperature Range	-40	125	°C

(1) Input select must be held HIGH or LOW and it shouldn't float.

High Voltage, Low Leakage SPST Analog Switch**Thermal Information**

Package Type	θ_{JA}	θ_{JC}	Unit
SOP16	100	50	°C/W

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Electrical Characteristics

All test conditions: over operating temperature range (–40°C to 125°C), typical at $T_A = 25^\circ\text{C}$, $V_{DD} = 13.5\text{ V}$ to 16.5 V , $V_{SS} = -16.5\text{ V}$ to 13.5 V , and $\text{GND} = 0\text{ V}$, unless otherwise noted.

Symbol	Parameter	Conditions	$V_{DD} / V_{SS} \text{ (V)}$	Min	Typ	Max	Unit
Power Supply							
I_{DD}	Quiescent Supply Current	$V_{IN} = 0\text{ V}$ or V_{DD}	16.5/–1 6.5		250	400	μA
I_{SS}	Quiescent Supply Current	$V_{IN} = 0\text{ V}$ or V_{DD}	16.5/–1 6.5		30	60	μA
Digital Input							
V_{IH}	Input Voltage High		16.5/–1 6.5	1.35			V
V_{IL}	Input Voltage Low		16.5/–1 6.5			0.8	V
I_{IN}	Input Leakage Current	$V_{IN} = 0\text{ V}$ or V_{DD}	16.5/–1 6.5	–0.1	0.005	0.1	μA
$C_{IN}^{(1)}$	Logic Input Capacitance		15/–15		3		pF
Analog Switch							
R_{ON}	On Resistance	$V_S = -10\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, Figure 11	13.5/–1 3.5		4	7	Ω
		$V_S = -10\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				7	Ω
ΔR_{ON}	On Resistance Match between Channels	$V_S = -10\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, Figure 11	13.5/–1 3.5		0.1	0.5	Ω
		$V_S = -10\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				0.5	Ω
$R_{FLAT(ON)}$	On Resistance Flatness	$V_S = -10\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, Figure 11	13.5/–1 3.5		0.2	0.5	Ω
		$V_S = -10\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				0.5	Ω
$I_S(\text{Off})$	Source Off Leakage	Switch Off, $V_S = 10\text{ V}$, -10 V , $V_D = -10\text{ V}$, 10 V , Figure 13	16.5/–1 6.5	–23	± 0.05	23	nA
		Switch Off, $V_S = 10\text{ V}$, -10 V , $V_D = -10\text{ V}$, 10 V , $T_A = -40^\circ\text{C}$ to 85°C , Figure 13		–1.3		1.3	nA
$I_D(\text{Off})$	Drain Off Leakage	Switch Off, $V_S = 10\text{ V}$, -10 V , $V_D = -10\text{ V}$, 10 V , Figure 13	16.5/–1 6.5	–23	± 0.05	23	nA

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Symbol	Parameter	Conditions	V _{DD} / V _{SS} (V)	Min	Typ	Max	Unit
		Switch Off, V _S = 10 V, −10 V, V _D = −10 V, 10 V, T _A = −40°C to 85°C, Figure 13		−1.3		1.3	nA
I _S (On), I _D (On)	Channel On Leakage	Switch On, V _S = V _D = 10 V or V _S = V _D = −10 V, Figure 12	16.5/-1 6.5	−30	±0.050	30	nA
		Switch On, V _S = V _D = 10 V or V _S = V _D = −10 V, T _A = −40°C to 85°C, Figure 12		−1		1	nA
Dynamic Characteristics ⁽¹⁾							
t _B	Break-Before-Make Time	V _S = 10 V, R _L = 300 Ω, C _L = 35 pF, Figure 14	15/−15	80	90		ns
t _{ON}	Switch Turn-on Time	V _S = 10 V, R _L = 300 Ω, C _L = 35 pF, Figure 15	15/−15		180	390	ns
t _{OFF}	Switch Turn-off Time	V _S = 10 V, R _L = 300 Ω, C _L = 35 pF, Figure 15	15/−15		90	100	ns
Q _C	Charge Injection	V _S = 0 V, C _L = 1 nF, Figure 16	15/−15		±200		pC
OISO	OFF-Isolation	R _L = 50 Ω, C _L = 5 pF, V _{BIAS} = 0 V, f = 1 MHz, Test Circuit and Waveforms, Figure 17	15/−15		−80		dB
XTALK	Crosstalk	R _L = 50 Ω, C _L = 5 pF, V _{BIAS} = 0 V, f = 1 MHz, Figure 18	15/−15		−100		dB
BW	Bandwidth	R = 50 Ω, C = 5 pF, V _{BIAS} = 0 V, Figure 19	15/−15		500		MHz
Capacitance ⁽¹⁾							
C _S (Off), C _D (Off)	Off Capacitance	f = 1 MHz, V _{BIAS} = 0 V	15/−15		8		pF
C _S (On), C _D (On)	On Capacitance	f = 1 MHz, V _{BIAS} = 0 V	15/−15		8		pF

Electrical Characteristics (Continued)

All test conditions: over operating temperature range (–40°C to 125°C), typical at $T_A = 25^\circ\text{C}$, $V_{DD} = 10.8\text{ V}$ to 13.2 V , $V_{SS} = 0\text{ V}$, and $\text{GND} = 0\text{ V}$, unless otherwise noted.

Symbol	Parameter	Conditions	$V_{DD} / V_{SS} \text{ (V)}$	Min	Typ	Max	Unit
Power Supply							
I_{DD}	Quiescent Supply Current	$V_{IN} = 0\text{ V}$ or V_{DD}	13.2/0		250	400	μA
I_{SS}	Quiescent Supply Current	$V_{IN} = 0\text{ V}$ or V_{DD}	13.2/0		30	60	μA
Digital Input							
V_{IH}	Input Voltage High		13.2/0	1.35			V
V_{IL}	Input Voltage Low		13.2/0			0.8	V
I_{IN}	Input Leakage Current	$V_{IN} = 0\text{ V}$ or V_{DD}	13.2/0	–0.1	± 0.005	0.1	μA
$C_{IN}^{(1)}$	Logic Input Capacitance		12/0		3		pF
Analog Switch							
R_{ON}	On Resistance	$V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, Figure 11	10.8/0		4	7	Ω
		$V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				7	Ω
ΔR_{ON}	On Resistance Match between Channels	$V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, Figure 11	10.8/0		0.1	0.5	Ω
		$V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				0.5	Ω
$R_{FLAT(ON)}$	On Resistance Flatness	$V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, Figure 11	10.8/0		0.2	0.5	Ω
		$V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				0.5	Ω
$I_S(\text{Off})$	Source Off Leakage	Switch Off, $V_S = 10\text{ V}$, 0 V , $V_D = 0\text{ V}$, 10 V , Figure 13	13.2/0	–15	± 0.05	15	nA
		Switch Off, $V_S = 10\text{ V}$, 0 V , $V_D = 0\text{ V}$, 10 V , $T_A = -40^\circ\text{C}$ to 85°C , Figure 13				0.8	nA
$I_D(\text{Off})$	Drain Off Leakage	Switch Off, $V_S = 10\text{ V}$, 0 V , $V_D = 0\text{ V}$, 10 V , Figure 13	13.2/0	–15	± 0.05	15	nA
		Switch Off, $V_S = 10\text{ V}$, 0 V , $V_D = 0\text{ V}$, 10 V , $T_A = -40^\circ\text{C}$ to 85°C , Figure 13		–0.8		0.8	nA
$I_S(\text{On})$, $I_D(\text{On})$	Channel On Leakage	Switch On, $V_S = V_D = 0\text{ V}$ or $V_S = V_D = 10\text{ V}$, Figure 12	13.2/0	–30	0.05	30	nA

High Voltage, Low Leakage SPST Analog Switch

Symbol	Parameter	Conditions	V_{DD} / V_{SS} (V)	Min	Typ	Max	Unit
		Switch On, $V_S = V_D = 0$ V or $V_S = V_D = 10$ V, $T_A = -40^\circ\text{C}$ to 85°C , Figure 12		-1		1	nA
Dynamic Characteristics ⁽¹⁾							
t_B	Break-Before-Make Time	$V_S = 8$ V, $R_L = 300\ \Omega$, $C_L = 35$ pF, Figure 14	12/0	10	15		ns
t_{ON}	Switch Turn-on Time	$V_S = 8$ V, $R_L = 300\ \Omega$, $C_L = 35$ pF, Figure 15	12/0		150	360	ns
t_{OFF}	Switch Turn-off Time	$V_S = 8$ V, $R_L = 300\ \Omega$, $C_L = 35$ pF, Figure 15	12/0		130	200	ns
Q_C	Charge Injection	$V_S = 6$ V, $C_L = 1$ nF, Figure 16	12/0		± 120		pC
OISO	OFF-Isolation	$R_L = 50\ \Omega$, $C_L = 5$ pF, $V_{BIAS} = 6$ V, $f = 1$ MHz, Figure 17	12/0		-70		dB
XTALK	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5$ pF, $V_{BIAS} = 6$ V, $f = 1$ MHz, Figure 18	12/0		-100		dB
BW	Bandwidth	$R_L = 50\ \Omega$, $C_L = 5$ pF, $V_{BIAS} = 3$ V, Figure 19	12/0		400		MHz
Capacitance ⁽¹⁾							
$C_S(\text{Off})$, $C_D(\text{Off})$	Off Capacitance	$f = 1$ MHz, $V_{BIAS} = 6$ V	12/0		12		pF
$C_S(\text{On})$, $C_D(\text{On})$	On Capacitance	$f = 1$ MHz, $V_{BIAS} = 6$ V	12/0		12		pF

(1) Provided by design simulation and lab test, not subject to production test.

Electrical Characteristics (Continued)

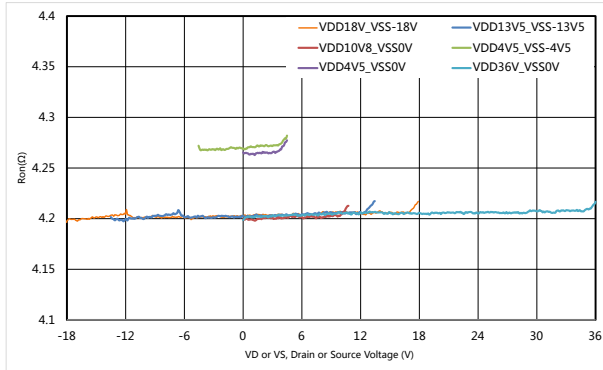
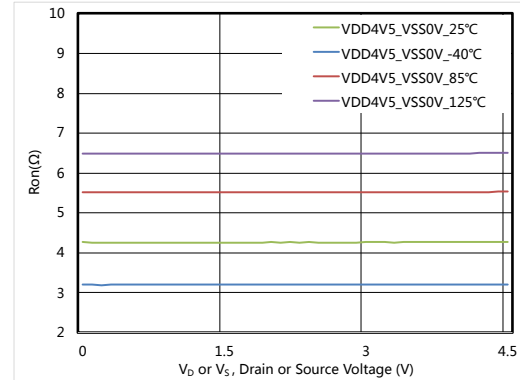
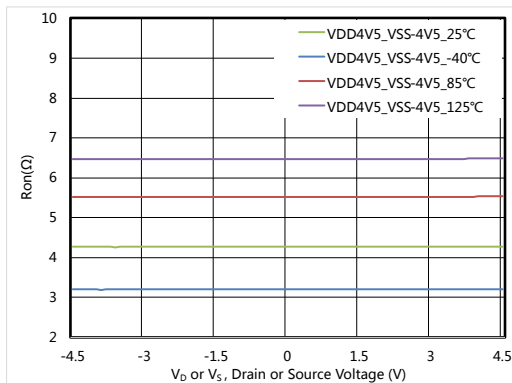
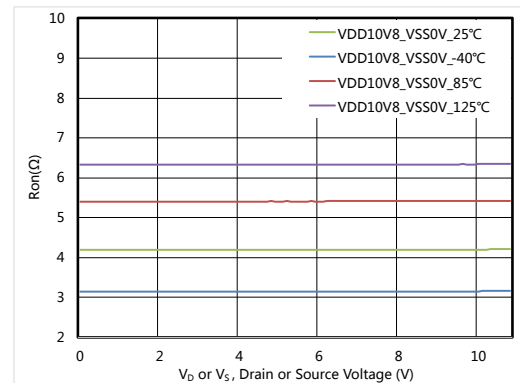
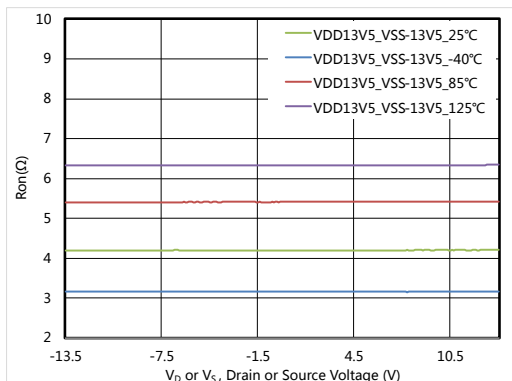
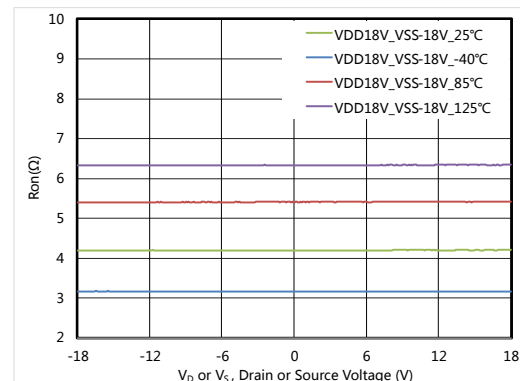
All test conditions: over operating temperature range (–40°C to 125°C), typical at $T_A = 25^\circ\text{C}$, $V_{DD} = 4.5\text{ V}$ to 5.5 V , $V_{SS} = -5.5\text{ V}$ to -4.5 V , and $\text{GND} = 0\text{ V}$, unless otherwise noted.

Symbol	Parameter	Conditions	$V_{DD} / V_{SS} \text{ (V)}$	Min	Typ	Max	Unit
Power Supply							
I_{DD}	Quiescent Supply Current	$V_{IN} = 0\text{ V}$ or V_{DD}	5.5/–5.5		250	400	μA
I_{SS}	Quiescent Supply Current	$V_{IN} = 0\text{ V}$ or V_{DD}	5.5/–5.5		30	60	μA
Digital Input							
V_{IH}	Input Voltage High		5.5/–5.5	1.35			V
V_{IL}	Input Voltage Low		5.5/–5.5			0.8	V
I_{IN}	Input Leakage Current	$V_{IN} = 0\text{ V}$ or V_{DD}	5.5/–5.5	–0.1	± 0.005	0.1	μA
$C_{IN}^{(1)}$	Logic Input Capacitance		5/–5		3		pF
Analog Switch							
R_{ON}	On Resistance	$V_S = -3.5\text{ V}$ to 3.5 V , $I_S = -10\text{ mA}$, Figure 11	4.5/–4.5		4	7	Ω
		$V_S = -3.5\text{ V}$ to 3.5 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				7	Ω
ΔR_{ON}	On Resistance Match between Channels	$V_S = -3.5\text{ V}$ to 3.5 V , $I_S = -10\text{ mA}$, Figure 11	4.5/–4.5		0.1	0.5	Ω
		$V_S = -3.5\text{ V}$ to 3.5 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				0.5	Ω
$R_{FLAT(ON)}$	On Resistance Flatness	$V_S = -3.5\text{ V}$ to 3.5 V , $I_S = -10\text{ mA}$, Figure 11	4.5/–4.5		0.2	0.5	Ω
		$V_S = -3.5\text{ V}$ to 3.5 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				0.5	Ω
$I_S(\text{Off})$	Source Off Leakage	Switch Off, $V_S = 4.5\text{ V}$, -4.5 V , $V_D = -4.5\text{ V}$, 4.5 V , Figure 13	5.5/–5.5	–15	± 0.02	15	nA
		Switch Off, $V_S = 4.5\text{ V}$, -4.5 V , $V_D = -4.5\text{ V}$, 4.5 V , $T_A = -40^\circ\text{C}$ to 85°C , Figure 13		–0.8		0.8	nA
$I_D(\text{Off})$	Drain Off Leakage	Switch Off, $V_S = 4.5\text{ V}$, -4.5 V , $V_D = -4.5\text{ V}$, 4.5 V , Figure 13	5.5/–5.5	–15	0.03	15	nA

High Voltage, Low Leakage SPST Analog Switch

Symbol	Parameter	Conditions	V _{DD} / V _{SS} (V)	Min	Typ	Max	Unit
		Switch Off, V _S = 4.5 V, −4.5 V, V _D = −4.5 V, 4.5 V, T _A = −40°C to 85°C, Figure 13		−0.8		0.8	nA
I _S (On), I _D (On)	Channel On Leakage	Switch On, V _S = V _D =4.5 V or V _S = V _D = −4.5 V, Figure 12	5.5/−5 .5	−22	±0.02	22	nA
		Switch On, V _S = V _D =4.5 V or V _S = V _D = −4.5 V, T _A = −40°C to 85°C, Figure 12		−0.8		0.8	nA
Dynamic Characteristics ⁽¹⁾							
t _B	Break-Before-Make Time	V _S = 3 V, R _L = 300 Ω, C _L = 35 pF, Figure 14	5/−5	60	80		ns
t _{ON}	Switch Turn-on Time	V _S = 3 V, R _L = 300 Ω, C _L = 35 pF, Figure 15	5/−5		200	380	ns
t _{OFF}	Switch Turn-off Time	V _S = 3 V, R _L = 300 Ω, C _L = 35 pF, Figure 15	5/−5		110	140	ns
Q _C	Charge Injection	V _S = 0 V, C _L = 1 nF, Figure 16	5/−5		±120		pC
OISO	OFF-Isolation	R _L = 50 Ω, C _L = 5 pF, V _{BIAS} = 0 V, f = 1 MHz, Figure 17	5/−5		−80		dB
XTALK	Crosstalk	R _L = 50 Ω, C _L = 5 pF, V _{BIAS} = 0 V, f = 1 MHz, Figure 18	5/−5		−100		dB
BW	Bandwidth	R _L = 50 Ω, C _L = 5 pF, V _{BIAS} = 0 V, Figure 19	5/−5		480		MHz
Capacitance ⁽¹⁾							
C _S (Off), C _D (Off)	Off Capacitance	f = 1 MHz, V _{BIAS} = 0 V	5/−5		10		pF
C _S (On), C _D (On)	On Capacitance	f = 1 MHz, V _{BIAS} = 0 V	5/−5		10		pF

(1) Provided by design simulation and lab test, not subject to production test.

Typical Performance Characteristics

Figure 1. R_{ON} vs V_{DD} , Temp = 25°C

Figure 2. R_{ON} , $V_{DD} = 4.5$ V, $V_{SS} = 0$ V, Temp = -40°C, 25°C, 85°C, 125°C

Figure 3. R_{ON} , $V_{DD} = 4.5$ V, $V_{SS} = -4.5$ V, Temp = -40°C, 25°C, 85°C, 125°C

Figure 4. R_{ON} , $V_{DD} = 10.8$ V, $V_{SS} = 0$ V, Temp = -40°C, 25°C, 85°C, 125°C

Figure 5. R_{ON} , $V_{DD} = 13.5$ V, $V_{SS} = -13.5$ V, Temp = -40°C, 25°C, 85°C, 125°C

Figure 6. R_{ON} , $V_{DD} = 18$ V, $V_{SS} = -18$ V, Temp = -40°C, 25°C, 85°C, 125°C

High Voltage, Low Leakage SPST Analog Switch

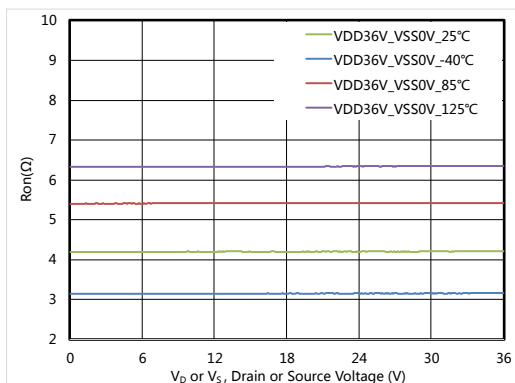


Figure 7. R_{ON} , $V_{DD} = 36\text{ V}$, $V_{SS} = 0\text{ V}$, Temp = -40°C , 25°C , 85°C , 125°C

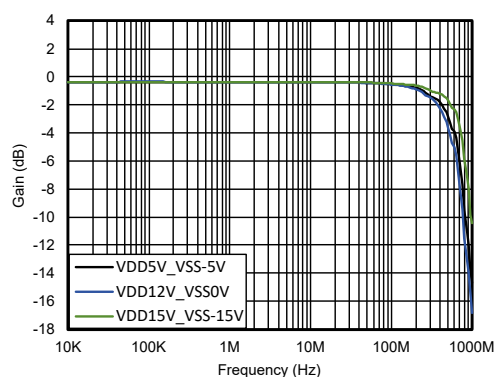


Figure 8. Bandwidth, $V_{DD}/V_{SS} = 5\text{ V}/-5\text{ V}$, $12\text{ V}/0\text{ V}$, $15\text{ V}/-15\text{ V}$

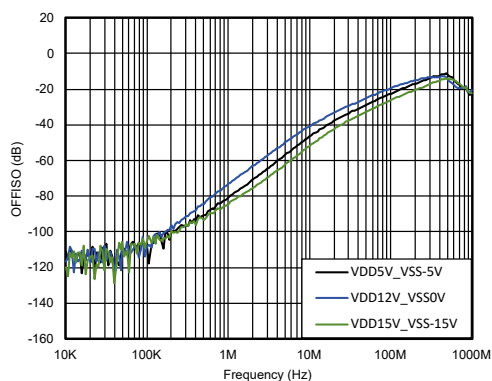


Figure 9. OFFISO, $V_{DD}/V_{SS} = 5\text{ V}/-5\text{ V}$, $12\text{ V}/0\text{ V}$, $15\text{ V}/-15\text{ V}$

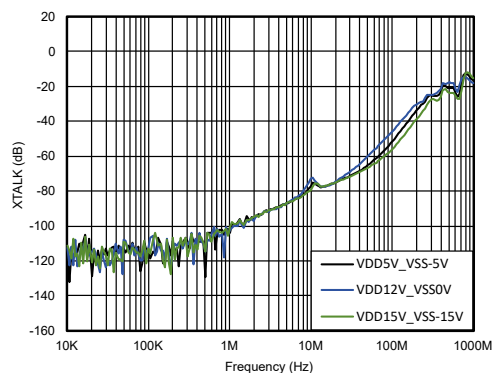


Figure 10. Crosstalk, $V_{DD}/V_{SS} = 5\text{ V}/-5\text{ V}$, $12\text{ V}/0\text{ V}$, $15\text{ V}/-15\text{ V}$

Test Circuit and Waveforms

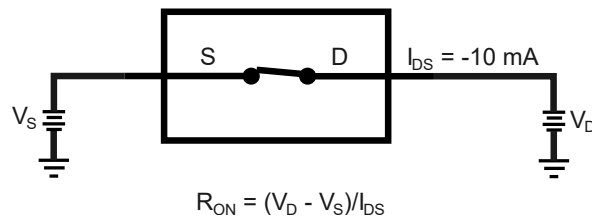


Figure 11. On Resistance

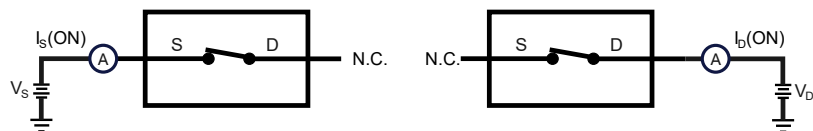


Figure 12. On Leakage

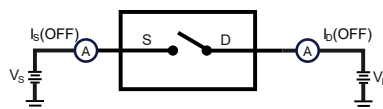


Figure 13. Off Leakage

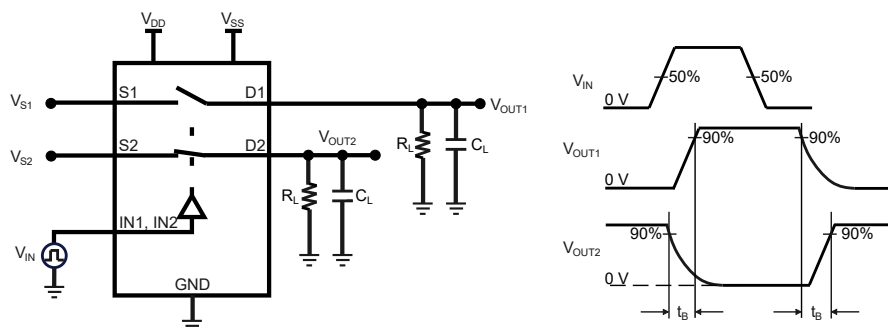


Figure 14. Switch Break Time

High Voltage, Low Leakage SPST Analog Switch

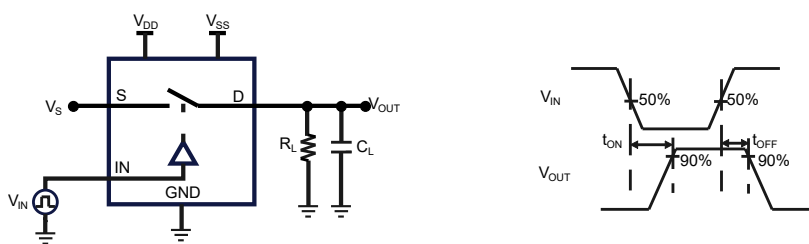


Figure 15. Switching Time

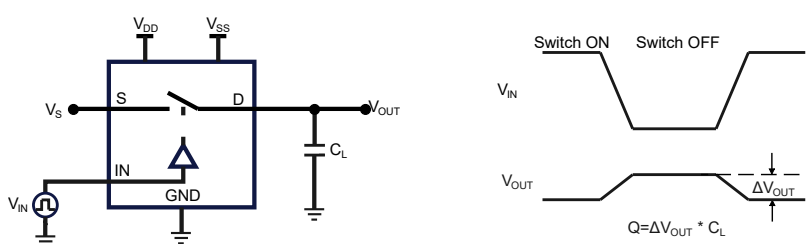


Figure 16. Charge Injection

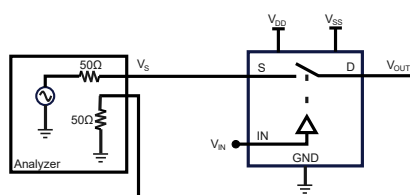


Figure 17. Off Isolation

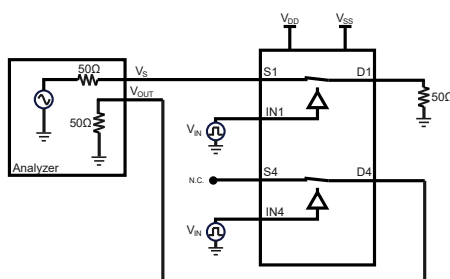


Figure 18. Crosstalk

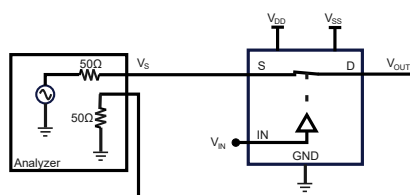


Figure 19. Bandwidth

Application and Implementation

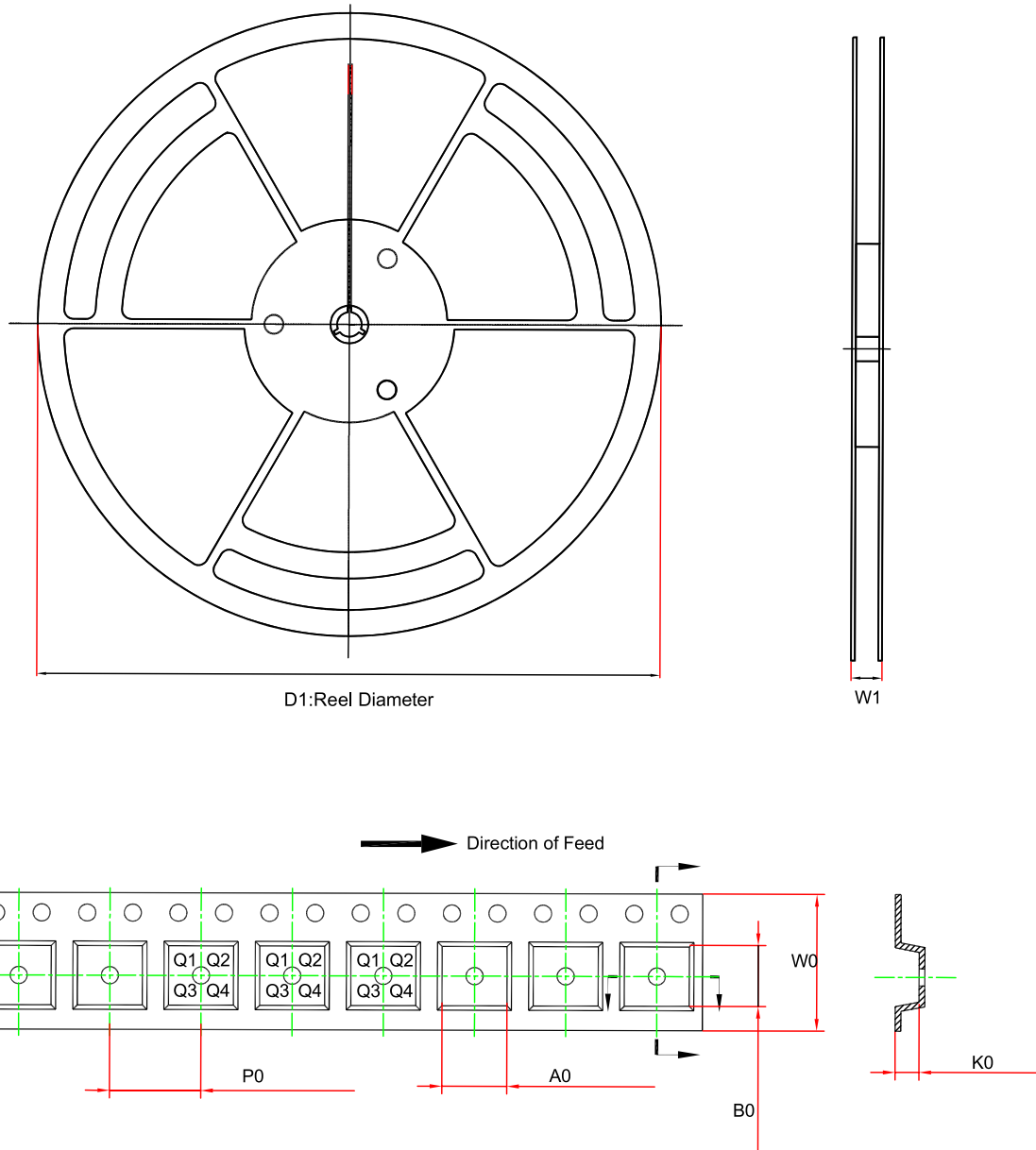
Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

0.1- μ F bypass capacitors on V_{DD} and V_{SS} are recommended to prevent power disturbance.

Tape and Reel Information



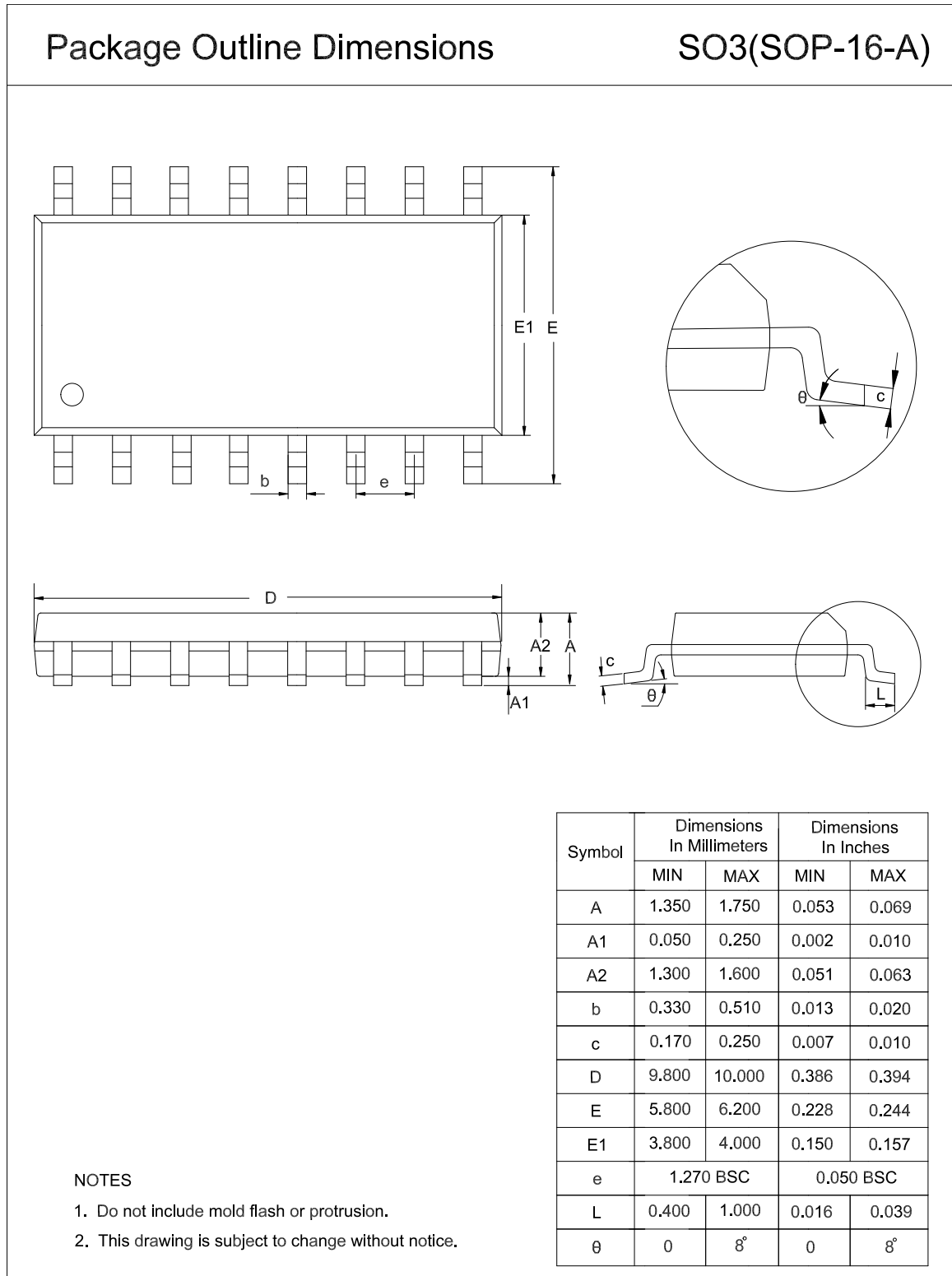
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) ⁽¹⁾	B0 (mm) ⁽¹⁾	K0 (mm) ⁽¹⁾	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPW6414R-SO3R-S	SOP16	330.0	20.4	6.8	10.5	2.2	8.0	16.0	Q1
TPW6414R-TS3R-S ⁽²⁾	TSSOP16	330.0	17.6	6.8	5.5	1.5	8.0	12.0	Q1

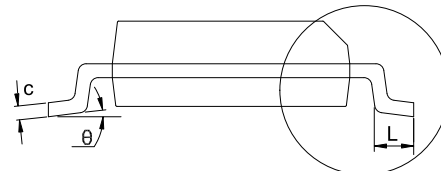
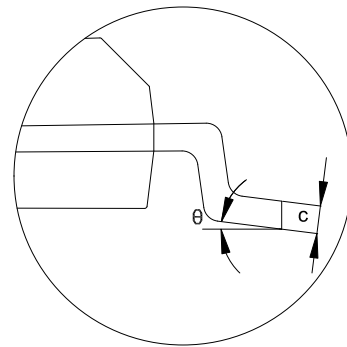
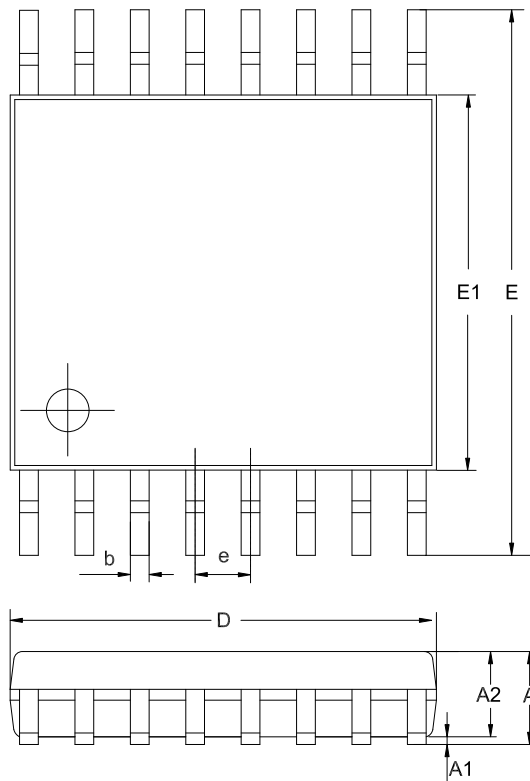
(1) The value is for reference only. Contact the 3PEAK factory for more information.

(2) For the future product, contact the 3PEAK factory for more information and samples.

Package Outline Dimensions

SOP16



TSSOP16 ⁽¹⁾
Package Outline Dimensions
TS3(TSSOP-16-A)


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

(1) For the future product, contact the 3PEAK factory for more information and samples.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPW6414R-SO3R-S	-40 to 125°C	SOP16	W6414R	MSL3	Tape and Reel, 2500	Green
TPW6414R-TS3R-S ⁽¹⁾	-40 to 125°C	TSSOP16	W6414R	MSL3	Tape and Reel, 3000	Green

(1) For the future product, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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