

High Voltage, Low Leakage SPDT Analog Switch

Features

- Supply Voltage: 4.5 V to 40 V
- Dual Supply Voltage: Up to ± 20 V
- Low Leakage: Maximum 4 nA at -40°C to 85°C
- Low ON-State Resistance: Typical $2.5\ \Omega$ at ± 15 V
- Low On-State Resistance Flatness
- -3 dB Bandwidth: 200 MHz at ± 15 V
- 1.8-V Logic Compatible
- Rail-to-Rail Operation
- Break-Before-Making Switching
- Operation Temperature Range: -40°C to 125°C

Applications

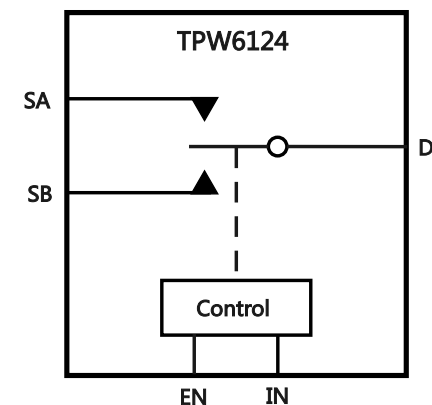
- Industry Control Systems
- Battery-Powered Systems
- Audio Signal Routing
- Portable Instruments and Mobile Devices

Description

The TPW6124 is a monolithic CMOS SPDT switch. This switch comprises one single-pole dual-throw (SPDT) analog switch controlled by two digital logic (EN, IN). The TPW6124 features low on resistance, low resistance flatness, and low leakage current. The TPW6124 can operate from a single-supply range of 4.5 V to 40 V.

The TPW6124 is available in the DFN2X3-8 package, and is characterized from -40°C to $+125^{\circ}\text{C}$.

Functional Block Diagram



SWITCHES SHOWN FOR A LOGIC 0 INPUT

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Revision History

Date	Revision	Notes
2026-05-09	Rev.A.0	Initial Version.

Pin Configuration and Functions

TPW6124
DFN2X3-6
Top View

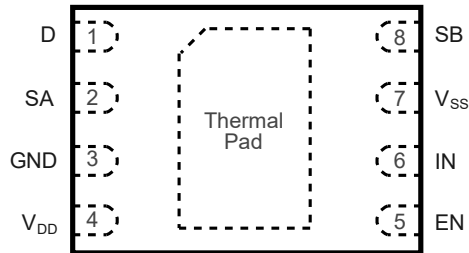


Table 1. Pin Functions

Pin No.	Name	I/O	Description
1	D	I/O	Drain pin. Can be used as input or output.
2	SA	I/O	Source pin A. Can be used as input or output.
3	GND		Ground (0 V) reference pin.
4	V _{DD}		Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{DD} and GND.
5	EN	I	Active High logic Input. When this pin is low, the device is disabled and all switches are returned off. When this pin is high, the IN logic input determines which switch is turned on.
6	IN	I	Logic control input.
7	V _{SS}		Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{SS} and GND. V _{SS} must be connected to ground for single supply voltage applications.
8	SB	I/O	Source pin B. Can be used as input or output.
	Thermal Pad		Exposed Pad. Exposed pad tied to substrate, V _{SS} .

Table 2. Functional Table

EN	IN	Switch A	Switch B
0	X	Off	Off
1	0	On	Off
1	1	Off	On

X denotes do not care.

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Specifications

Absolute Maximum Ratings ⁽¹⁾

Parameter		Min	Max	Unit
$V_{DD} - V_{SS}$	Supply Voltage	-0.3	44	V
V_{DD}		-0.3	44	V
V_{SS}		-44	-0.3	V
V_{IN}	Logic Control Input Pin Voltage (EN, IN)	-0.3	$V_{DD} + 0.3$	V
V_S or V_D	Switch I/O Port Voltage	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
I_S or $I_{D(CONT)}$	Switch I/O Continuous Current	-30	30	mA
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	-65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions ⁽¹⁾

Parameter	Min	Max	Unit
Positive Power Supply Voltage (single), V_{DD}	4.5	40	V
Negative Power Supply Voltage (dual), V_{SS}	-20	0	V
Supply Rail Voltage Difference, $V_{DD} - V_{SS}$	4.5	40	V
V_{IN}	0	V_{DD}	V
V_S or V_D	V_{SS}	V_{DD}	V
Operating Temperature Range	-40	125	°C

(1) Input select must be held HIGH or LOW and it shouldn't float.

High Voltage, Low Leakage SPDT Analog Switch**Thermal Information**

Package Type	θ_{JA}	θ_{JC}	Unit
DFN2X3-6	53.7	55.9	°C/W

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Electrical Characteristics

All test conditions: over operating temperature range (–40°C to 125°C), typical at $T_A = 25^\circ\text{C}$, $V_{DD} = 13.5\text{ V}$ to 16.5 V , $V_{SS} = -16.5\text{ V}$ to 13.5 V , and $\text{GND} = 0\text{ V}$, unless otherwise noted.

Symbol	Parameter	Conditions	$V_{DD} / V_{SS} \text{ (V)}$	Min	Typ	Max	Unit
Power Supply							
I_{DD}	Quiescent Supply Current	$V_{IN} = 0\text{ V}$ or V_{DD}	16.5/–1 6.5		200	400	μA
I_{SS}	Quiescent Supply Current	$V_{IN} = 0\text{ V}$ or V_{DD}	16.5/–1 6.5		100	200	μA
Digital Input							
V_{IH}	Input Voltage High		16.5/–1 6.5	1.35			V
V_{IL}	Input Voltage Low		16.5/–1 6.5			0.8	V
I_{IN}	Input Leakage Current	$V_{IN} = 0\text{ V}$ or V_{DD}	16.5/–1 6.55	–0.1	± 0.005	0.1	μA
$C_{IN}^{(1)}$	Logic Input Capacitance		15/–15		2		pF
Analog Switch							
R_{ON}	On Resistance	$V_S = -10\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, Figure 11	13.5/–1 3.5		2.5	4	Ω
		$V_S = -10\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				4	Ω
ΔR_{ON}	On Resistance Match between Channels	$V_S = -10\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, Figure 11	13.5/–1 3.5		0.2	0.5	Ω
		$V_S = -10\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				0.5	Ω
$R_{FLAT(ON)}$	On Resistance Flatness	$V_S = -10\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, Figure 11	13.5/–1 3.5		0.1	0.5	Ω
		$V_S = -10\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				0.5	Ω
$I_S(\text{Off})$	Source Off Leakage	Switch Off, $V_S = 10\text{ V}$, -10 V , $V_D = -10\text{ V}$, 10 V , Figure 13	16.5/–1 6.5		± 0.05	30	nA
		Switch Off, $V_S = 10\text{ V}$, -10 V , $V_D = -10\text{ V}$, 10 V , $T_A = -40^\circ\text{C}$ to 85°C , Figure 13				3	nA
$I_D(\text{Off})$	Dain Off Leakage	Switch Off, $V_S = 10\text{ V}$, -10 V , $V_D = -10\text{ V}$, 10 V , Figure 13	16.5/–1 6.5		0.05	50	nA

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Symbol	Parameter	Conditions	V _{DD} / V _{SS} (V)	Min	Typ	Max	Unit
		Switch Off, V _S = 10 V, −10 V, V _D = −10 V, 10 V, T _A = −40°C to 85°C, Figure 13				4	nA
I _S (On), I _D (On)	Channel On Leakage	Switch On, V _S = V _D = 10 V or V _S = V _D = −10 V, Figure 12	16.5/−1 6.5		±0.05	55	nA
		Switch On, V _S = V _D = 10 V or V _S = V _D = −10 V, T _A = −40°C to 85°C, Figure 12				4	nA
Dynamic Characteristics ⁽¹⁾							
t _B	Break-Before-Make Time	V _S = 10 V, R _L = 300 Ω, C _L = 35 pF, Figure 14	15/−15	80	92		ns
t _{ON}	Switch Turn-on Time	V _S = 10 V, R _L = 300 Ω, C _L = 35 pF, Figure 15	15/−15		158	384	ns
t _{OFF}	Switch Turn-off Time	V _S = 10 V, R _L = 300 Ω, C _L = 35 pF, Figure 15	15/−15		100	123	ns
t _{TRAN}	Transition Time	V _S = 10 V, R _L = 300 Ω, C _L = 35 pF, Figure 16	15/−15		180	320	ns
Q _C	Charge Injection	V _S = 0 V, C _L = 1 nF, Figure 17	15/−15		±400		pC
OISO	OFF-Isolation	R _L = 50 Ω, C _L = 5 pF, V _{BIAS} = 0 V, f = 1 MHz, Test Circuit and Waveforms, Figure 18	15/−15		−75		dB
XTALK	Crosstalk	R _L = 50 Ω, C _L = 5 pF, V _{BIAS} = 0 V, f = 1 MHz, Figure 19	15/−15		−75		dB
BW	Bandwidth	R = 50 Ω, C = 5 pF, V _{BIAS} = 0 V, Figure 20	15/−15		200		MHz
Capacitance ⁽¹⁾							
C _S (Off)	Source Off Capacitance	f = 1 MHz, V _{BIAS} = 0 V	15/−15		17		pF
C _D (Off)	Drain Off Capacitance	f = 1 MHz, V _{BIAS} = 0 V	15/−15		31		pF
C _S (On), C _D (On)	On Capacitance	f = 1 MHz, V _{BIAS} = 0 V	15/−15		30		pF

High Voltage, Low Leakage SPDT Analog Switch

Electrical Characteristics (Continued)

All test conditions: over operating temperature range (–40°C to 125°C), typical at $T_A = 25^\circ\text{C}$, $V_{DD} = 10.8\text{ V}$ to 13.2 V , $V_{SS} = 0\text{ V}$, and $\text{GND} = 0\text{ V}$, unless otherwise noted.

Symbol	Parameter	Conditions	$V_{DD} / V_{SS} \text{ (V)}$	Min	Typ	Max	Unit
Power Supply							
I_{DD}	Quiescent Supply Current	$V_{IN} = 0\text{ V}$ or V_{DD}	13.2/0		200	400	μA
I_{SS}	Quiescent Supply Current	$V_{IN} = 0\text{ V}$ or V_{DD}	13.2/0		100	200	μA
Digital Input							
V_{IH}	Input Voltage High		13.2/0	1.35			V
V_{IL}	Input Voltage Low		13.2/0			0.8	V
I_{IN}	Input Leakage Current	$V_{IN} = 0\text{ V}$ or V_{DD}	13.2/0	–0.1	± 0.005	0.1	μA
$C_{IN}^{(1)}$	Logic Input Capacitance		13.2/0		2		pF
Analog Switch							
R_{ON}	On Resistance	$V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, Figure 11	10.8/0		2.5	4	Ω
		$V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				4	Ω
ΔR_{ON}	On Resistance Match between Channels	$V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, Figure 11	10.8/0		0.2	0.5	Ω
		$V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				0.5	Ω
$R_{FLAT(ON)}$	On Resistance Flatness	$V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, Figure 11	10.8/0		0.1	0.5	Ω
		$V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				0.5	Ω
$I_{S(Off)}$	Source Off Leakage	Switch Off, $V_S = 10\text{ V}$, 0 V , $V_D = 0\text{ V}$, 10 V , Figure 13	13.2/0		0.02	22	nA
		Switch Off, $V_S = 10\text{ V}$, 0 V , $V_D = 0\text{ V}$, 10 V , $T_A = -40^\circ\text{C}$ to 85°C , Figure 13				1.5	nA
$I_{D(Off)}$	Drain Off Leakage	Switch Off, $V_S = 10\text{ V}$, 0 V , $V_D = 0\text{ V}$, 10 V , Figure 13	13.2/0		0.02	40	nA
		Switch Off, $V_S = 10\text{ V}$, 0 V , $V_D = 0\text{ V}$, 10 V , $T_A = -40^\circ\text{C}$ to 85°C , Figure 13				2.5	nA
$I_{S(On)}, I_{D(On)}$	Channel On Leakage	Switch On, $V_S = V_D = 0\text{ V}$ or $V_S = V_D = 10\text{ V}$, Figure 12	13.2/0		0.05	53	nA

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Symbol	Parameter	Conditions	V_{DD} / V_{SS} (V)	Min	Typ	Max	Unit
		Switch On, $V_S = V_D = 0$ V or $V_S = V_D = 10$ V, $T_A = -40^{\circ}\text{C}$ to 85°C , Figure 12				3	nA
Dynamic Characteristics ⁽¹⁾							
t_B	Break-Before-Make Time	$V_S = 8$ V, $R_L = 300\ \Omega$, $C_L = 35$ pF, Figure 14	12/0	15	20		ns
t_{ON}	Switch Turn-on Time	$V_S = 8$ V, $R_L = 300\ \Omega$, $C_L = 35$ pF, Figure 15	12/0		190	290	ns
t_{OFF}	Switch Turn-off Time	$V_S = 8$ V, $R_L = 300\ \Omega$, $C_L = 35$ pF, Figure 15	12/0		160	240	ns
t_{TRAN}	Transition Time	$V_S = 8$ V, $R_L = 300\ \Omega$, $C_L = 35$ pF, Figure 16	12/0		260	400	ns
Q_C	Charge Injection	$V_S = 6$ V, $C_L = 1$ nF, Figure 17	12/0		± 200		pC
OISO	OFF-Isolation	$R_L = 50\ \Omega$, $C_L = 5$ pF, $V_{BIAS} = 6$ V, $f = 1$ MHz, Figure 18	12/0		-65		dB
XTALK	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5$ pF, $V_{BIAS} = 6$ V, $f = 1$ MHz, Figure 19	12/0		-65		dB
BW	Bandwidth	$R_L = 50\ \Omega$, $C_L = 5$ pF, $V_{BIAS} = 3$ V, Figure 20	12/0		140		MHz
Capacitance ⁽¹⁾							
$C_S(\text{Off})$	Source Off Capacitance	$f = 1$ MHz, $V_{BIAS} = 6$ V	12/0		25		pF
$C_D(\text{Off})$	Drain Off Capacitance	$f = 1$ MHz, $V_{BIAS} = 6$ V	12/0		38		pF
$C_S(\text{On})$, $C_D(\text{On})$	On Capacitance	$f = 1$ MHz, $V_{BIAS} = 6$ V	12/0		42		pF

(1) Provided by design simulation and lab test, not subject to production test.

High Voltage, Low Leakage SPDT Analog Switch

Electrical Characteristics (Continued)

All test conditions: over operating temperature range (–40°C to 125°C), typical at $T_A = 25^\circ\text{C}$, $V_{DD} = 4.5\text{ V}$ to 5.5 V , $V_{SS} = -5.5\text{ V}$ to -4.5 V , and $\text{GND} = 0\text{ V}$, unless otherwise noted.

Symbol	Parameter	Conditions	$V_{DD} / V_{SS} \text{ (V)}$	Min	Typ	Max	Unit
Power Supply							
I_{DD}	Quiescent Supply Current	$V_{IN} = 0\text{ V}$ or V_{DD}	5.5/–5.5		200	400	μA
I_{SS}	Quiescent Supply Current	$V_{IN} = 0\text{ V}$ or V_{DD}	5.5/–5.5		100	200	μA
Digital Input							
V_{IH}	Input Voltage High		5.5/–5.5	1.35			V
V_{IL}	Input Voltage Low		5.5/–5.5			0.8	V
I_{IN}	Input Leakage Current	$V_{IN} = 0\text{ V}$ or V_{DD}	5.5/–5.5	–0.1	± 0.01	0.1	μA
$C_{IN}^{(1)}$	Logic Input Capacitance		5/–5		2		pF
Analog Switch							
R_{ON}	On Resistance	$V_S = -3.5\text{ V}$ to 3.5 V , $I_S = -10\text{ mA}$, Figure 11	4.5/–4.5		2.5	4	Ω
		$V_S = -3.5\text{ V}$ to 3.5 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				4	Ω
ΔR_{ON}	On Resistance Match between Channels	$V_S = -3.5\text{ V}$ to 3.5 V , $I_S = -10\text{ mA}$, Figure 11	4.5/–4.5		0.2	0.5	Ω
		$V_S = -3.5\text{ V}$ to 3.5 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				0.5	Ω
$R_{FLAT(ON)}$	On Resistance Flatness	$V_S = -3.5\text{ V}$ to 3.5 V , $I_S = -10\text{ mA}$, Figure 11	4.5/–4.5		0.1	0.5	Ω
		$V_S = -3.5\text{ V}$ to 3.5 V , $I_S = -10\text{ mA}$, $T_A = -40^\circ\text{C}$ to 85°C , Figure 11				0.5	Ω
$I_S(\text{Off})$	Source Off Leakage	Switch Off, $V_S = 4.5\text{ V}$, -4.5 V , $V_D = -4.5\text{ V}$, 4.5 V , Figure 13	5.5/–5.5	–22	0.02	22	nA
		Switch Off, $V_S = 4.5\text{ V}$, -4.5 V , $V_D = -4.5\text{ V}$, 4.5 V , $T_A = -40^\circ\text{C}$ to 85°C , Figure 13		–1.3		1.3	nA
$I_D(\text{Off})$	Drain Off Leakage	Switch Off, $V_S = 4.5\text{ V}$, -4.5 V , $V_D = -4.5\text{ V}$, 4.5 V , Figure 13	5.5/–5.5	–40	0.02	40	nA

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Symbol	Parameter	Conditions	V _{DD} / V _{SS} (V)	Min	Typ	Max	Unit
		Switch Off, V _S = 4.5 V, −4.5 V, V _D = −4.5 V, 4.5 V, T _A = −40°C to 85°C, Figure 13				2.5	nA
I _S (On), I _D (On)	Channel On Leakage	Switch On, V _S = V _D =4.5 V or V _S = V _D = −4.5 V, Figure 12	5.5/−5.5	−53	±0.05	53	nA
		Switch On, V _S = V _D =4.5 V or V _S = V _D = −4.5 V, T _A = −40°C to 85°C, Figure 12		−4		4	nA
Dynamic Characteristics ⁽¹⁾							
t _B	Break-Before-Make Time	V _S = 3 V, R _L = 300 Ω, C _L = 35 pF, Figure 14	5/−5	60	80		ns
t _{ON}	Switch Turn-on Time	V _S = 3 V, R _L = 300 Ω, C _L = 35 pF, Figure 15	5/−5		2.4	7.2	us
t _{OFF}	Switch Turn-off Time	V _S = 3 V, R _L = 300 Ω, C _L = 35 pF, Figure 15	5/−5		120	163	ns
t _{TRAN}	Transition Time	V _S = 3 V, R _L = 300 Ω, C _L = 35 pF, Figure 16	5/−5		200	408	ns
Q _C	Charge Injection	V _S = 0 V, C _L = 1 nF, Figure 17	5/−5		±250		pC
OISO	OFF-Isolation	R _L = 50 Ω, C _L = 5 pF, V _{BIAS} = 0 V, f = 1 MHz, Figure 18	5/−5		−75		dB
XTALK	Crosstalk	R _L = 50 Ω, C _L = 5 pF, V _{BIAS} = 0 V, f = 1 MHz, Figure 19	5/−5		−75		dB
BW	Bandwidth	R _L = 50 Ω, C _L = 5 pF, V _{BIAS} = 0 V, Figure 20	5/−5		160		MHz
Capacitance ⁽¹⁾							
C _S (Off)	Source Off Capacitance	f = 1 MHz, V _{BIAS} = 0 V	5/−5		25		pF
C _D (Off)	Drain Off Capacitance	f = 1 MHz, V _{BIAS} = 0 V	5/−5		62		pF
C _S (On), C _D (On)	On Capacitance	f = 1 MHz, V _{BIAS} = 0 V	5/−5		42		pF

(1) Provided by design simulation and lab test, not subject to production test.

Typical Performance Characteristics

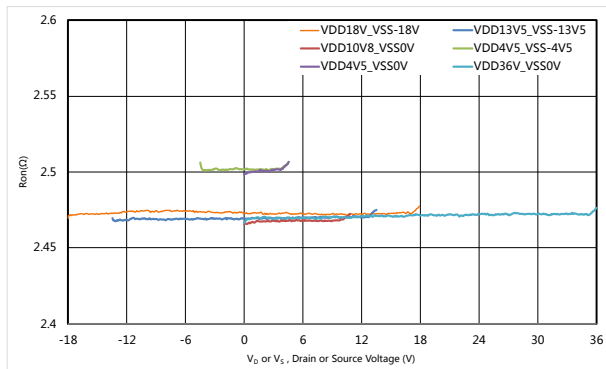


Figure 1. R_{ON} vs V_{DD} , Temp = 25°C

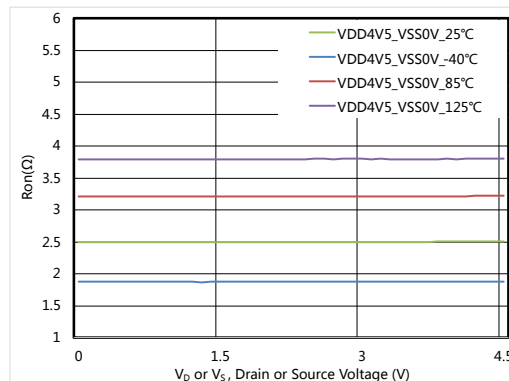


Figure 2. R_{ON} , $V_{DD} = 4.5$ V, $V_{SS} = 0$ V, Temp = -40°C, 25°C, 85°C, 125°C

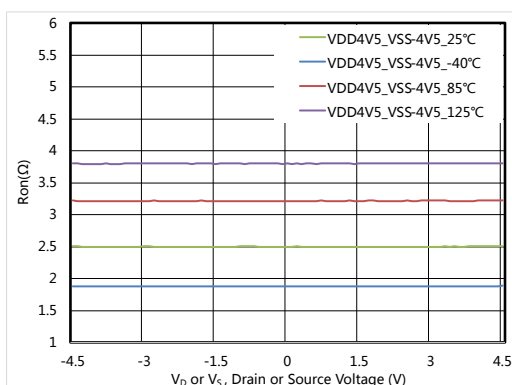


Figure 3. R_{ON} , $V_{DD} = 4.5$ V, $V_{SS} = -4.5$ V, Temp = -40°C, 25°C, 85°C, 125°C

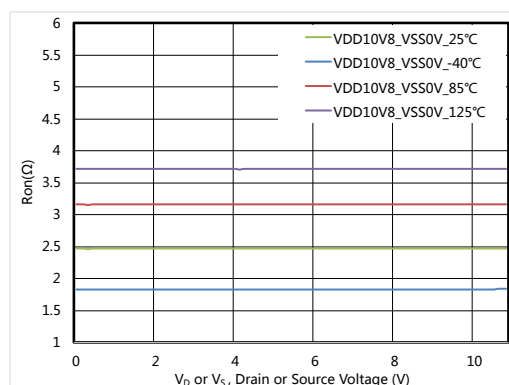


Figure 4. R_{ON} , $V_{DD} = 10.8$ V, $V_{SS} = 0$ V, Temp = -40°C, 25°C, 85°C, 125°C

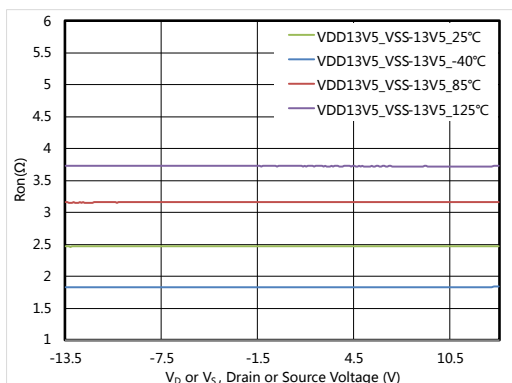


Figure 5. R_{ON} , $V_{DD} = 13.5$ V, $V_{SS} = -13.5$ V, Temp = -40°C, 25°C, 85°C, 125°C

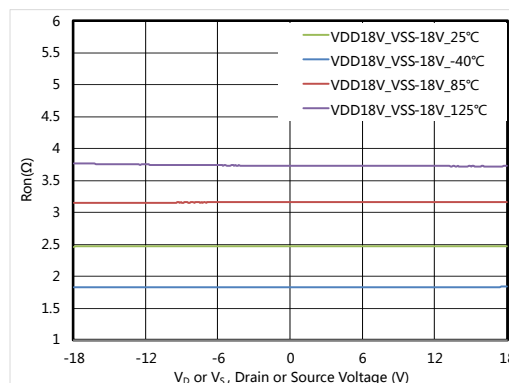


Figure 6. R_{ON} , $V_{DD} = 18$ V, $V_{SS} = -18$ V, Temp = -40°C, 25°C, 85°C, 125°C

High Voltage, Low Leakage SPDT Analog Switch

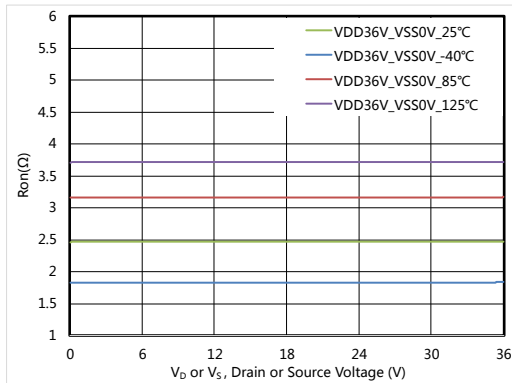


Figure 7. R_{ON} , $V_{DD} = 36\text{ V}$, $V_{SS} = 0\text{ V}$, Temp = -40°C , 25°C , 85°C , 125°C

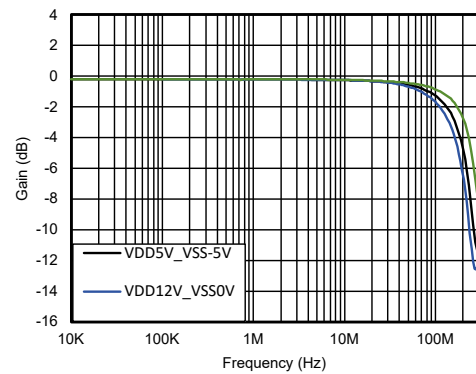


Figure 8. Bandwidth, $V_{DD}/V_{SS} = 5\text{ V}/-5\text{ V}$, $12\text{ V}/0\text{ V}$, $15\text{ V}/-15\text{ V}$

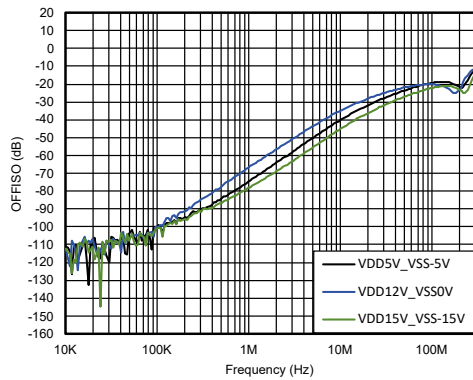


Figure 9. OFFISO, $V_{DD}/V_{SS} = 5\text{ V}/-5\text{ V}$, $12\text{ V}/0\text{ V}$, $15\text{ V}/-15\text{ V}$

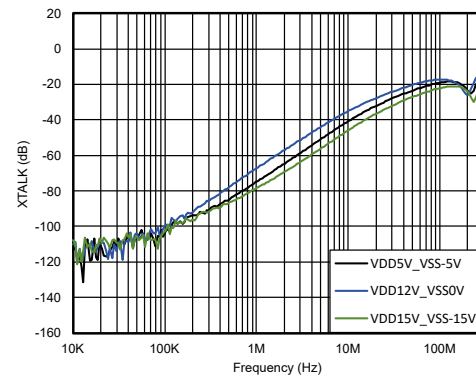


Figure 10. Crosstalk, $V_{DD}/V_{SS} = 5\text{ V}/-5\text{ V}$, $12\text{ V}/0\text{ V}$, $15\text{ V}/-15\text{ V}$

High Voltage, Low Leakage SPDT Analog Switch

Test Circuit and Waveforms

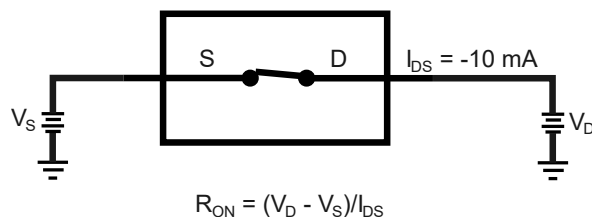


Figure 11. On Resistance

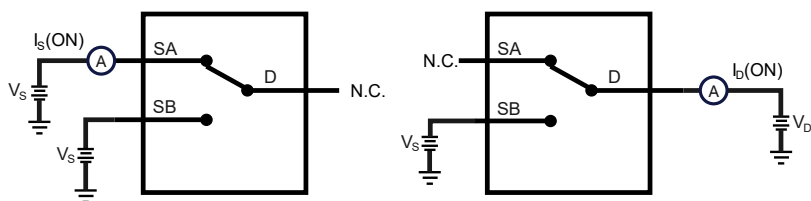


Figure 12. On Leakage

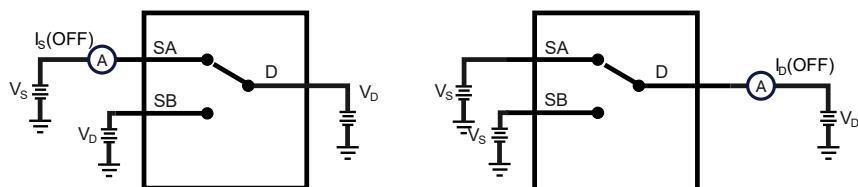


Figure 13. Off Leakage

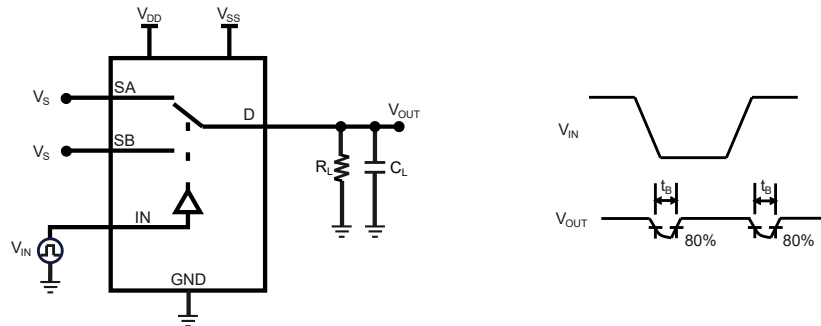


Figure 14. Switch Break Time

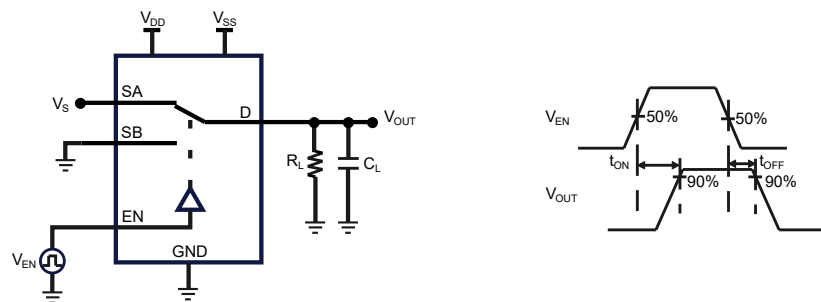


Figure 15. Switching Time

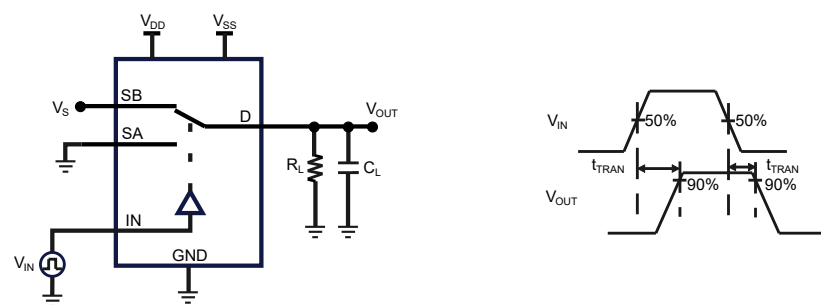


Figure 16. Transition Time

High Voltage, Low Leakage SPDT Analog Switch

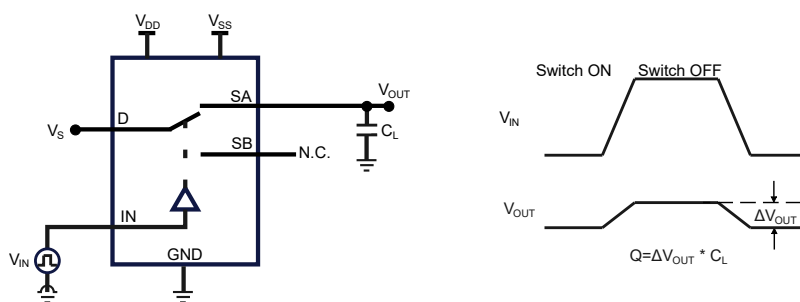


Figure 17. Charge Injection

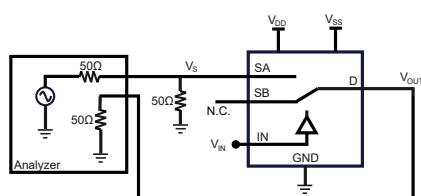


Figure 18. Off Isolation

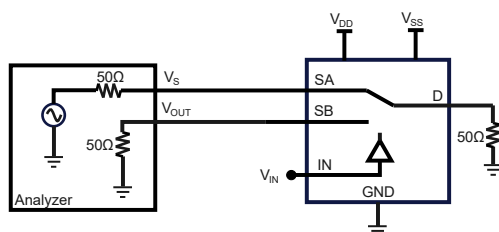


Figure 19. Crosstalk

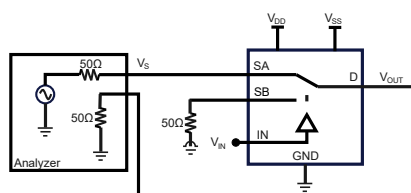


Figure 20. Bandwidth

Application and Implementation

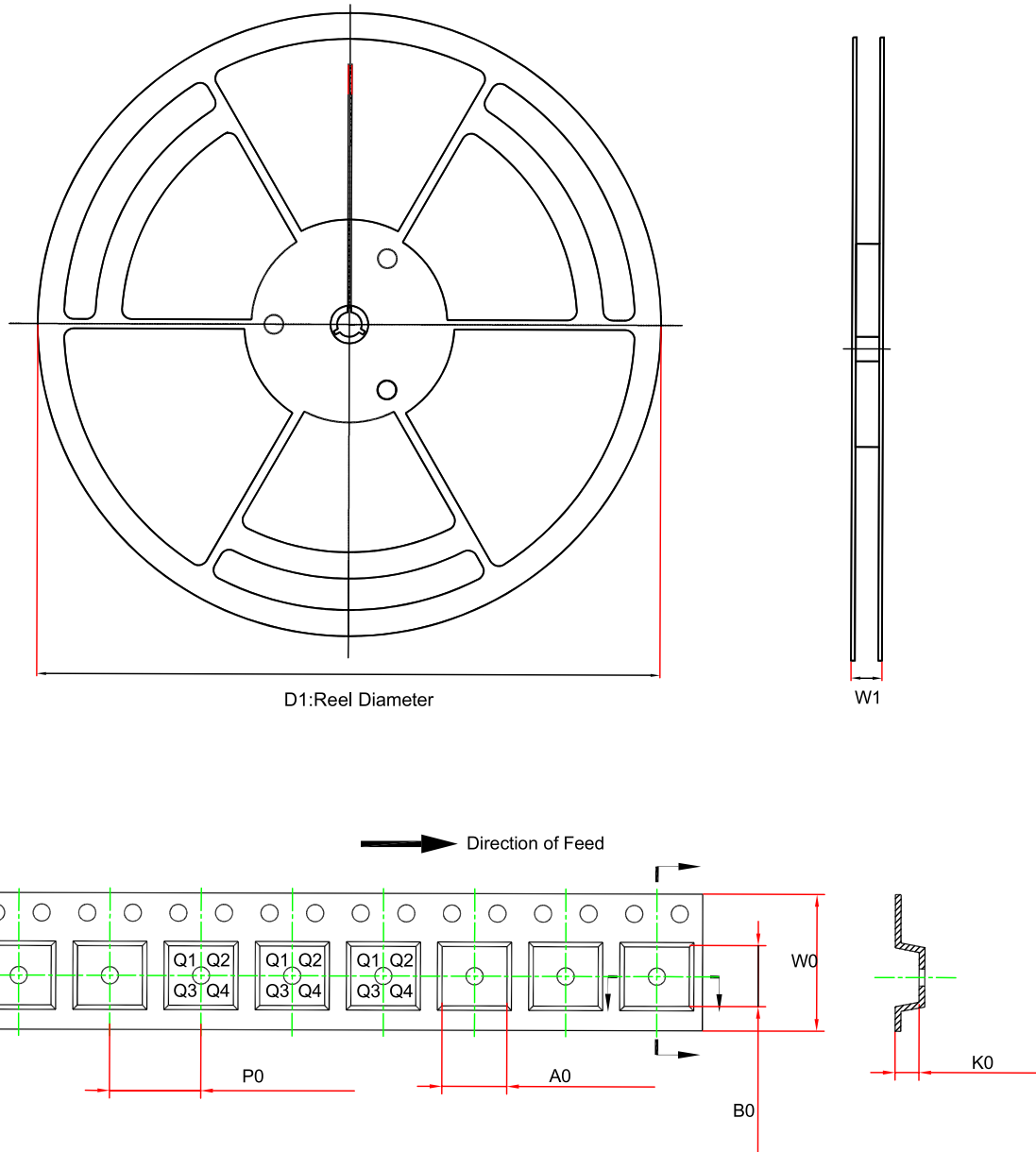
Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

0.1- μ F bypass capacitors on V_{DD} and V_{SS} are recommended to prevent power disturbance.

Tape and Reel Information

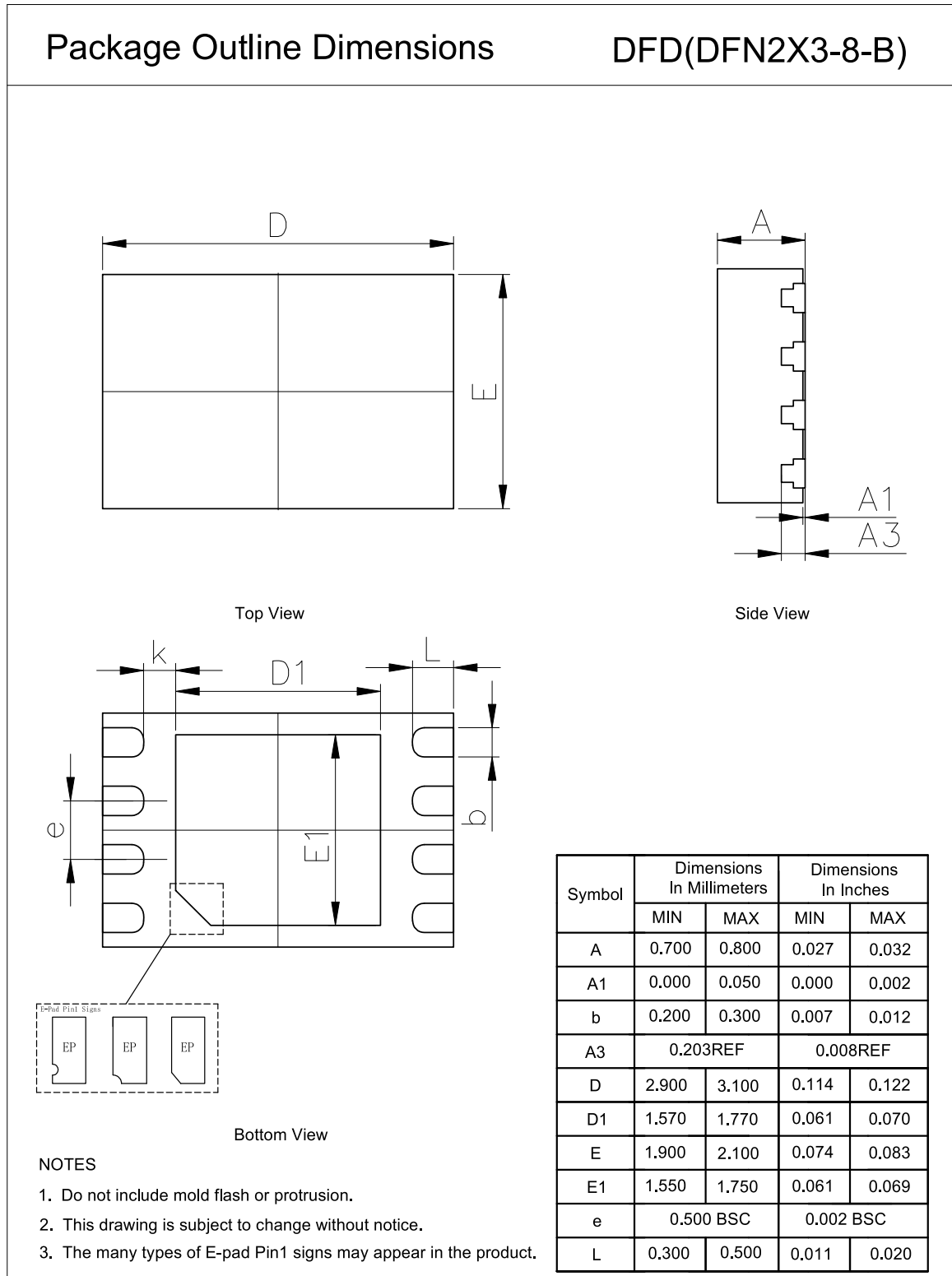


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) ⁽¹⁾	B0 (mm) ⁽¹⁾	K0 (mm) ⁽¹⁾	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPW6124-DFDR-S	DFN2X3-8	180.0	12	3.3	2.3	0.95	4.0	8.0	Q1

(1) The value is for reference only. Contact the 3PEAK factory for more information.

Package Outline Dimensions

DFN2X3-8



Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPW6124-DFDR-S	-40 to 125°C	DFN2X3-8	W24	MSL3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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