

Features

- AEC-Q100 Qualified for Automotive Applications, Grade 1: −40°C to 125°C T_A
- Analog Switch Voltage: 1.8 V, 2.5 V, 3.3 V, 5 V
- Low ON-State Resistance:
 - Typical 75 Ω at Vs = 5 V
 - Typical 120 Ω at Vs = 3.3 V
 - Typical 650 Ω at Vs = 1.8 V
- Bandwidth: 250 MHz
- Fast Switching Times: t_{ON} = 22 ns, t_{OFF} = 8 ns
- Break-before-Make Switching
- TPW3188Q P2P with the Industry Version TPW4051

Applications

- Automotive
- Industry Control Systems
- · Battery-Powered Systems
- Instrumentation

Description

The TPW3188Q is a single-pole octal-throw analog switch (SP8T) suitable for analog or digital 8:1 multiplexer/demultiplexer applications. The switch features three digital select inputs (S0, S1, and S2), eight independent inputs/outputs (An), a common input/output (A), and a digital enable input (/EN). When /EN is HIGH, the switches are turned off.

The device is designed on an enhanced process that provides lower power dissipation and gives high switching speeds. These devices can operate equally well as either multiplexers or de-multiplexers and have an input range that extends to the supplies. All channels exhibit breakbefore-make switching action, preventing momentary shorting when switching channels.

The TPW3188Q is available in the TSSOP-16 and QFN2.5X3.5-16 packages, and is characterized from -40° C to $+125^{\circ}$ C.

Typical Application Circuit

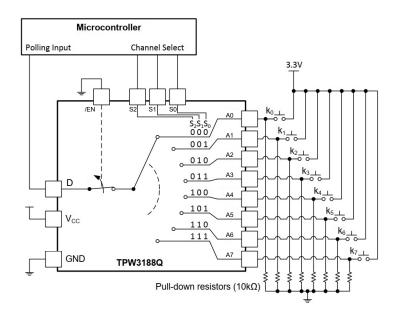




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Revision History

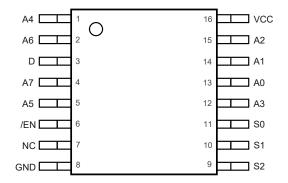
Date	Revision	Notes
2023-05-28	Rev. A.0	Released version.
2023-07-10	Rev. A.1	 Added I_{GND}, I_{OK}, and P_{tot} parameters in the table of Absolute Maximum Ratings. Added LU parameter in the table of ESD, Electrostatic Discharge Protection.
2024-12-29	Rev. A.2	Added part number: TPW3188Q-QN4R-S, TPW3188AQ-TS3R-S. The following updates are all about the new datasheet formats or typos, and the actual product remains unchanged. Adjusted some description. Updated the Tape and Reel Information.

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Pin Configuration and Functions

TPW3188Q TSSOP16 Package Top View



TPW3188Q QFN2.5x3.5-16 Package Top View

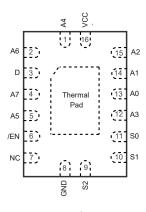


Table 1. Pin Functions: TPW3188Q

Pin No.	Name	I/O	Description
1	A4	I/O	Channel 4 input or output
2	A6	I/O	Channel 6 input or output
3	D	I/O	Common input or output
4	A7	I/O	Channel 7 input or output
5	A5	I/O	Channel 5 input or output
6	/EN	I	Enable switches, active low
7	NC		Not Connected
8	GND		Ground
9	S2	I	Control Input
10	S1	ı	Control Input
11	S0	I	Control Input
12	A3	I/O	Channel 3 input or output
13	A0	I/O	Channel 0 input or output
14	A1	I/O	Channel 1 input or output
15	A2	I/O	Channel 2 input or output
16	Vcc		Positive Power Input

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Table 2. Functional Table

/EN, Enable	S2	S1	S0	ON Channel
L	L	L	L	A0
L	L	L	Н	A1
L	L	Н	L	A2
L	L	Н	Н	A3
L	Н	L	L	A4
L	Н	L	Н	A5
L	Н	Н	L	A6
L	Н	Н	Н	A7
Н	Х	Х	Х	None

⁽¹⁾ X = Don't care

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Specifications

Absolute Maximum Ratings (1)

	Parameter	Min	Max	Unit
Vcc	Supply Voltage	-0.5	6	V
V_S or V_D	Analog Switch Voltage, V _S = Voltage of Ax, V _D = Voltage of D	-0.5	V _{CC} +0.5	V
Icc	Analog Switch Current	-25	+25	mA
Icci	Digital Input Current, /EN, S2, S1, S0	-30	+30	mA
V_{DI}	Digital Input Voltage, /EN, S2, S1, S0	GND	V _{CC} +0.5	V
I _{GND}	Continuous Current through GND	-100	+100	mA
Іок	Current per input into source or drain pins when single voltage exceeds recommended operating voltage	-50	0	mA
P _{tot}	Total Power Dissipation		500	mW
T _C	Maximum Junction Temperature		150	°C
Ts	Storage Temperature Range	-65	150	°C
TL	Lead Temperature (Soldering, 10 sec)		260	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
НВМ	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV
LU	Latch up	LU, per JESD78, All Pin (3)	±100	mA

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- (3) Test at the temperature of 25°C.

Recommended Operating Conditions (1)

	Parameter	Min	Max	Unit
Vcc	Supply Voltage, V _{CC}	1.65	5.5	V
V _S or V _D	Analog Switch Voltage, V _S = Voltage of Ax, V _D = Voltage of D	0	Vcc	V
Vı	Select Input Voltage	0	Vcc	V
T _{R/F}	Input Transition Rise and Fall Rate		100	ns/V
V _{IO}	Switch I/O Port Voltage	0	Vcc	V
T _A	Operating Temperature Range	-40	125	°C

⁽¹⁾ Input select must be held HIGH or LOW and it shouldn't float.

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Thermal Information

Package Type	θ _{JA}	θ _{JC}	Unit
TSSOP16	150	70	°C/W
QFN2.5X3.5-16	70	69	°C/W

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Electrical Characteristics

All test conditions: $T_A = -40$ °C to 125°C, unless otherwise noted.

	Parameter	Test Conditions	vcc	Min	Тур	Max	Units
Analog	Switch						
			1.8 V 2.5 V ⁽¹⁾		650	2100	-
Ron	On-state Switch Resistance	$V_{IS} = 0 \text{ V to } V_{CC}$			230	900	Ω
	Switch Resistance	I _{OS} = 0.5 mA	3.3 V		120	370	-
			5 V ⁽¹⁾		75	270	
	On-state Switch		1.8 V		10	45	-
ΔR_{ON}	Resistance Matching	$V_{IS} = V_{CC} / 2$	2.5 V ⁽¹⁾		3	22	Ω
	between Inputs	I _{OS} = 0.5 mA	3.3 V		2	15	
			5 V ⁽¹⁾		1	14	
		Switch Off	1.8 V	-800	±1	800	
I _{A(OFF)}	Source Off State	Switch Off $V_{OS} = 0.8 \times V_{CC} / 0.2 \times V_{CC}$	2.5 V	-800	±1	800	nA
IA(OFF)	Leakage Current	$V_{IS} = 0.2 \times V_{CC} / 0.8 \times V_{CC}$	3.3 V	-800	±1	800	
			5 V	-800	±1	800	
	Drain Off State Leakage Current (Common Drain Pin)		1.8 V	-800	±1	800	nA
		Switch Off	2.5 V	-800	±1	800	
I _{D(OFF)}		$V_{OS} = 0.8 \text{ x } V_{CC} / 0.2 \text{ x } V_{CC}$ $V_{IS} = 0.2 \text{ x } V_{CC} / 0.8 \text{ x } V_{CC}$	3.3 V	-800	±1	800	
		710 01 <u>2</u> X 700 Y 010 X 700	5 V	-800	±1	800	
			1.8 V	-800	±1	800	nA
$I_{D(ON)}$	Channel On State	Switch On	2.5 V	-800	±1	800	
I _{A(ON)}	Leakage Current	$V_{OS} = V_{IS} = 0.8 \text{ x } V_{CC} \text{ or}$ $V_{OS} = V_{IS} = 0.2 \text{ x } V_{CC}$	3.3 V	-800	±1	800	
		VOS - VIS - 0.2 X VCC	5 V	-800	±1	800	
			1.8 V		4.5	14	
•	Source off	$V_{IS} = V_{CC} / 2$	2.5 V		4.5	14	1
C _{AOFF}	Capacitance (1)	f = 1 MHz	3.3 V		4	14	pF
			5 V		5	14	
			1.8 V		15	37	
	Drain off	V _{IS} = V _{CC} / 2	2.5 V		15	37	_
C_{DOFF}	Capacitance (1)	f = 1 MHz	3.3 V		14	37	pF
			5 V		14	37	
C _{AON}	On Capacitance ⁽¹⁾	V _{IS} = V _{CC} / 2 f = 1 MHz	1.8 V ~ 5 V		20	40	pF

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	Parameter	Test Conditions	vcc	Min	Тур	Max	Units
Power \$	Supply		<u> </u>				
			1.8 V			1.2	
	V 0 1 0 1		2.5 V			1.5	
Icc	V _{CC} Supply Current	Logic inputs = 0 V or V _{CC}	3.3 V			2	− uA
			5 V			3	
Logic Ir	nputs						
			1.8 V	1.05		5.5	
/	Input Logio Lligh		2.5 V	1.12		5.5	
V _{IH}	Input Logic High		3.3 V	1.18		5.5	V
			5V	1.25		5.5	
			1.8V	0		0.6	
.,	lancet Landa Lacc		2.5 V	0		0.65	
VIL	Input Logic Low		3.3 V	0		0.7	V
			5 V	0		0.75	
I _{IH}	Logic High Input Leakage Current	V _{LOGIC} = 1.8 V or V _{CC}	all			1	uA
I _{IL}	Logic Low Input Leakage Current	V _{LOGIC} = 0 V	all	-1			uA
C _{IN}	Logic Input Capacitance	V _{LOGIC} = 0 V, 1.8 V, V _{CC} f = 1 MHz	all		2		pF
Dynami	ic Characteristics				1		
			1.8 V		8		
	Observed Indication (1)	$V_{IS} = V_{CC} / 2 RS = 0 \Omega, C_L =$	2.5 V		8		
Qinj	Charge Injection (1)	100 pF	3.3 V		10		pC
			5 V		15		
		$V_{BIAS} = V_{CC} / 2$	1.8 V		-110		
	OFF 11-# (1)	V _{IS} = 200 mVpp	2.5 V		-110		-ID
O _{ISO}	OFF-Isolation (1)	$R_L = 50 \Omega$, $C_L = 5 pF$	3.3 V		-110		dB
		f = 100 kHz	5 V		-110		
		V _{BIAS} = V _{CC} / 2	1.8 V		-90		
	055 1 1 (1)	$V_{IS} = 200 \text{ mVpp}$	2.5 V		-90		
O _{ISO}	OFF-Isolation (1)	$R_L = 50 \Omega$, $C_L = 5 pF$	3.3 V		-90		dB
		f = 1 MHz	5 V		-90		1
		V _{BIAS} = V _{CC} / 2	1.8 V		-110		
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	0 (1)	V _{IS} = 200 mVpp	2.5 V		-110]
XTALK	Crosstalk (1)	$R_L = 50 \Omega$, $C_L = 5 pF$	3.3 V		-110		dB -
		f = 100 kHz	5 V		-110		
XTALK	Crosstalk (1)	V _{BIAS} = V _{CC} / 2	1.8 V		-90		dB

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	Parameter	Test Conditions	vcc	Min	Тур	Max	Units	
		V _{IS} = 200 mVpp	2.5 V		-90			
		$R_L = 50 \Omega$, $C_L = 5 pF$	3.3 V		-90			
		f = 1 MHz	5 V		-90			
			1.8 V		250			
	D (1)	$V_{BIAS} = V_{CC} / 2$	2.5V		250] <u>-</u>	
BW	Bandwidth ⁽¹⁾	$V_{IS} = 200 \text{ mVpp}$ $R_L = 50 \Omega, C_L = 5 \text{ pF}$	3.3 V		250		MHZ	
		π = 30 12, 0[= 3 μι	5 V		250			
Switchin	g Characteristics (Timing Chara	acteristics)		1	1		'	
			1.8 V		15	30		
		C _L = 50 pF	2.5 V		8	20		
t _{PD}	Propagation Delay (2)	Ax to D, D to Ax	3.3 V		5	15	ns	
			5 V		4	10		
		C _L = 15 pF ⁽¹⁾	5 V		1.5	5	-	
	Transition-time between Inputs (2)		1.8 V		44	103	ns	
t _{TRAN}		R_L = 10 kΩ, C_L = 50 pF Sx to D, Sx to Ax	2.5 V		30	67		
		SX to D, SX to AX	3.3 V		23	54		
t _{TRAN}	Transition-time between Inputs	$R_L = 10 \text{ k}\Omega, C_L = 50 \text{ pF}$ Sx to D, Sx to Ax	5 V		18	46	ns	
	(2)	$R_L = 10 \text{ k}\Omega, C_L = 15 \text{ pF}^{(1)}$	5 V		15	43		
			1.8 V		39	75		
		$R_L = 10 \text{ k}\Omega, C_L = 50 \text{ pF}$	2.5 V		30	50	ns	
t _{ON(EN)}	Turn on-time from Enable (2)	EN to D, EN to Ax	3.3 V		26	42		
			5 V		24	37		
		$R_L = 10 \text{ k}\Omega, C_L = 15 \text{ pF}^{(1)}$	5 V		22	35		
			1.8 V		58	85		
		$R_L = 10 \text{ k}\Omega, C_L = 50 \text{ pF}$	2.5 V		21	72		
t _{OFF(EN)}	Turn off Time from Enable (2)	EN to D, EN to Ax	3.3 V		15	70	ns	
			5 V		11	45		
		$R_L = 10 \text{ k}\Omega, C_L = 15 \text{ pF}^{(1)}$	5		8	20		
			1.8 V	1	16			
. (1)	Dural hafana maalaa tiiraa (1)	$R_L = 10 \text{ k}\Omega, C_L = 15 \text{ pF}$	2.5 V	1	22		1	
t _{BBM} (1)	Break before make time ⁽¹⁾	Ax to D, D to Ax	3.3 V	1	24		ns	
			5 V	1	33			

⁽¹⁾ Provided by bench test and design simulation.

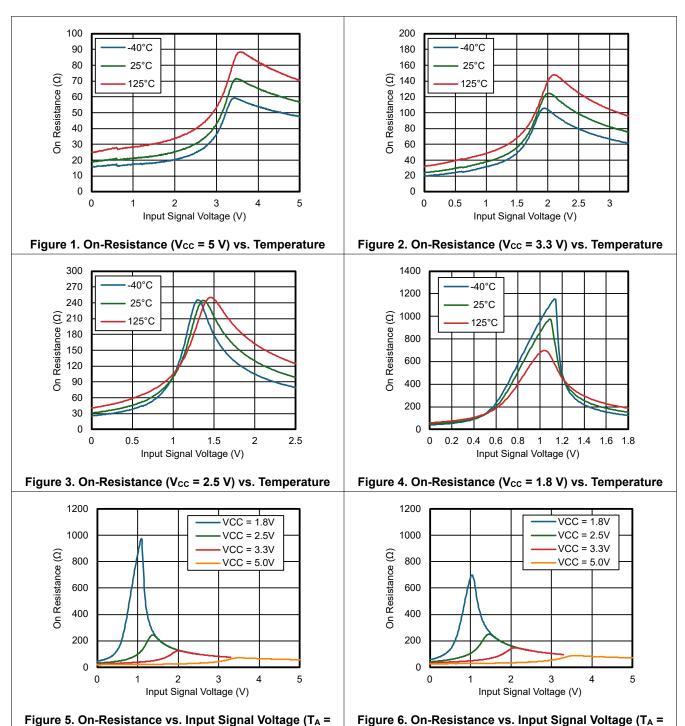
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 $^{(2) \} For \ TPW3188AQ-TS3R-S \ and \ TPW3188Q-QN4R-S, \ provided \ by \ bench \ test \ and \ design \ simulation.$



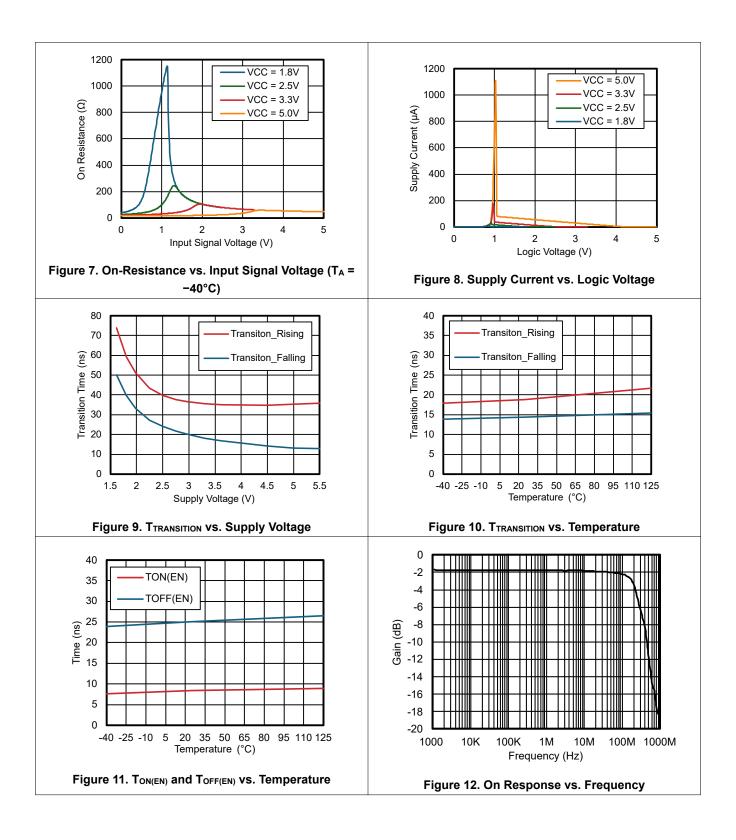
Typical Performance Characteristics

All test conditions: T_A = 25°C, VCC = 5 V, unless otherwise noted.

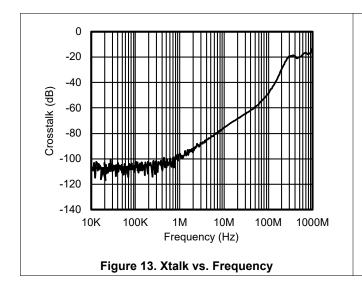


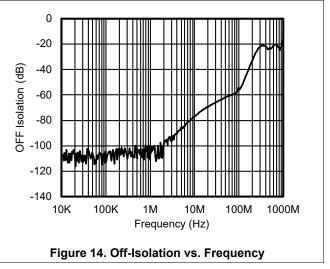
125°C)













Test Circuits and Waveforms

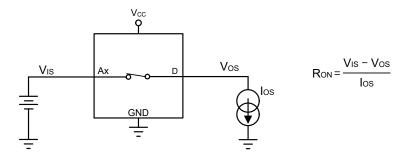


Figure 15. On-Resistance Measurement Setup

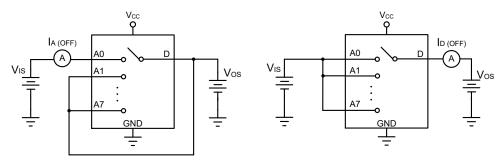


Figure 16. Off-Leakage Measurement Setup

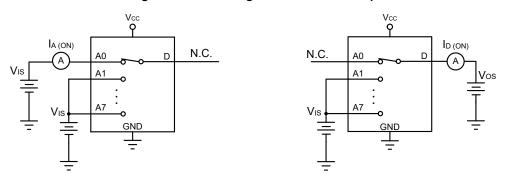


Figure 17. On-Leakage Measurement Setup

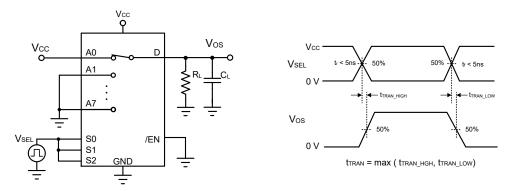


Figure 18. Transition-Time Measurement Setup

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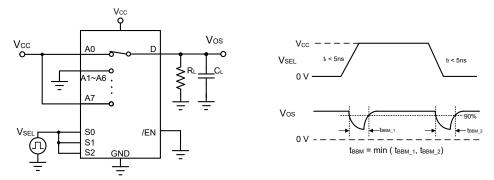


Figure 19. Break-Before-Make Delay Measurement Setup

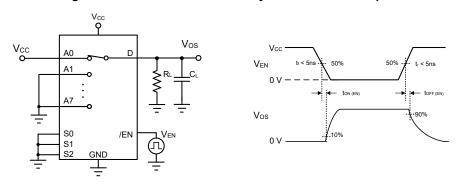


Figure 20. Turn-On and Turn-Off Time Measurement Setup

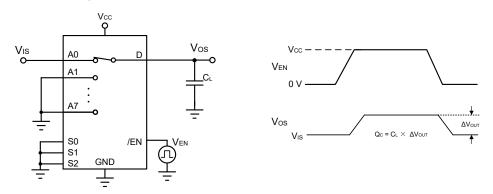


Figure 21. Charge-Injection Measurement Setup

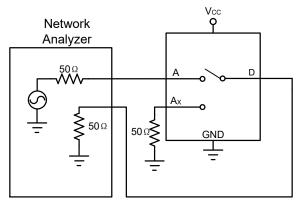


Figure 22. Off Isolation Measurement Setup

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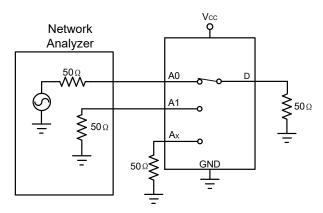


Figure 23. Channel-to-Channel Crosstalk Measurement Setup

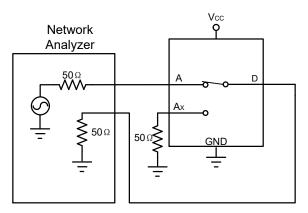


Figure 24. Bandwidth Measurement Setup

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Detailed Description

Overview

The TPW3188Q is a single-pole octal-throw analog switch (SP8T) suitable for analog or digital 8:1 multiplexer/demultiplexer applications. The switch features three digital select inputs (S0, S1, and S2), eight independent inputs/outputs (An), a common input/output (A), and a digital enable input (/EN). When /EN is HIGH, the switches are turned off.

Functional Block Diagram

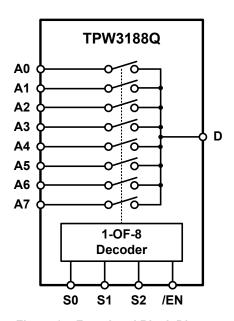


Figure 25. Functional Block Diagram

Feature Description

The TPW3188Q is the automotive analog switch qualified as AEC Q100 - automotive grade 1. The VCC voltage range is 1.8 V, 2.5 V, 3.3 V, and 5 V. The Ron resistance is very low, such as typical 75 Ω at Vs = 5 V, typical 120 Ω at Vs = 3.3 V, and typical 650 Ω at Vs = 1.8 V. The TPW3188Q bandwidth is 250 MHz, it is in a break state before the switch operation. The switching time is very fast, which is 22 ns in the ON state, and 8 ns in the OFF time.

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Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPW3188Q line of multiplexers and demultiplexers can be used for a wide variety of applications.

A $0.1-\mu F$ bypass capacitor on V_{CC} is recommended to prevent power disturbance.

The current per input into source or drain pin when input signal voltage exceeds Vcc

As the input signal voltage is higher than the V_{CC} voltage, the current per input into source or drain can be very large and close to 50 mA, which may damage the device. Therefore, the input signal is not recommended to exceed V_{CC} .

Input signal voltage should be less than V_{CC} + 0.5 V

The TPW3188Q has an internal ESD diode to the GND pin, which is around 20 mA as the diode is turned on. The input signal voltage should NOT be lower than GND-0.5V. Resistors are suggested to be added to limit the current. The device requires the input signal voltage to be less than V_{CC} + 0.5 V. Otherwise, the current increases in exponential magnitude as the input signal voltage rises higher than V_{CC} + 0.5 V. Thus, the function cannot be guaranteed in the application, and the device may be damaged.

In some special cases, if the input signal voltage exceeds VCC as the channel is OFF, the voltage is clamped to VCC + 0.7 V approximately. The input current may be as large as tens of mA and introduces coupling to other channels, so the device is not recommended in this case.

Typical Application

One application of the TPT3188Q device is used in conjunction with a microcontroller to poll a keypad. Figure 26 shows the basic schematic for such a polling system.

The microcontroller uses channel-select pins to cycle through different channels while reading the input to see if a user is pressing any of the keys. This is a very robust setup that allows for simultaneous key presses with very little power consumption. It also uses very few pins on the microcontroller. The downside of polling is that the microcontroller must frequently scan the keys for a press.

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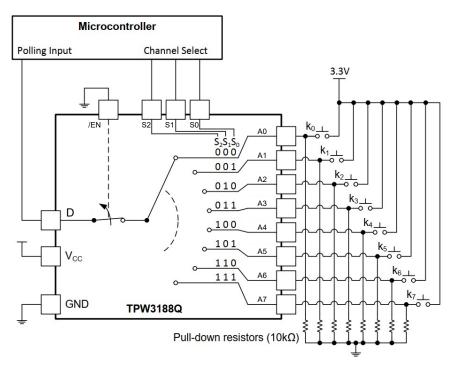


Figure 26. Typical Application Circuit

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Layout

Layout Example

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they have to turn corners. Figure 27 shows progressively better techniques for rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

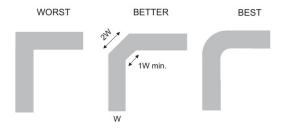


Figure 27. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 28 illustrates an example of a PCB layout with the TPW3188Q. Some key considerations are:

- Decouple the V_{CC} pin with a 0.1-µF capacitor, and place as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{CC} supply.
- · Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible and only make perpendicular crossings when necessary.

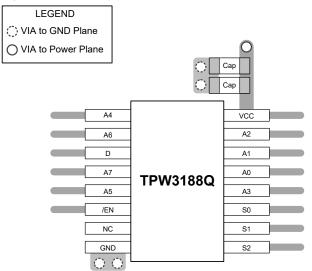
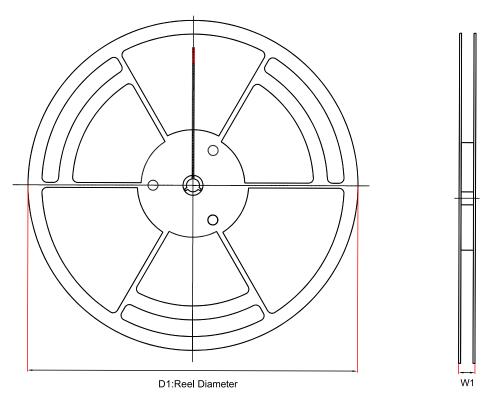


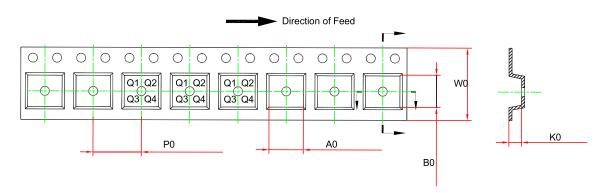
Figure 28. TPW3188Q Layout Example

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Tape and Reel Information





Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) ⁽¹⁾	B0 (mm) ⁽¹⁾	K0 (mm) ⁽¹⁾	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPW3188Q-TS3R-S	TSSOP16	330	17.6	6.8	5.5	1.5	8	12	Q1
TPW3188AQ-TS3R-S	TSSOP16	330	17.6	6.8	5.5	1.5	8	12	Q1
TPW3188Q-QN4R-S	QFN2.5X3.5-16	330	17.6	2.75	3.75	1.0	4	12	Q1

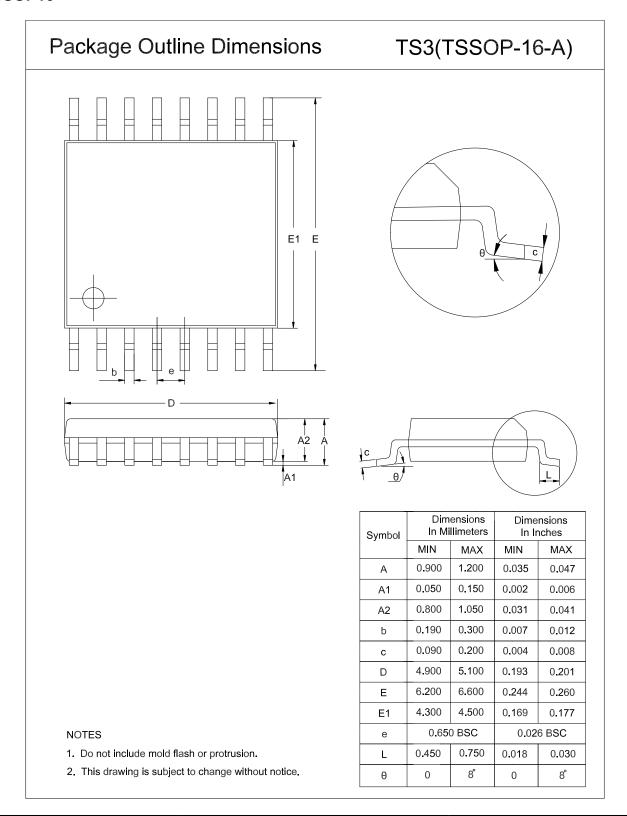
⁽¹⁾ The value is for reference only. Contact the 3PEAK factory for more information.

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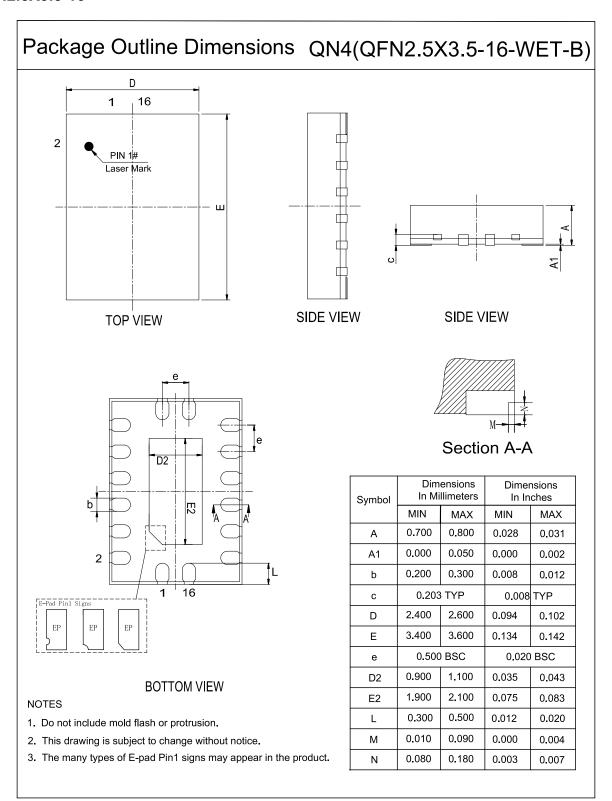
Package Outline Dimensions

TSSOP16





QFN2.5X3.5-16





Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPW3188Q-TS3R-S	−40 to 125°C	TSSOP16	3188Q	MSL1	Tape and Reel, 3000	Green
TPW3188AQ-TS3R-S	-40 to 125°C	TSSOP16	3188AQ	MSL1	Tape and Reel, 3000	Green
TPW3188Q-QN4R-S	-40 to 125°C	QFN2.5X3.5-16	38Q	MSL2	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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