2/4-Channel High-Side Power Switch for Automotive Camera Modules

Features

- Qualified for Automotive Applications
  - AEC-Q100 Grade 1, T_A: −40°C to +125°C
  - Junction Temperature, T_J: −40°C to +150°C
- Input Voltage Range
  - Power Supply, VDD: 3 V to 5.5 V
  - Input Voltage, VIN: 3 V to 15 V
- 400-mΩ Low Turn-On Resistance
- Up to 2/4 Output Channels
  - Parallel Multiple Channels for Higher Current
- Adjustable Current Limit
  - from 18 mA to 672 mA for Each Channel
  - 8% Current Limit Accuracy
  - Iset Pin and Dedicate Register to Configure
- Very Low Standby Current: < 0.4 uA
- Current and Voltage Readable with 8-Bit 1-MHz I2C Interface
- Functional Safety ASIL-B Compliant
- Fault Diagnosis
  - Short to Battery and Short to Ground Diagnostics
  - Input Over/Undervoltage Diagnostics
  - Differential Output Over/Undervoltage Diagnostics
- Protection
  - Output Short to Battery Protection
  - Over Current and Short to Ground Protection
  - Over Temperature Protection
- Package Option
  - QFN4X4-20 Package with Exposed Pad

Applications

- Off -Board Load Power Supply
- Power-over-Coax for Radar and Camera Modules
- Automotive infotainment, Navigation, Telematics
- Automotive ADAS, Surround-View Cameras

Description

The TPW20400xQ is a 400-mΩ 2/4-channel high-side isolation/protection power switch series with internal current limiting and diagnostics. The TPW20400xQ is AEC-Q100 qualified and can increase the diagnostic coverage to achieve ASIL-B compliance.

The TPW20400xQ input voltage operating range is from 3 V to 15 V, with an absolute maximum rating of 20 V. The VDD range is from 3 V to 5.5 V, with an absolute maximum rating of 6 V.

The TPW20400xQ is equipped with high-precision current sensing capabilities. It offers a current sense accuracy of ±8% from 300 mA to 600 mA. This accurate current sensing enables easy identification of load status and measurement of load current.

The TPW20400xQ integrates full fault diagnostics and device protection to prevent the device damage from short-circuit to the battery, short-circuit to ground, input over/under voltage, output over/under voltage, over current and over temperature.

The TPW20400xQ provides and enables input and I^2C interface to read the diagnostic status of the device. It integrates an 8-bit ADC to read the current of each channel. The current limit ratio can also be configured, and the status, including OTP warning, can be read for each channel through the I^2C interface. Each channel can also be turned on/off by I^2C.

The TPW20400xQ is designed to operate within the ambient temperature range from −40°C to +125°C.

Typical Application Circuit

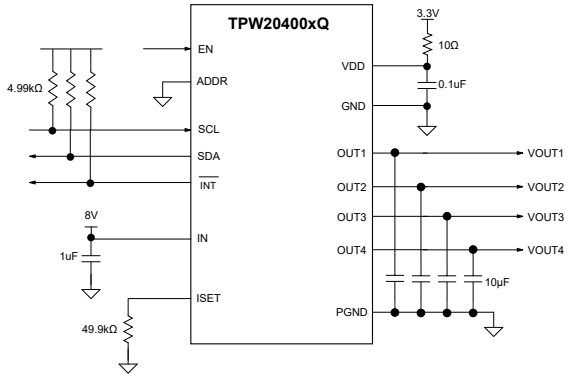


Table of Contents

Product Family Table

Order Number	Operating Voltage Range (V)	Channel #	I²C (ADDR=0)	Option	Package
TPW20400QQ-QFOR-S	3 to 5.5	4	0x28	-	QFN4X4-20
TPW20400QBQ-QFOR-S (1)	3 to 5.5	4	0x2A	-	QFN4X4-20
TPW20400QCQ-QFOR-S (1)	3 to 5.5	4	0x2C	-	QFN4X4-20
TPW20400QAQ-QFOR-S	3 to 5.5	4	0x28	ASIL-B	QFN4X4-20
TPW20400QABQ-QFOR-S (1)	3 to 5.5	4	0x2A	ASIL-B	QFN4X4-20
TPW20400QACQ-QFOR-S (1)	3 to 5.5	4	0x2C	ASIL-B	QFN4X4-20
TPW20400QDQ-QFOR-S (1)	3 to 5.5	4	0x28	-	QFN4X4-20
TPW20400QDAQ-QFOR-S (1)	3 to 5.5	4	0x28	ASIL-B	QFN4X4-20
TPW20400DQ-QFOR-S	3 to 5.5	2	0x28	-	QFN4X4-20
TPW20400DBQ-QFOR-S (1)	3 to 5.5	2	0x2A	-	QFN4X4-20
TPW20400DCQ-QFOR-S (1)	3 to 5.5	2	0x2C	-	QFN4X4-20
TPW20400DAQ-QFOR-S	3 to 5.5	2	0x28	ASIL-B	QFN4X4-20
TPW20400DABQ-QFOR-S (1)	3 to 5.5	2	0x2A	ASIL-B	QFN4X4-20
TPW20400DACQ-QFOR-S (1)	3 to 5.5	2	0x2C	ASIL-B	QFN4X4-20

(1) For further information, please contact your 3PEAK Sales Representative.

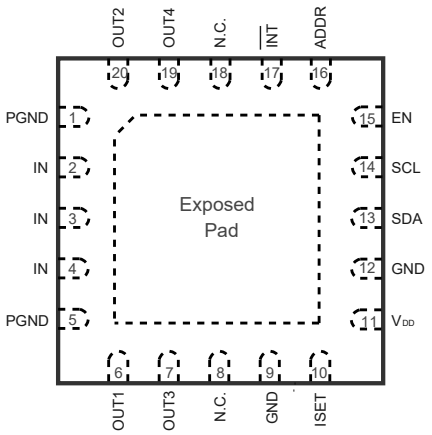
Revision History

Date	Revision	Notes
2026-03-11	Rev.A.0	Initial released.
2026-03-30	Rev.A.1	Corrected typos in the pin configuration and functions. The actual product remains unchanged.
2026-07-02	Rev.A.2	1. Add information for the TPW20400 dual-channel version. 2. Add the ILIM calculation formula.

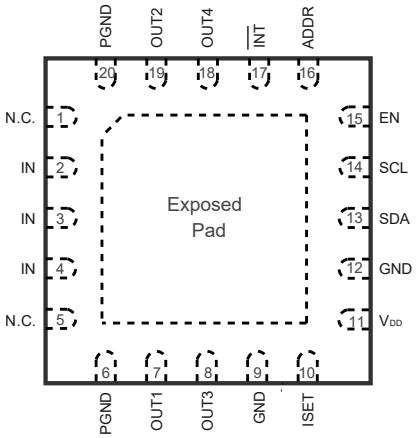
Date	Revision	Notes
		3. Update typical application diagrams.

Pin Configuration and Functions

TPW20400QQ/QAQ/QBQ/QABQ/QCQ/QACQ-QFOR-S
QFN4X4-20
Top View



TPW20400QDQ/QDAQ-QFOR-S
QFN4X4-20
Top View



TPW20400DQ/DBQ/DCQ/DAQ/DABQ/DACQ-QFOR-S

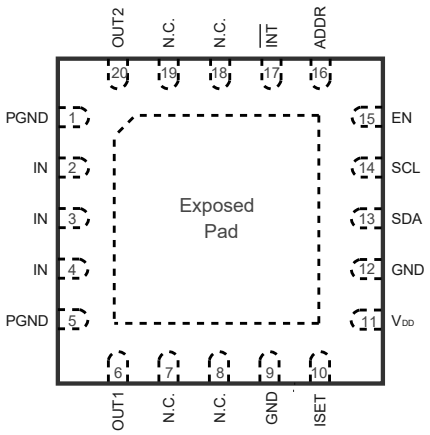


Table 1. Pin Functions: TPW20400xQ-QFOR-S

Pin No.			Name	Description
TPW20400QQ/QBQ/QCQ/QAQ/QABQ/QACQ-QFOR-S	TPW20400QDQ/QDAQ-QFOR-S	TPW20400DQ/DBQ/DCQ/DAQ/DABQ/DACQ-QFOR-S		
2, 3, 4	2, 3, 4	2, 3, 4	IN	Camera Supply. Connect to the output of the DC-DC converter feeding the cameras.

Pin No.			Name	Description
TPW20400QQ/QBQ/QCQ/QAQ/QABQ/QACQ-QFOR-S	TPW20400QDQ/QDAQ-QFOR-S	TPW20400DQ/DBQ/DCQ/DAQ/DABQ/DACQ-QFOR-S		
1, 5	6, 20	1, 5	PGND	Power Ground. Connect GND and PGND together to the exposed pad (EP).
6	7	6	OUT1	Protected Camera Supply Output 1. Connect a 1-μF or larger ceramic capacitor from OUT1 to PGND.
7	8	-	OUT3	Protected Camera Supply Output 3. Connect a 1-μF or larger ceramic capacitor from OUT3 to PGND.
8, 18	1, 5	7, 8, 18, 19	N.C.	Not Connected. Leave unconnected or connect to ground.
9, 12	9, 12	9, 12	GND	Analog Ground.
10	10	10	ISET	Output Current-Limit Setting. Connect a resistor from ISET to GND to set the per-channel current limit.
11	11	11	V_{DD}	Device Input Supply. Connect a 100-nF or larger ceramic capacitor from VDD to GND.
13	13	13	SDA	I^2C Data I/O.
14	14	14	SCL	I^2C Clock Input.
15	15	15	EN	Active-High Enable Input. Drive EN high for normal operation. On the rising edge, the enabled channels (in the CONFIG register) enter soft-start and on the falling edge, the channels turn off.
16	16	16	ADDR	I^2C Address Select. Connect to ground or VDD to select between two different I^2C addresses.
17	17	17	$\overline{INT}$	Active-Low, Open-Drain Interrupt Output. External pullup resistor required
19	18	-	OUT4	Protected Camera Supply Output 4. Connect a 1-μF or larger ceramic capacitor from OUT4 to PGND.
20	19	20	OUT2	Protected Camera Supply Output 2. Connect a 1-μF or larger ceramic capacitor from OUT2 to PGND.

(1) The Exposed Pad **MUST** be connected to the device GND directly.

Specifications

Absolute Maximum Ratings (1) (2) (3)

Parameter	Min	Max	Unit
IN	−0.3	20.0	V
OUT1, OUT2, OUT3, OUT4	−0.3	26.0	V
OUT1, OUT2, OUT3, OUT4 to IN	−20.0	26.0	V
VDD	−0.3	6.0	V
ISET, EN	−0.3	VDD + 0.3	V
SCL, SDA, ADDR, $\overline{INT}$	−0.3	6.0	V
GND to PGND	−0.3	0.3	V
T_J	−40.0	150.0	°C
T_{STG}	−65.0	150.0	°C
T_L		260.0	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.
(3) All absolute negative voltage on these terminals is not to go below −0.3 V.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	AEC Q100-002	±2	kV
CDM	Charged Device Model ESD	AEC Q100-011	±1	kV

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{DD}	Supply Voltage on V_{DD} pin to GND	3	5.5	V
V_{IN}	Supply Voltage on V_{IN}pin to PGND	3	15	V
	Voltage on EN, ISET pins to GND	0	V_{DD}	V
	Voltage on $\overline{INT}$, SDA, SCL, ADDR pins to GND	0	5	V
	Voltage on OUT1, OUT2, OUT3, OUT4 to PGND	0	26	V
T_A	Ambient Temperature Range	−40	125	°C
T_J	Junction Temperature Range	−40	150	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
QFN4X4-20	32.3	10	2	°C/W

Electrical Characteristics

All test conditions: T_A = −40°C to +125°C; typical values at T_A = 25°C, V_{DD} = 5 V, V_{IN} = 6.5 V, over operating free-air temperature range (unless otherwise noted).

Parameter		Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range		3.0		5.5	V
I_{SD}	Supply Shutdown Current	VEN = 0 V, TA = -40°C ~ +125°C		3.0	8.7	μA
I_{VDD}	Supply Current	VEN = 5 V		2.0		mA
V_{DD_UV}	VDD Undervoltage Lockout	Falling	2.7	2.8	2.9	V
		Hysteresis		150.0		mV
V_{DD_OV}	VDD Overvoltage Lockout	Rising	5.5	5.7	5.9	V
		Hysteresis		100.0		mV
V_{IN}	Input Power Voltage Range		3.0		15.0	V
I_{IN}	Input Current	VEN = 0 V, TA = +25°C		0.4		μA
		VEN = 0 V			3.0	μA
		All switches enabled, no load		1.0		mA
V_{IN_UV}	VIN Undervoltage Lockout	Falling	2.5	2.7	2.9	V
		Hysteresis		150.0		mV
V_{IN_OV}	VIN Overvoltage Lockout	Rising	15.8	16.5	17.1	V
		Hysteresis		170.0		mV
R_{ON}	Power MOSFET On Resistance			400.0	700.0	mΩ
t_{ON}	Soft-Start Ramp Time	0mA to ILIM		0.5		ms
t_{OFF}	Soft-Shutdown Ramp Time	From full-on ILIM value to high impedance, any condition that turns off a channel		0.25		ms
V_{REV}	Output Reverse Voltage Threshold	VOUT - VIN, VOUT rising, output disabled	0.09	0.15	0.25	V
t_{REV}	Output Reverse Voltage Blanking Time	Force VOUT 1 V above threshold, for short to VBAT detection		1.0		μs
V_{OUT_UV}	Output Voltage Undervoltage Lockout	VIN - VOUT, VOUT falling	0.45	0.55	0.65	V
		Hysteresis		40.0		mV
t_{OUT_UV}	Output Voltage Undervoltage Lockout Blanking Time	Force VOUT 1 V below threshold		1.0		μs
I_{SET}	ISET Operating Range		72.0		672.0	mA
I_{OUT}	Default Output Current	ISET out of operating range		600.0		mA
I_{SET_PU}	ISET Pullup Current	VISET = 1.25 V	11.9	12.5	13.1	μA
I_{LIM}	Current Limit	VISET = 0.3125 V		150.0		mA
		VISET = 0.625 V		300.0		mA

Parameter		Conditions	Min	Typ	Max	Unit
		VISET = 1.25 V		600.0		mA
V_{STG}	Hard Short Detection Threshold		1.8	1.9	2.0	V
t_{STG}	Hard Short Detection Delay Time	Output in current limit, hard short detected		10.0		ms
t_{SC}	Shorted Output Detection Time	Output in current limit, UV detected		20.0		ms
t_{SC_TRY}	Shorted Output Retry Time		225.0	250.0	275.0	ms
K_{VIN}	VIN Divide Ratio			7.164		V/V
K_{VDD}	VDD Divide Ratio			2.56		V/V
K_{ISET}	VISET Divide Ratio			2.0		V/V
K_{VOUT}	VOUT Divide Ratio			7.164		V/V
K_{IOUT}	IOUT Divide Ratio			0.31		A/V
LSB_V_{IN}	VIN Voltage LSB			70.0		mV
LSB_V_{DD}	VDD Voltage LSB			25.0		mV
LSB_I_{SET}	VIET Voltage LSB			5.0		mV
LSB_V_{OUT}	VOUT Voltage LSB			70.0		mV
LSB_I_{OUT}	IOUT Current LSB			3.0		mA
RES	Resolution			8.0		Bits
INL	Relative Accuracy	Integral Non-Linearity			±1.5	Bits
DNL	Differential Accuracy	Differential Non-Linearity			±1	Bits
OS	Offset Error				±2.2	Bits
t_{CON}	Conversion Time			1.0		ms
t_{ACQU}	Track-and-Hold Acquisition Time			20.0		μs
V_{REF}	Reference	Full-scale reading	1.23	1.25	1.27	V
V_{OL_INT}	INT Output Low Level	VDD = 3 V, ISINK = 2 mA			0.2	V
I_{INT}	INT Leakage Current	ERR, SDA = VDD = 5.5 V			1.0	μA
V_{OL_SDA}	SDA Output Low Level	ISINK = 13 mA			0.4	V
V_{IH}	Input High Level	Rising	1.3			V
V_{IL}	Input Low Level	Falling			0.5	V
V_{HYS}	Hysteresis			100.0		mV
I_{EN}	EN Pulldown Current	VEN = 5 V		1.0		μA
I_{ADDR}	ADDR Pulldown Current	VADDR = 5 V		3.0		μA
I_{LKG}	Leakage of SDA and SCL	0 or 5.5V, VDD = 5.5V, TA = +25°C			1.0	μA
f_{SCL}	Clock Frequency				1.1	MHz
t_{SU_STA}	START Setup Time (Repeated)		260.0			ns
t_{HD_STA}	START Hold Time (Repeated)		260.0			ns

Parameter		Conditions	Min	Typ	Max	Unit
t_{LOW_SCL}	SCL Low Time		350.0			ns
t_{HIGH_SCL}	SCL High Time		260.0			ns
t_{SU_DAT}	Data Setup Time		50.0			ns
t_{HU_DAT}	Data Hold Time		0.0			ns
t_{SU_STOP}	STOP Setup Time		260.0			ns
t_{SP}	Spike Suppression			50.0		ns
TSD	Thermal-Shutdown Threshold			165.0		°C
	Hysteresis			15.0		°C

Typical Performance Characteristics

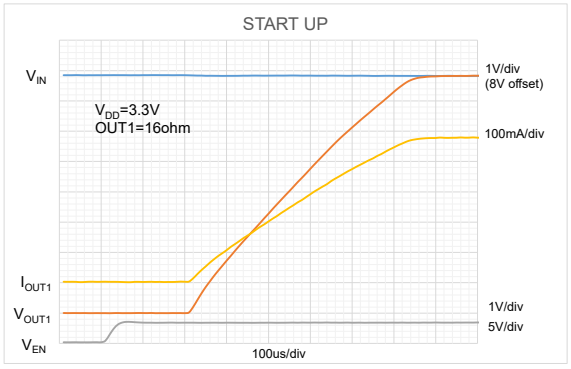


Figure 1. Waveform Output with EN Enabled

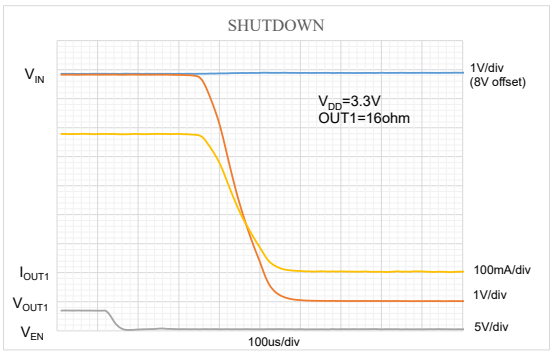


Figure 2. Waveform Output with EN Disabled

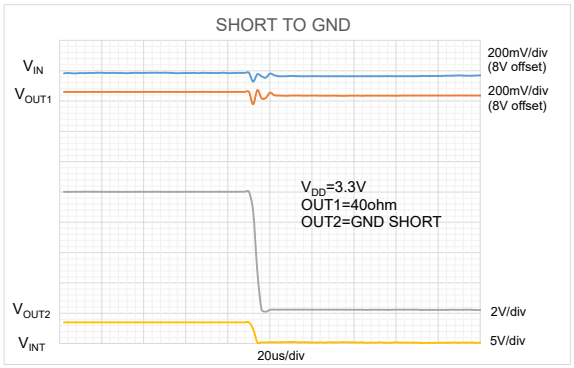


Figure 3. OUT2 Short-To-GND Response

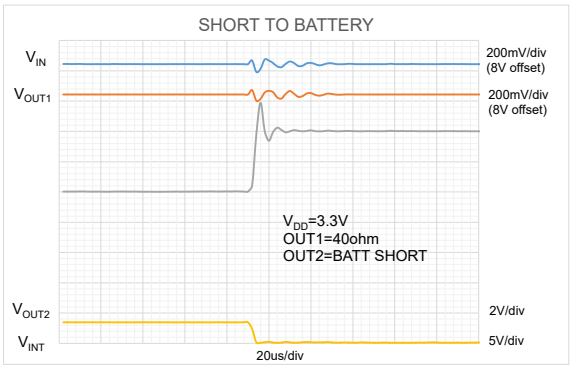


Figure 4. OUT2 Short-To-Battery Response

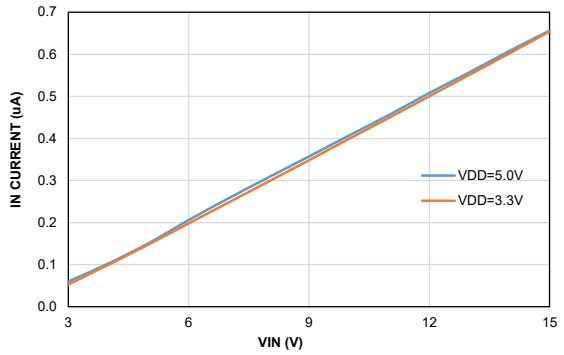


Figure 5. VIN Leakage vs. Voltage

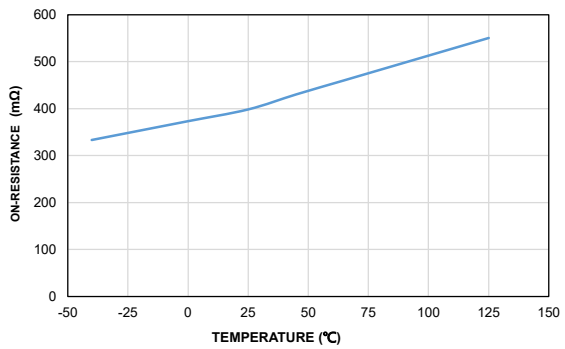


Figure 6. Ron vs. Temperature

Detailed Description

Overview

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The TPW20400xQ is designed to operate within the ambient temperature range from −40°C to +125°C.

Functional Block Diagram

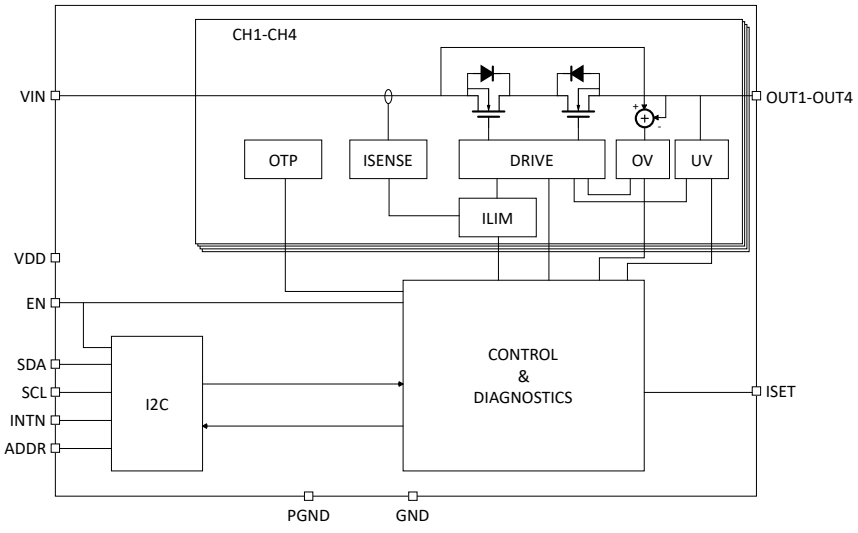


Figure 7. Functional Block Diagram

Feature Description

Adjustable Current Limit (ILIM)

During the power-up phase, each channel behaves approximately as a current source. When the output load has a relatively large equivalent capacitance, each channel operates in a current-limiting state, which means that the chip consumes a higher amount of power at this time. To protect the chip, each channel can only remain in the current-limiting state for a certain

duration; therefore, it is necessary to ensure that the output capacitance is powered up within this time. Several factors determine the minimum current limit setting required for normal operation.

The current limit for each channel can be determined by Equation 1.

$$ILIM = 600mA \times \frac{R_{ISET}}{100K\Omega} \quad (1)$$

The TPW20400 supports parallel use of channels to provide higher output current. When channels are used in parallel, it is recommended to reserve approximately 10% margin to avoid current mismatch between channels.

OV Comparator Diagnostics

The input and output overvoltage comparators can be tested by using the following procedure.

1. Set EN pin = Low
2. Set CONFIG.EN[4:1] = "0"
3. Set EN pin = High
4. IN voltage >IN UV threshold
5. Set MASK.OVTST = "1"
6. Read STAT1 and STAT2 registers and verify that the STAT1.OVIN, STAT1.OVDD, and STAT2.OV[4:1]bits are setto "1" . (The STAT2.UV [4:1] bits are also set, due to disabling the outputs per step 1.)
7. Set MASK.OVTST = "0".

I2C interface

The ICs feature an I2C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the ICs and the controller at clock rates up to 1MHz. The controller, typically a microcontroller, generates SCL and initiates data transfer on the bus. A controller device communicates to the ICs by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition, and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse. The IC's SDA line operates as both an input and an open-drain output. A pull-up resistor greater than 500Ω is required on the SDA bus. The IC's SCL line operates as an input only. A pull-up resistor greater than 500Ω is required on SCL if there are multiple controllers on the bus, or if the controller in a single-controller system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to ensure proper device operation, even on a noisy bus.

Bit Transfer

Bit Transfer One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. SDA and SCL idle high when the I2C bus is not busy.

STOP and START Conditions

A controller device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. A START (S) condition from the controller signals the beginning of a transmission to the IC. The controller terminates transmission, and frees the bus, by issuing a STOP (P) condition. The bus remains active if a Repeated START (Sr) condition is generated instead of a STOP condition.

Early STOP Condition

The device recognizes a STOP condition at any point during data transmission, except if the STOP condition occurs in the same high pulse as a START condition.

Clock Stretching

In general, the clock-signal generation for the I2C bus is the responsibility of the controller device. The I2C specification allows slow target devices to alter the clock signal by holding down the clock line. The process in which a target device holds down the clock line is typically called “clock stretching.” The ICs do not use any form of clock stretching to hold down the clock line.

Target Address

ADDR PIN	A6	A5	A4	A3	*A2	*A1	A0	7-BIT ADDR	WRITE	READ
0	0	1	0	1	0	0	0	0x28	0x50	0x51
1	0	1	0	1	0	0	1	0x29	0x52	0x53
0	0	1	0	1	0	1	0	0x2A	0x54	0x55
1	0	1	0	1	0	1	1	0x2B	0x56	0x57
0	0	1	0	1	1	0	0	0x2C	0x58	0x59
1	0	1	0	1	1	0	1	0x2D	0x5A	0x5B
0	0	1	0	1	1	1	0	0x2E	0x5C	0x5D
1	0	1	0	1	1	1	1	0x2F	0x5E	0x5F

Register Maps

Offset	Reg Name	Reg Description	Width	Field	Field Name	Access	Reset Value	Field Description
0x00	MASK	Interrupt Mask Register	8	[7]	OVTST	RW	0	1 = OV comparator diagnostics enable 0 = OV comparators function normally indicate that comparators are operational. The EN[4:1] bits must be low to run the diagnostics. The OVIN and OV[4:1] bits in the status registers are set to ‘1’ to Overvoltage Diagnostics Enable:
				[6]	ACCM	RW	0	1 = Mask ADC conversion complete (ACC) 0 = ADC conversion complete (ACC), mapped to INT pin
				[5]	TSM	RW	0	1 = Mask thermal-shutdown fault 0 = Thermal-shutdown faults TS[4:1] mapped to INT pin
				[4]	VDDM	RW	0	1 = Mask OVIN fault 0 = OVDD and UVDD mapped to INT pin
				[3]	VINM	RW	0	1 = Mask OVIN fault 0 = OVIN and UVIN mapped to INT pin
				[2]	OCM	RW	0	1 = Mask short-to-ground fault 0 = Overcurrent faults OC[4:1] mapped to INT pin
				[1]	OVM	RW	0	1 = Mask short-to-battery fault 0 = Overvoltage faults OV[4:1] mapped to INT pin
				[0]	UVM	RW	0	1 = Mask UV fault 0 = Undervoltage faults UV[4:1] mapped to INT pin
0x01	CONFIG	Configuration Register	8	[7]	MUX1	RW	0	11 = Reserved 10 = ADC1–ADC3 registers contain VIN, VDD, and VISET 01 = ADC1–ADC4 registers contain the output-voltage readings of each output 00 = ADC1–ADC4 registers contain current reading of each output ADC Mux Select {MUX1,MUX0}:
				[6]	MUX0	RW	0	Refer to MUX1 description
				[5]	ENC	RW	0	conversion is started after ADC1 is read. 1 = ADC continuously updates ADC1–ADC4 registers. First conversion is started when EN pin toggles high. A new 0 = ADC conversion cycle started by reading ADC1 register; ADC1–ADC4 registers updated sequentially Enable Continuous ADC Reading:
				[4]	CLR	RW	1'h1	1 = Status registers show real-time fault information; INT pin reflects the real-time status 0 = Status registers latch faults until read through I2C Clear Faults on Read:

Offset	Reg Name	Reg Description	Width	Field	Field Name	Access	Reset Value	Field Description
				[3]	EN4	RW	1'h1	0 = Disabled 1 = Enabled when EN pin is high Individual Enable Control: Both the EN pin and EN_ bit must be high to enable channel4.
				[2]	EN3	RW	1'h1	0 = Disabled 1 = Enabled when EN pin is high Individual Enable Control: Both the EN pin and EN_ bit must be high to enable a channel3
				[1]	EN2	RW	1'h1	0 = Disabled 1 = Enabled when EN pin is high Individual Enable Control: Both the EN pin and EN_ bit must be high to enable a channel2
				[0]	EN1	RW	1'h1	0 = Disabled 1 = Enabled when EN pin is high Individual Enable Control: Both the EN pin and EN_ bit must be high to enable a channel1
0x02	ID	ID Register	8	[7:6]	(reserved)	RO	0	
				[5:4]	ID	RO	0	Part ID Information:
				[3:0]	R	RO	0	Silicon revision of the device indicated by these 4 bits; revision sequential with 0x0 indicating pass 1 silicon Revision Information:
0x03	STAT1	Status Register 1	8	[7:6]	(reserved)	RO	0	
				[5]	ISET	RO	0	1 = ISET pin open or shorted 0 = ISET within operating range Use ADC reading to diagnose the resistance value. ISET Diagnostics Status:
				[4]	ACC	RO	0	1 = ADC conversions are completed 0 = Bit is reset reading ADC1; the latest completed ADC readings are always available at ADC1–ADC4 registers ADC Conversion Complete:
				[3]	OVIN	RO	0	1 = VIN > OVIN threshold 0 = VIN < OVIN threshold
				[2]	UVIN	RO	0	1 = VIN <=UVLO (switches are turned off) 0 = VIN > UVLO If the IN voltage is below the UVLO level, this bit is set to indicate device is unable to turn on the output switches. Input Undervoltage Lockout:
				[1]	OVDD	RO	0	1 = VDD > OVDD threshold 0 = VDD < OVDD threshold VDD Overvoltage Lockout:
				[0]	UVDD	RO	0	1 = VDD <=UVLO (switches are turned off) 0 = VDD > UVLO If the VDD voltage is below the UVLO level, this bit is set to indicate device is unable to turn on the output switches. VDD Undervoltage Lockout:
0x04	STAT2_L	ID Status Register 2	8	[7]	TS2	RO	0	1 = Thermal shutdown occurred on OUT2 0 = No fault Thermal Shutdown on OUT2: Each channel has its own thermal sensor.

Offset	Reg Name	Reg Description	Width	Field	Field Name	Access	Reset Value	Field Description
				[6]	OC2	RO	0	1 = Overcurrent present 0 = No overcurrent present not set, the OC bit still remains set for the duration of the 250ms hiccup cycle, and is cleared on restart after hiccup. The OC bit is set when an undervoltage event persists for longer than the shorted output-detection time. If fault latching is Overcurrent on OUT2:
				[5]	OV2	RO	0	1 = Output voltage > OV threshold 0 = Output voltage < OV threshold Overvoltage on OUT2:
				[4]	UV2	RO	0	1 = Output voltage < UV threshold 0 = Output voltage > UV threshold Undervoltage on OUT2:
				[3]	TS1	RO	0	1 = Thermal shutdown occurred on OUT1 0 = No fault Thermal Shutdown on OUT1: Each channel has its own thermal sensor.
				[2]	OC1	RO	0	1 = Overcurrent present 0 = No overcurrent present not set, the OC bit still remains set for the duration of the 250ms hiccup cycle, and is cleared on restart after hiccup. The OC bit is set when an undervoltage event persists for longer than the shorted output-detection time, If fault latching is Overcurrent on OUT1:
				[1]	OV1	RO	0	1 = Output voltage > OV threshold 0 = Output voltage < OV threshold Overvoltage on OUT1:
				[0]	UV1	RO	0	1 = Output voltage < UV threshold 0 = Output voltage > UV threshold Undervoltage on OUT1:
0x05	STAT2_H	ID Status Register 2	8	[7]	TS4	RO	0	1 = Thermal shutdown occurred on OUT4 0 = No fault Thermal Shutdown on OUT4: Each channel has its own thermal sensor.
				[6]	OC4	RO	0	1 = Overcurrent present 0 = No overcurrent present not set, the OC bit still remains set for the duration of the 250ms hiccup cycle, and is cleared on restart after hiccup. The OC bit is set when an undervoltage event persists for longer than the shorted output-detection time, If fault latching is Overcurrent on OUT4:
				[5]	OV4	RO	0	1 = Output voltage > OV threshold

Offset	Reg Name	Reg Description	Width	Field	Field Name	Access	Reset Value	Field Description
								0 = Output voltage < OV threshold Overvoltage on OUT4:
				[4]	UV4	RO	0	1 = Output voltage < UV threshold 0 = Output voltage > UV threshold Undervoltage on OUT4:
				[3]	TS3	RO	0	1 = Thermal shutdown occurred on OUT3 0 = No fault Thermal Shutdown on OUT3: Each channel has its own thermal sensor.
				[2]	OC3	RO	0	1 = Overcurrent present 0 = No overcurrent present not set, the OC bit still remains set for the duration of the 250ms hiccup cycle, and is cleared on restart after hiccup. The OC bit is set when an undervoltage event persists for longer than the shorted output-detection time, If fault latching is Overcurrent on OUT3:
				[1]	OV3	RO	0	1 = Output voltage > OV threshold 0 = Output voltage < OV threshold Overvoltage on OUT3:
				[0]	UV3	RO	0	1 = Output voltage < UV threshold 0 = Output voltage > UV threshold Undervoltage on OUT3:
0x06	ADC1	ADC Reading Registers1	8	[7:0]	D	RO	0	ADC1 Readings Register
0x07	ADC2	ADC Reading Registers2	8	[7:0]	D	RO	0	ADC2 Readings Register
0x08	ADC3	ADC Reading Registers3	8	[7:0]	D	RO	0	ADC3 Readings Register
0x09	ADC4	ADC Reading Registers4	8	[7:0]	D	RO	0	ADC4 Readings Register
0xa	CLCFG	Current Limit Cfg	8	[7:5]	(reserved)	RO	0	
				[4]	OTP_WARNM	RW	1	1=mask otp warn fault 0=OTP warn faults[4:1] map to INT pin
				[3:0]	CL_LATCH	RW	0	1: latch-off, recover when VIN or EN powerdown 0: auto-retry, with 250ms cycle the behavier of powermos after over current or hard short
0xb	CLSET	Current Limit Ratio Set	8	[7:6]	CLSET4	RW	0	00:100%, 01:75%, 10:50%, 11:25% CH4 current limit ratio
				[5:4]	CLSET3	RW	0	00:100%, 01:75%, 10:50%, 11:25% CH3 current limit ratio
				[3:2]	CLSET2	RW	0	00:100%, 01:75%, 10:50%, 11:25%

Offset	Reg Name	Reg Description	Width	Field	Field Name	Access	Reset Value	Field Description
								CH2 current limit ratio
				[1:0]	CLSET1	RW	0	00:100%, 01:75%, 10:50%, 11:25% CH1 current limit ratio
0xc	STAT3	Status Register 3	8	[7:4]	(reserved)	RO	0	
				[3]	OTP_WARN4	RO	0	CH4 over temperature
				[2]	OTP_WARN3	RO	0	CH3 over temperature
				[1]	OTP_WARN2	RO	0	CH2 over temperature
				[0]	OTP_WARN1	RO	0	CH1 over temperature
0xd	D2A_RESERVED	reserved	8	[7:0]	D2A_RESERVED	RW	0	reserved

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPW20400xQ is a 400-mΩ 2/4-channel high-side power switch product with AEC-Q100 qualified. The following application schematic shows a typical usage of the TPW20400xQ series.

Typical Application

Figure 8 shows the typical protection application schematic of the TPW20400xQ.

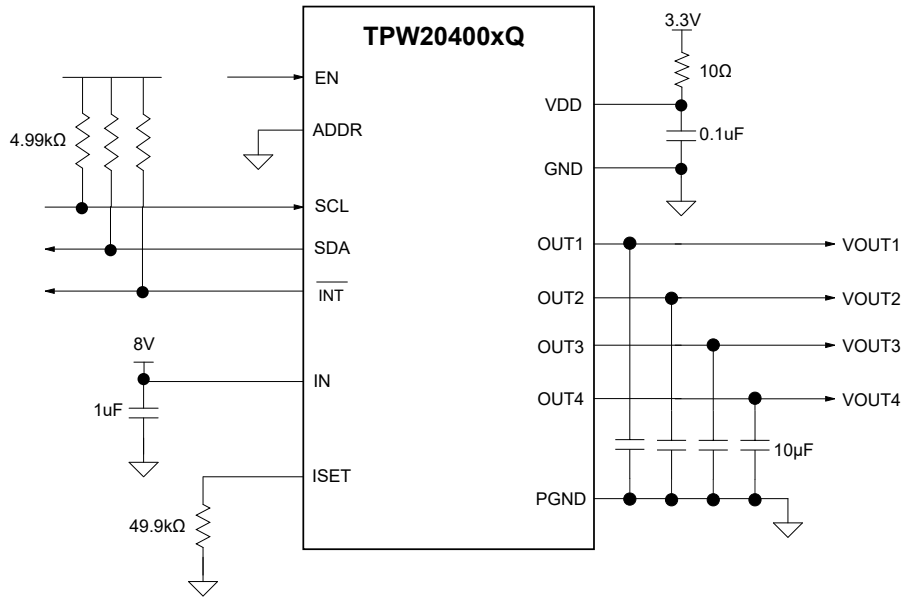


Figure 8. Typical Application Circuit

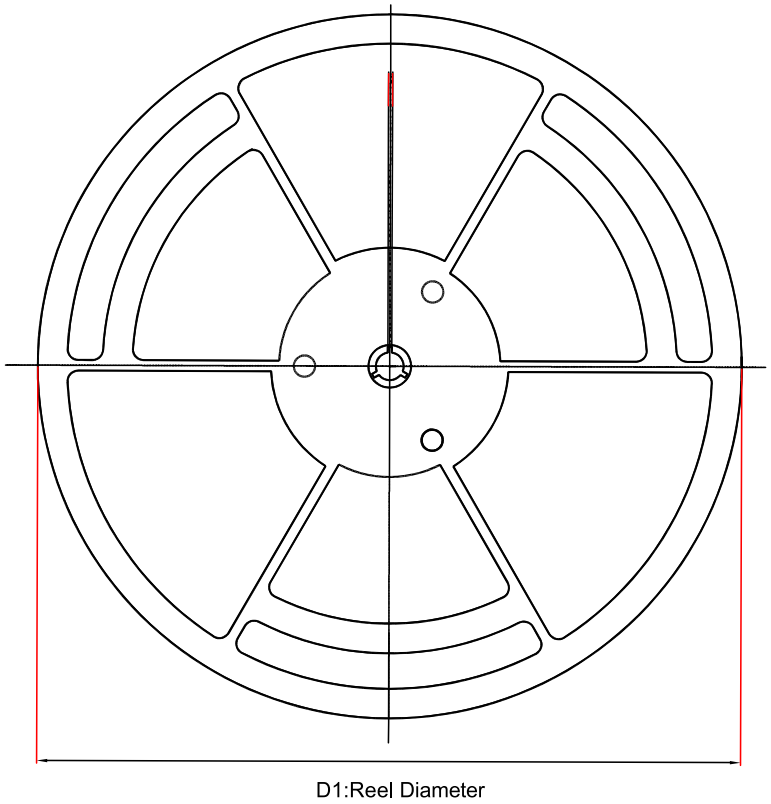
Layout

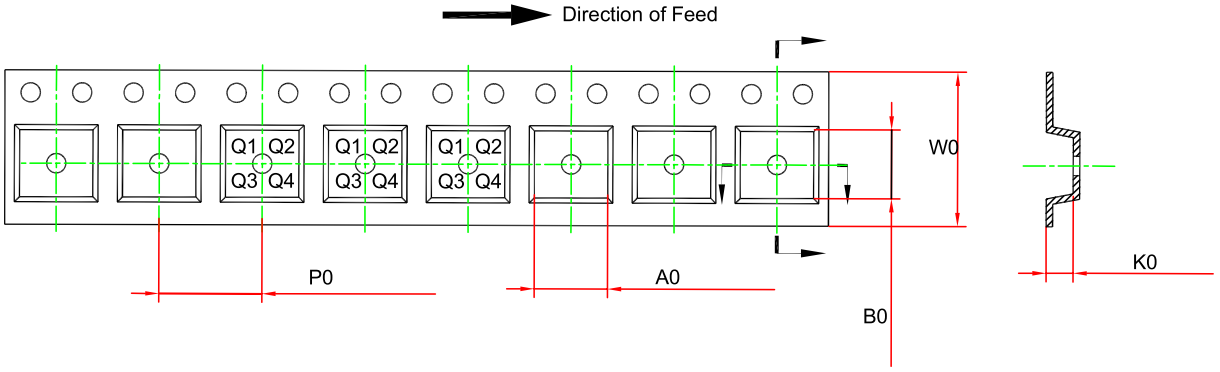
Layout Guideline

To get good thermal performance and prevent over-temperature protection, the PCB layout is important. A well-designed PCB layout can effectively optimize heat dissipation, which is crucial for ensuring the long-term reliability of the device.

- It is recommended to maximize the coverage of copper on the PCB to enhance the thermal conductivity of the board. Since the primary heat flow path from the package to the surrounding environment passes through the copper on the PCB, having maximum copper coverage is particularly important when there is no heat sink attached to the opposite side of the board.
- It is recommended to place as many thermal vias as possible underneath the package ground pad to optimize the thermal conductivity of the board.
- It is suggested that all thermal vias be either plated shut or plugged and capped on both sides of the board to prevent solder voids and maintain reliability and performance.
- It is recommended to use wide traces or thick copper weight in the input/output current paths to minimize I×R voltage drop.

Tape and Reel Information



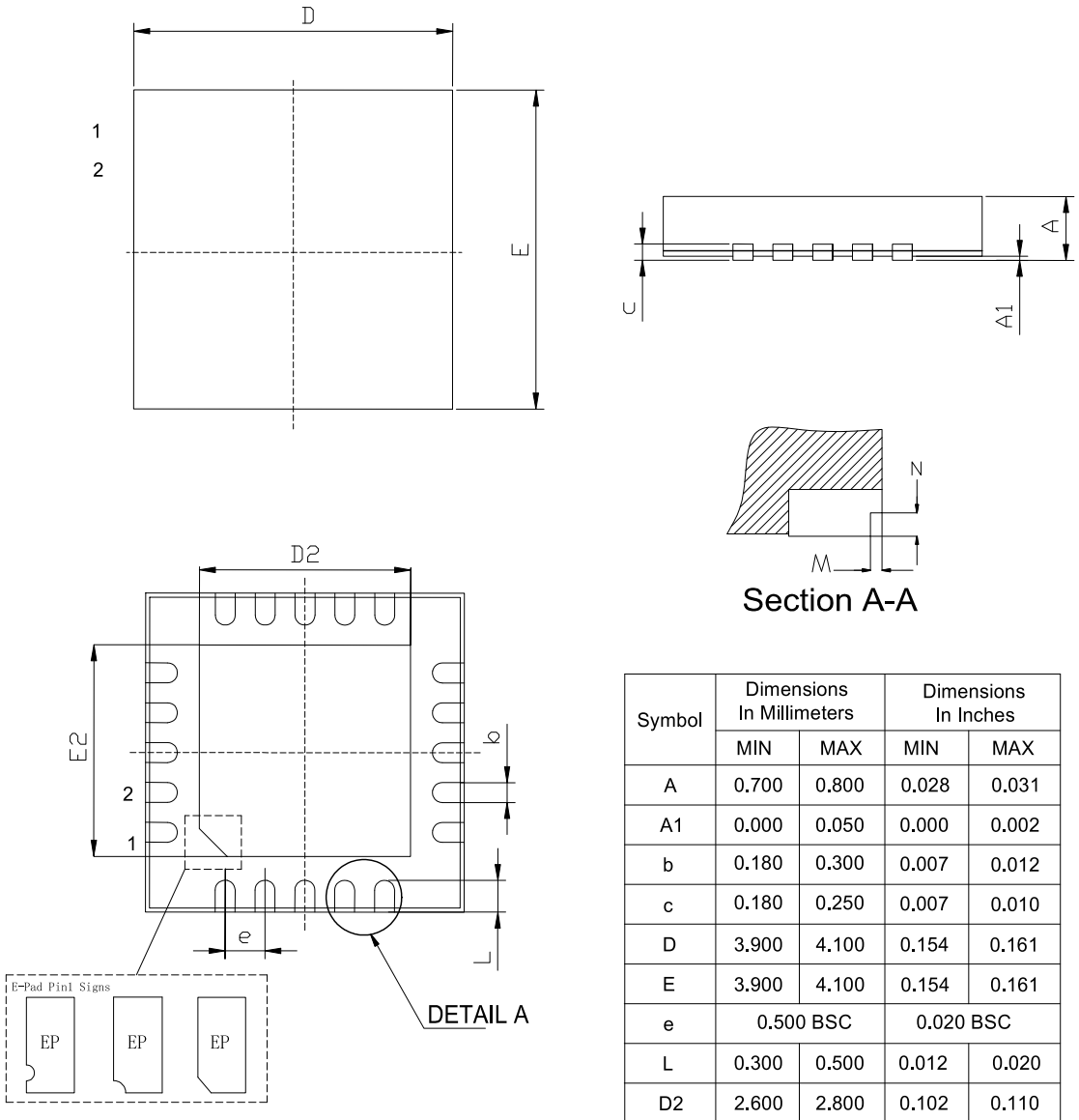


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPW20400QQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1
TPW20400QBQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1
TPW20400QCQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1
TPW20400QAQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1

Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPW20400QABQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1
TPW20400QACQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1
TPW20400QDQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1
TPW20400QDAQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1
TPW20400DQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1
TPW20400DBQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1
TPW20400DCQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1
TPW20400DAQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1
TPW20400DABQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1
TPW20400DACQ-QFOR-S	QFN4X4-20	330	4.3	1.1	12	17.6	4.3	8	Q1

QFN4X4-20-WET-D

Package Outline Dimensions QFO(QFN4X4-20-WET-D)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
c	0.180	0.250	0.007	0.010
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
e	0.500 BSC		0.020 BSC	
L	0.300	0.500	0.012	0.020
D2	2.600	2.800	0.102	0.110
E2	2.600	2.800	0.102	0.110
h	0.300	0.400	0.012	0.016
M	0.010	0.090	0.000	0.004
N	0.080	0.180	0.003	0.007

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPW20400QQ-QFOR-S	−40 to 125°C	QFN4X4-20	W400Q	MSL3	3,000	Green
TPW20400QBQ-QFOR-S (1)	−40 to 125°C	QFN4X4-20	QBQ	MSL3	3,000	Green
TPW20400QCQ-QFOR-S (1)	−40 to 125°C	QFN4X4-20	QCQ	MSL3	3,000	Green
TPW20400QAQ-QFOR-S	−40 to 125°C	QFN4X4-20	W400Q	MSL3	3,000	Green
TPW20400QABQ-QFOR-S (1)	−40 to 125°C	QFN4X4-20	QBQ	MSL3	3,000	Green
TPW20400QACQ-QFOR-S (1)	−40 to 125°C	QFN4X4-20	QCQ	MSL3	3,000	Green
TPW20400QDQ-QFOR-S (1)	−40 to 125°C	QFN4X4-20	QDQ	MSL3	3,000	Green
TPW20400QDAQ-QFOR-S (1)	−40 to 125°C	QFN4X4-20	QDQ	MSL3	3,000	Green
TPW20400DQ-QFOR-S	−40 to 125°C	QFN4X4-20	DQ	MSL3	3,000	Green
TPW20400DBQ-QFOR-S (1)	−40 to 125°C	QFN4X4-20	DBQ	MSL3	3,000	Green
TPW20400DCQ-QFOR-S (1)	−40 to 125°C	QFN4X4-20	DCQ	MSL3	3,000	Green
TPW20400DAQ-QFOR-S	−40 to 125°C	QFN4X4-20	DQ	MSL3	3,000	Green
TPW20400DABQ-QFOR-S (1)	−40 to 125°C	QFN4X4-20	DBQ	MSL3	3,000	Green
TPW20400DACQ-QFOR-S (1)	−40 to 125°C	QFN4X4-20	DCQ	MSL3	3,000	Green

(1) For future products, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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