Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

Features

- Wide-Supply Voltage Range: 1.6 V to 6.0 V
- Very Low Quiescent Current: 600 nA typ
- 0.5 V Fixed Threshold Voltage
- Power-on Reset Generator with Adjustable Delay Time
- High Threshold Accuracy 1% Typ
- Chip Enable Input
- Open-drain / Push-pull Output Options
- Active-high ENABLE / Active-low $\overline{\text{ENABLE}}$ Options
- Active-high RESET / Active-low $\overline{\text{RESET}}$ Options
- Temperature Range: −40°C to 125°C
- Green Product, DFN1.5X1-6 Package

Applications

- Server and Data Center
- Surveillance and IP Camera
- Network Switches and Routers
- Solid State Drive
- Optical Communication Module

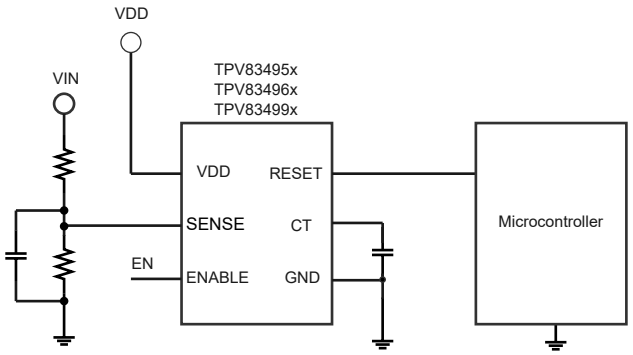
Description

The TPV8349x is a family of supervisory circuits. The SENSE pin features a high-impedance input, enabling different voltage monitoring requirements to be met by configuring external resistors. Asserting an active low/ active high open-drain or push-pull $\overline{\text{RESET}}$/RESET output when the voltage of the sense pin drops below a fixed threshold or when the enable pin ENABLE/$\overline{\text{ENABLE}}$ is logic high/low. The $\overline{\text{RESET}}$/RESET output remains low/ high for the user-adjusted delay time by the external capacitor after the sense voltage returns above the fixed threshold with a hysteresis, and the enable PIN ENABLE/ $\overline{\text{ENABLE}}$ is logic high/low.

The threshold voltage of the TPV8349x device can achieve 1% accuracy. The delay time can be set to 40 μs to 6.2 s by connecting the external capacitor to the CT pin. The TPV8349x family has a very low typical quiescent current of 600 nA.

The TPV8349x is available in the DFN1.5x1-6 package. Its operating temperature range is from −40°C to +125°C.

Typical Application Circuit



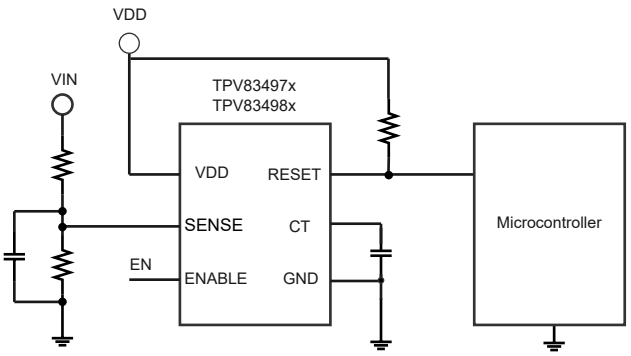


Table of Contents

Product Family Table

Order Number	Enable Type	RESET Type	t_{PROP}	t_{DELAY}	Marking	Package
TPV83495A-DFNR	active-high	push-pull, active-high	Capacitor Adjustable	Capacitor Adjustable	95A	DFN1.5X1-6
TPV83495P-DFNR	active-high	push-pull, active-high	350ns	Capacitor Adjustable	95P	DFN1.5X1-6
TPV83496A-DFNR (1)	active-low	push-pull, active-low	Capacitor Adjustable	Capacitor Adjustable	96A	DFN1.5X1-6
TPV83496P-DFNR (1)	active-low	push-pull, active-low	350ns	Capacitor Adjustable	96P	DFN1.5X1-6
TPV83497A-DFNR (1)	active-high	Open-drain, active-high	Capacitor Adjustable	Capacitor Adjustable	97A	DFN1.5X1-6
TPV83497P-DFNR (1)	active-high	Open-drain, active-high	350ns	Capacitor Adjustable	97P	DFN1.5X1-6
TPV83498A-DFNR (1)	active-low	Open-drain, active-low	Capacitor Adjustable	Capacitor Adjustable	98A	DFN1.5X1-6
TPV83498P-DFNR (1)	active-low	Open-drain, active-low	350ns	Capacitor Adjustable	98P	DFN1.5X1-6
TPV83499A-DFNR (1)	active-low	push-pull, active-high	Capacitor Adjustable	Capacitor Adjustable	99A	DFN1.5X1-6
TPV83499P-DFNR (1)	active-low	push-pull, active-high	350ns	Capacitor Adjustable	99P	DFN1.5X1-6

(1) For future products, contact the 3PEAK factory for more information and samples.

Revision History

Date	Revision	Notes
2026-04-20	Rev.A.0	Released version.

Pin Configuration and Functions

TPV8349x
DFN1.5X1-6 Package
Top View

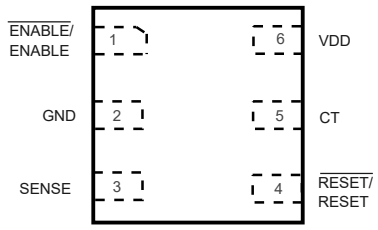


Table 1. Pin Functions: TPV8349x

Pin	Name	I/O	Description
1	$\overline{\text{ENABLE}}$ / ENABLE	I	Enable pin. For active-high ENABLE version: RESET/$\overline{\text{RESET}}$ will be de-asserted only when ENABLE is high and $V_{SENSE} > V_{IT}$; For active-low $\overline{\text{ENABLE}}$ version: RESET/$\overline{\text{RESET}}$ will be de-asserted only when $\overline{\text{ENABLE}}$ is low and $V_{SENSE} > V_{IT}$. When the enable logic is not satisfied, RESET/$\overline{\text{RESET}}$ will be asserted immediately.
2	GND	G	Ground. This pin should be connected to ground reference.
3	SENSE	I	Sense Pin. It is used for monitoring voltage. If the voltage drops below the threshold voltage VIT, the $\overline{\text{RESET}}$/RESET is asserted. The sense pin can be connected to any voltage by configuring an external resistor divider.
4	$\overline{\text{RESET}}$/RESET	O	$\overline{\text{RESET}}$/RESET Output. This pin is active low open drain output or push-pull output. It is driven to a low impedance state when $\overline{\text{RESET}}$/RESET is asserted by the voltage of the sense pin lower than the threshold V_{IT}, or $\overline{\text{ENABLE}}$/ENABLE pin is high/low . $\overline{\text{RESET}}$/RESET will keep low for the reset delay time programmed by the CT pin after both of the sense pin is above V_{IT} and $\overline{\text{ENABLE}}$/ ENABLE pin is low/high. A pulled-up resistor from 10 kΩ to 1 MΩ should be connected to VDD if it is open drain output.
5	CT	I/O	Reset Delay Time Programming Pin. Connecting this pin to VDD through a 40 kΩ to 200 kΩ resistor or leaving it open results in fixed reset delay times. Connecting this pin to ground-referenced capacitor (≥ 100 pF) gives a user-programmable reset delay time.
6	VDD	P	Supply Voltage. A 0.1-μF ceramic capacitor was placed as close as possible to the VDD pin.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Power Supply, V_{DD} to GND		−0.3	6.5	V
V_{CT} V_{RESET} V_{ENABLE}	Input Voltage for CT, ENABLE, $\overline{RESET}$/RESET pin	−0.3 to V_{DD} + 0.3 V, max 6 V		
V_{SENSE}	Input Voltage for SENSE Pin	−0.3	6.5	V
I_{RESET}	Current of $\overline{RESET}$/RESET Pin		20	mA
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		300	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC\text{-}TOP}$	Unit
DFN1.5X1-6	275	180	239	°C/W

Electrical Characteristics

All test conditions: V_{DD} = 5 V, T_A = −40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

Parameter			Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range		−40°C < T_A < 125°C	1.6		6.0	V
$V_{DD(min)}$	Minimum VDD to Guaranteed $\overline{RESET}$/ RESET Output Valid (1)				0.5	0.8	V
V_{UVLO}	Undervoltage Lockout		VDD falling		1.5		V
I_{DD}	Quiescent current (IQ) -TPV8349xA		VDD = VEN = 5.5 V, RESET not asserted, RESET/CT pin open		1		μA
	Quiescent current (IQ) -TPV8349xP				0.6		μA
V_{OL}	Output Low Voltage of $\overline{RESET}$/RESET Pin		1.6 V ≤ V_{DD} < 6.0 V, I_{OL} = 2.0 mA			0.3	V
V_{OH}	Output high voltage of RESET $\overline{RESET}$/ RESET Pin		1.6 V < V_{DD} < 6.0 V, I_{OH} = 2.0 mA	0.8V_{DD}			V
V_{IT}	Negative-going Input Threshold		−40°C < T_A < 125°C	0.48	0.495	0.51	V
V_{HYS}	Hysteresis on V_{IT}				5		mV
I_{SENSE}	Input Current at SENSE Pin		V_{SENSE} = V_{IT}		< 1		nA
C_{IN}	Input Capacitance, any pin	CT pin	V_{IN} = 0 V to V_{DD}		5		pF
		Other pins	V_{IN} = 0 V to 6.0 V		5		pF
V_{IL}	ENABLE Logic Low Input			0		0.3V_{DD}	
V_{IH}	ENABLE Logic High Input			0.7V_{DD}		V_{DD}	
I_{EN}	ENABLE Current			-100		100	nA
Switching Electrical Specifications							
t_{DELAY}	SENSE to RESET Propagation Delay	VIN rising	CCDELAY = 0 nF		40		μs
			CCDELAY = 47 nF		185		ms
t_{DL}		VIN falling			12		μs
t_{PW}	ENABLE Minimum Input Pulse Width			1			μs
	ENABLE Glitch Rejection				200		ns
t_{OFF}	From Device Enabled to Device Disabled				300		ns
t_{PROP}	From Device Disabled to Device Enabled	TPV8349xA	CCDELAY = 0 nF		40		μs
			CCDELAY = 47 nF		185		ms
		TPV8349xP			350		ns

(1) Guaranteed by bench test.

Typical Performance Characteristics

All test conditions: V_{DD} = 5 V, T_A = + 25°C, unless otherwise noted.

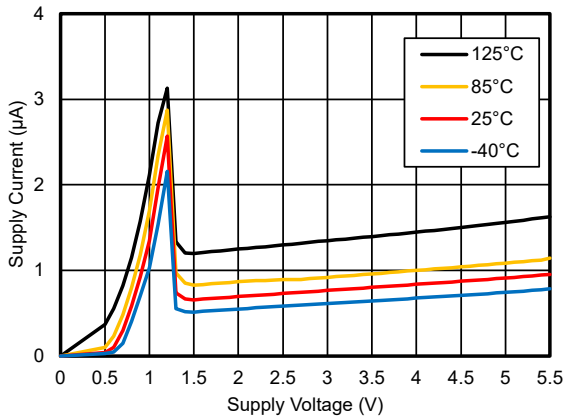


Figure 1. Supply Current vs. Supply Voltage

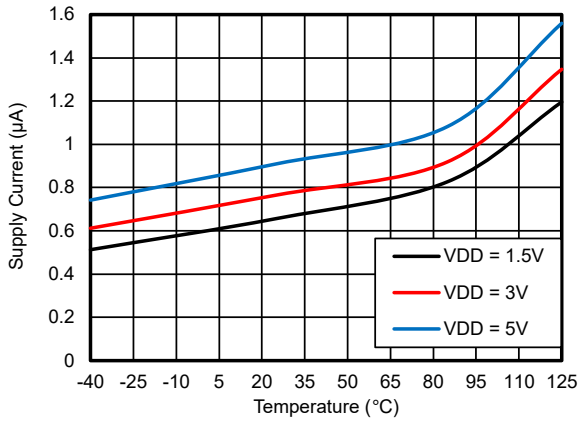


Figure 2. Supply Current vs. Temperature

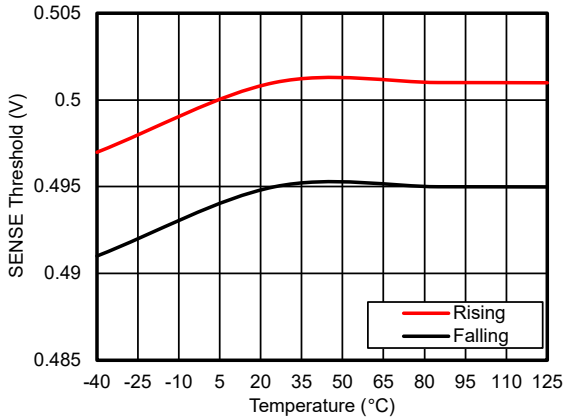


Figure 3. SENSE Threshold vs. Temperature

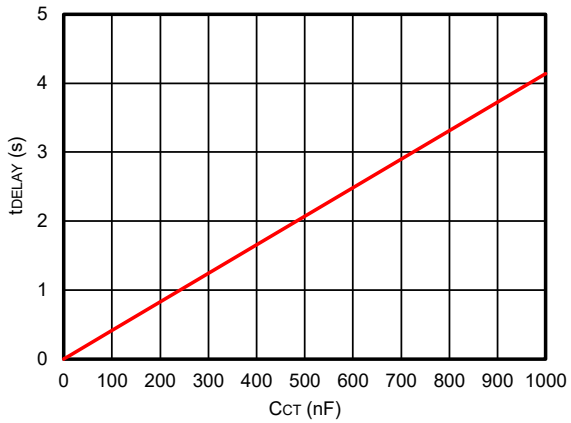


Figure 4. Reset Delay Time vs. C_T

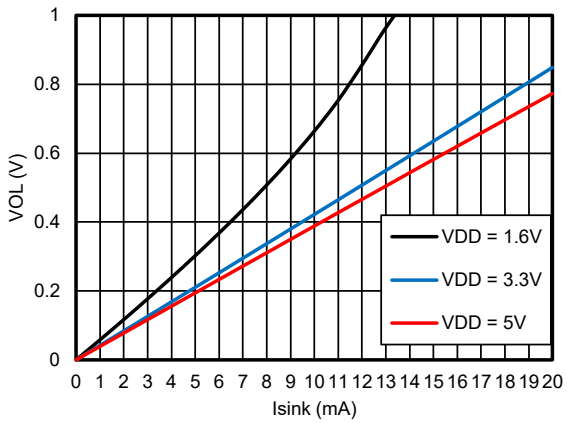


Figure 5. Output Low Voltage vs. Sink Current

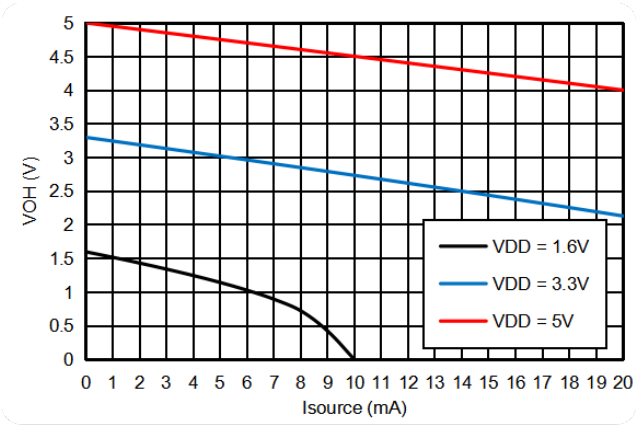


Figure 6. Output High Voltage vs. Source Current

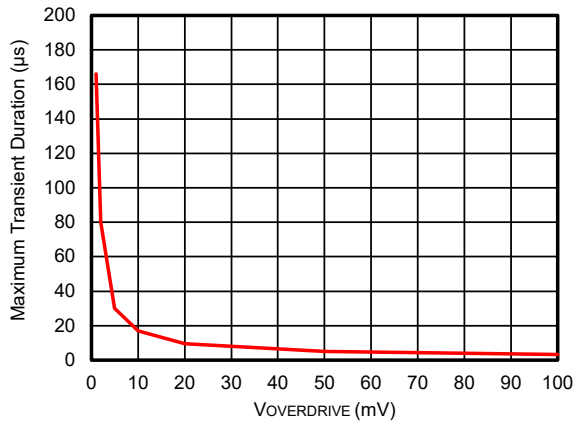


Figure 7. Maximum Transient Duration vs. $V_{OVERDRIVE}$

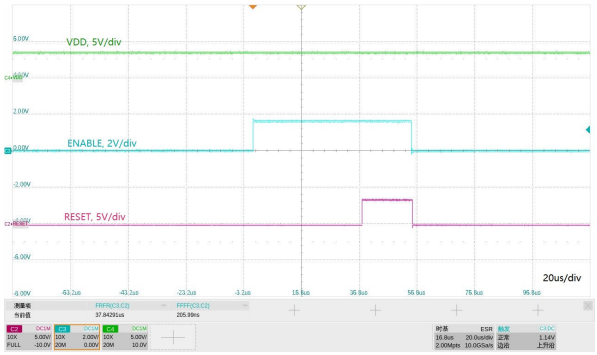


Figure 8. Enable Turn-On/Off Delay

Detailed Description

Overview

The TPV8349x is a family of supervisory circuits. The SENSE pin features a high-impedance input, enabling different voltage monitoring requirements to be met by configuring external resistors. Asserting an active low/active high open-drain or push-pull $\overline{\text{RESET}}$/RESET output when the voltage of the sense pin drops below a fixed threshold or when the enable pin ENABLE/$\overline{\text{ENABLE}}$ is logic high/low. The $\overline{\text{RESET}}$/RESET output remains low/high for the user-adjusted delay time by the external capacitor after the sense voltage returns above the fixed threshold with a hysteresis and the enable PIN ENABLE/ $\overline{\text{ENABLE}}$ is logic high/low.

The threshold voltage of the TPV8349x device can achieve 1% accuracy. The delay time can be set to 40 µs to 6.2 s by connecting the external capacitor to the CT pin. The TPV8349x family has a very low typical quiescent current of 600 nA.

Functional Block Diagram

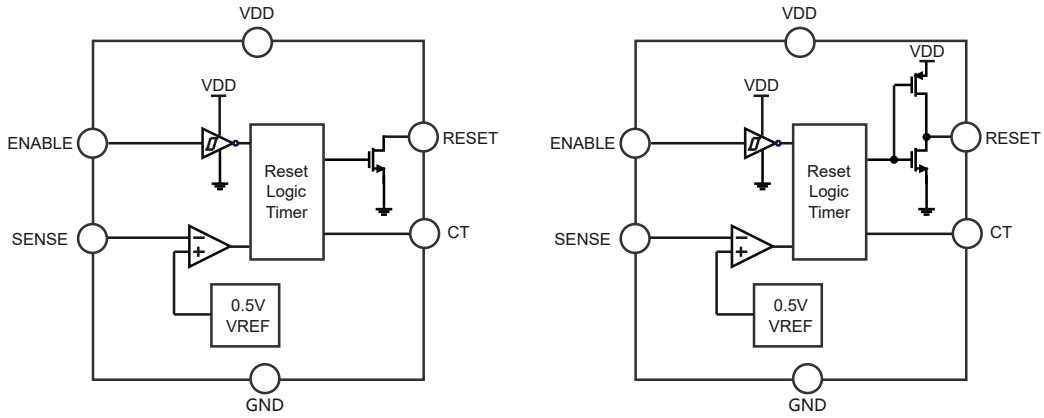


Figure 9. Functional Block Diagram

Feature Description

RESET Output

The reset threshold voltage can be set to any voltage above 0.5 V using an external resistor divider. The sense pin monitors the system voltage. If the voltage on this pin drops below V_{IT}, the $\overline{\text{RESET}}$ /RESET is asserted.

The TPV8349x features an active-low or active-high output. For active-low output, the reset signal is guaranteed to be logic low for V_{SENSE} down to V_{IT}. For active-high output, the reset signal is guaranteed to be logic high for V_{SENSE} down to V_{IT}. Reset remains asserted for the duration of the reset delay time (t_{DELAY}) after VSENSE rises above the reset threshold. Figure 10 shows the reset output.

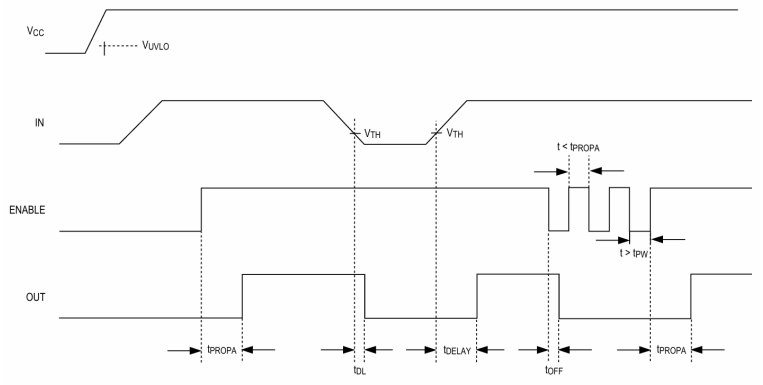


Figure 10. SENSE Reset and ENABLE Reset Timing

RESET Delay Time

The TPV8349x provides a programmable reset delay time (t_{DELAY}), which is realized by selecting a capacitor between CT and GND to allow the designer to set any reset delay time. The reset delay time (t_{DELAY}) under a given capacitor value is calculated using Equation 1.

$$t_{DELAY}\,(\mu s) = 4 \times C_{CT}\,(pF) + 40\,(\mu s) \quad (1)$$

Enable control

TPV83495 and TPV83497 feature an active-high enable input pin (ENABLE), while TPV83496, TPV83498, and TPV83499 feature an active-low input pin ($\overline{\text{ENABLE}}$). When V_{SENSE} exceeds V_{IT} and ENABLE is driven high or $\overline{\text{ENABLE}}$ is driven low, for the A version, RESET is asserted high and $\overline{\text{RESET}}$ is asserted low after an adjustable delay t_{PROPA}; for the P version, RESET is driven high and $\overline{\text{RESET}}$ is driven low after a fixed delay t_{PROPP}.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

Figure 11 shows the typical application circuit of TPV8349x with a reset threshold voltage set by the external resistor divider.

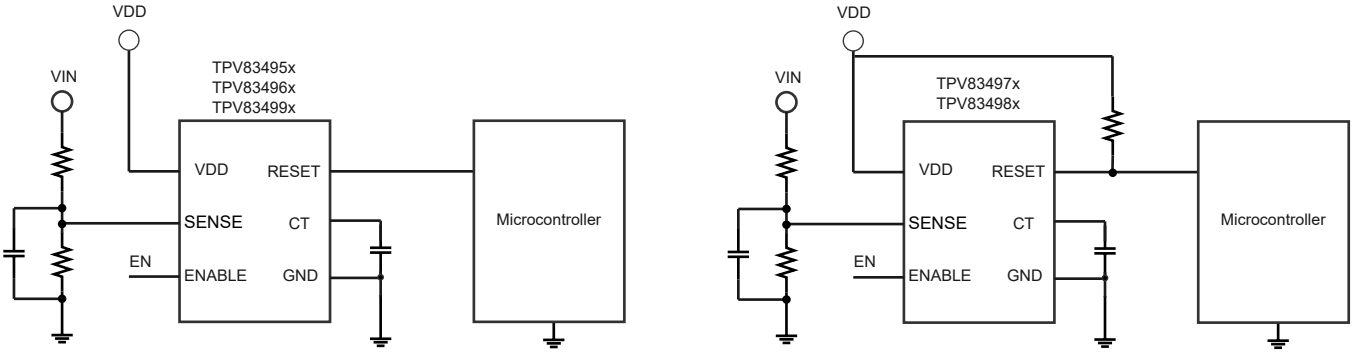
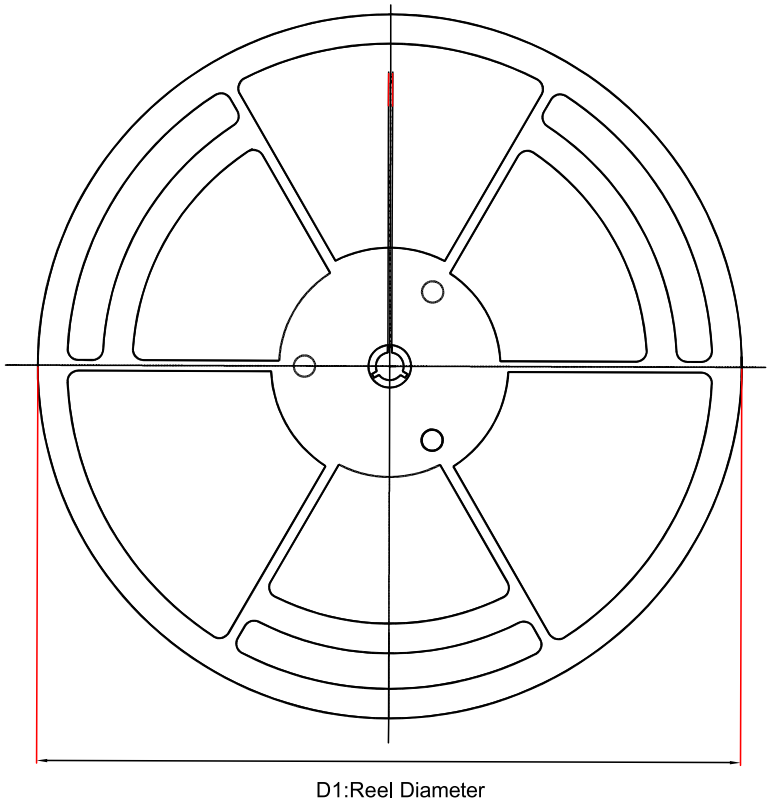
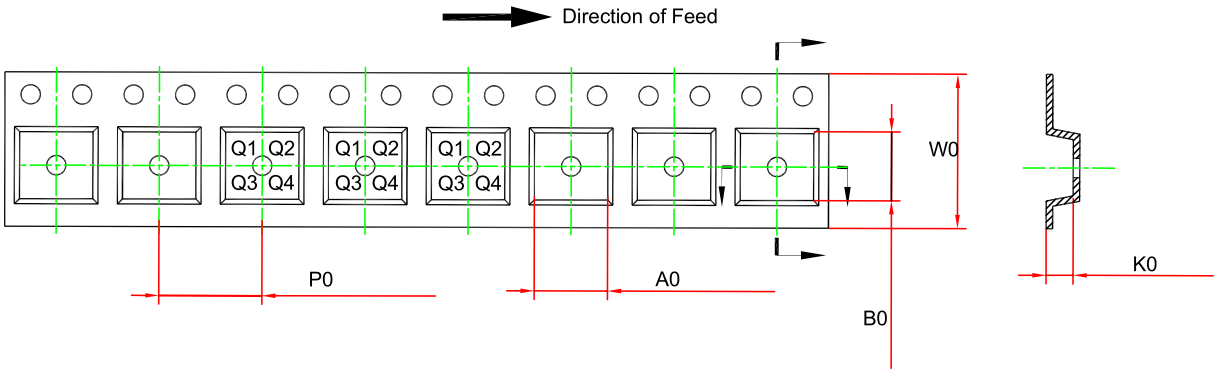


Figure 11. Typical Application Circuit

Tape and Reel Information



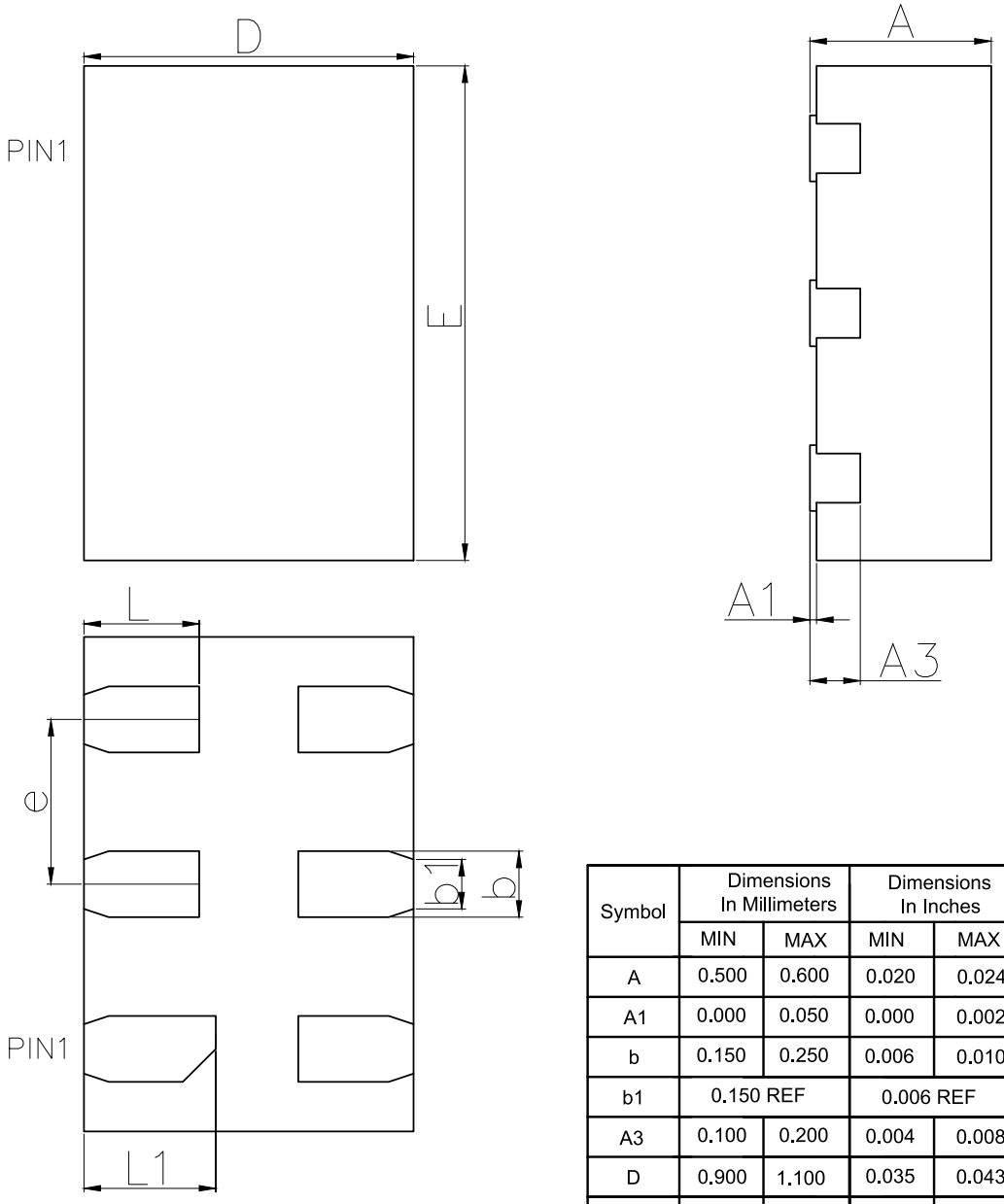


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPV8349x-DFNR	DFN1.5X1-6	180	13.1	1.15	1.72	0.70	4	8	Q1

Package Outline Dimensions

DFN1.5X1-6

Package Outline Dimensions DFN(DFN1.5X1-6-A)



NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
b	0.150	0.250	0.006	0.010
b1	0.150 REF		0.006 REF	
A3	0.100	0.200	0.004	0.008
D	0.900	1.100	0.035	0.043
E	1.400	1.600	0.055	0.063
e	0.500 BSC		0.020 BSC	
L	0.274	0.426	0.011	0.017
L1	0.324	0.476	0.013	0.019

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPV83495A-DFNR	−40 to 125°C	DFN1.5X1-6	95A	1	Tape and Reel, 3000	Green
TPV83495P-DFNR	−40 to 125°C	DFN1.5X1-6	95P	1	Tape and Reel, 3000	Green
TPV83496A-DFNR (1)	−40 to 125°C	DFN1.5X1-6	96A	1	Tape and Reel, 3000	Green
TPV83496P-DFNR (1)	−40 to 125°C	DFN1.5X1-6	96P	1	Tape and Reel, 3000	Green
TPV83497A-DFNR (1)	−40 to 125°C	DFN1.5X1-6	97A	1	Tape and Reel, 3000	Green
TPV83497P-DFNR (1)	−40 to 125°C	DFN1.5X1-6	97P	1	Tape and Reel, 3000	Green
TPV83498A-DFNR (1)	−40 to 125°C	DFN1.5X1-6	98A	1	Tape and Reel, 3000	Green
TPV83498P-DFNR (1)	−40 to 125°C	DFN1.5X1-6	98P	1	Tape and Reel, 3000	Green
TPV83499A-DFNR (1)	−40 to 125°C	DFN1.5X1-6	99A	1	Tape and Reel, 3000	Green
TPV83499P-DFNR (1)	−40 to 125°C	DFN1.5X1-6	99P	1	Tape and Reel, 3000	Green

(1) For future products, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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