

Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

Features

- Wide Supply Voltage Range: 1.6 V to 6 V
- Very Low Quiescent Current: 2 μ A
- Reset Threshold Voltage from 1.6 V to 4.2 V
- Power-On Reset Generator with Adjustable Delay Time 430 μ s to 150 ms
- High Threshold Accuracy 1.5% Typ.
- Manual Reset ($\overline{\text{MR}}$) Input
- Open-Drain $\overline{\text{RESET}}$ Output
- Active Low $\overline{\text{RESET}}$
- Temperature Range: -40°C to 125°C
- Green Product, SOT23-5 Package

Applications

- Server and Datacenter
- Surveillance and IP Camera
- Network Switches and Routers
- Solid State Drive
- Optical Communication Module

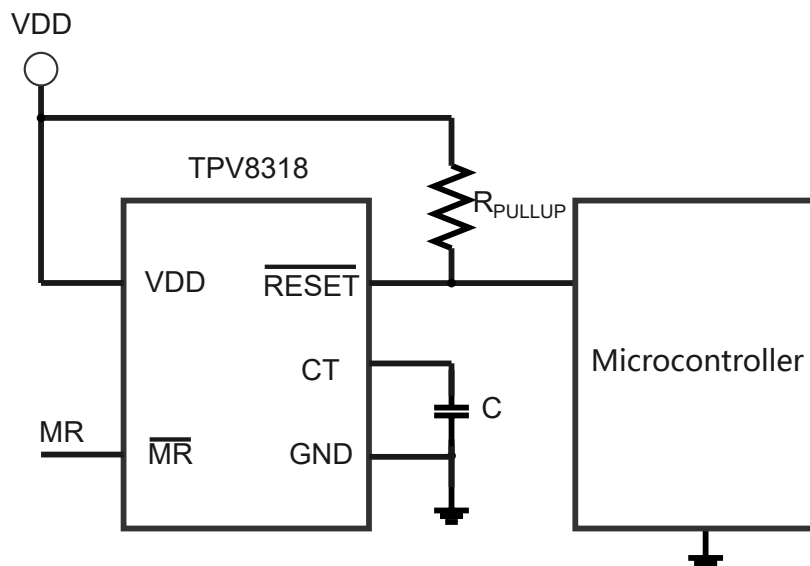
Description

The TPV8318 is a family of supervisory circuits to monitor a voltage rail from 1.6 V to 6 V, asserting an active low open drain $\overline{\text{RESET}}$ output when the VDD voltage drops below the reset threshold or when manual reset pin $\overline{\text{MR}}$ is logic low. The $\overline{\text{RESET}}$ output remains low for the user-adjusted delay time by an external capacitor after the VDD voltage returns above the fixed threshold with a 150-mV hysteresis or manual reset $\overline{\text{MR}}$ returns to logic high.

The threshold voltage of the TPV8318 device can achieve 1.5% accuracy. The delay time can be set to 430 μ s to 150 ms by connecting the external capacitor to the CT pin. The TPV8318 has a very low typical quiescent current of 2 μ A.

The TPV8318 is available in the SOT23 package, and its operating temperature range is from -40°C to $+125^{\circ}\text{C}$.

Typical Application Circuit



**Low Quiescent Current Supervisory Circuits with Programmable
Reset Delay****Table of Contents**

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**Low Quiescent Current Supervisory Circuits with Programmable
Reset Delay****Product Family Table**

Order Number	Threshold Voltage (V)	Nominal Monitored Voltage (V)	Marking	Package
TPV8318LD160-S5TR-S ⁽¹⁾	1.6	1.8	L16	SOT23-5
TPV8318LD170-S5TR-S ⁽¹⁾	1.7	1.9	L17	SOT23-5
TPV8318LD220-S5TR-S ⁽¹⁾	2.2	2.5	L22	SOT23-5
TPV8318LD270-S5TR-S ⁽¹⁾	2.7	3.0	L27	SOT23-5
TPV8318LD300-S5TR-S	3.0	3.3	L30	SOT23-5
TPV8318LD400-S5TR-S ⁽¹⁾	4.0	5.0	L40	SOT23-5
TPV8318LD420-S5TR-S ⁽¹⁾	4.2	5	L42	SOT23-5

(1) For future products, contact the 3PEAK factory for more information and samples.

Revision History

Date	Revision	Notes
2023-04-13	Rev.A.0	Initial release.
2024-02-5	Rev.A.1	Corrected the temperature range to 125°C in order information.
2024-06-05	Rev.A.2	Corrected typo.

Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

Pin Configuration and Functions

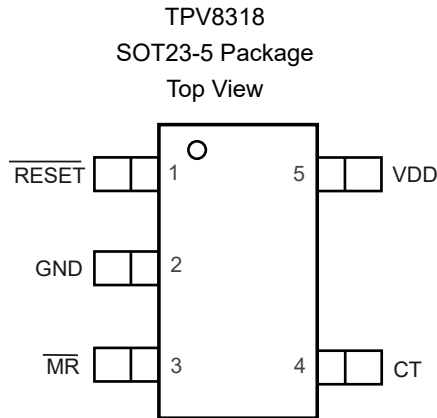


Table 1. Pin Functions: TPV8318

Pin No.	Name	I/O	Description
1	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$ Output. This pin is active low open drain output. It is driven to a low impedance state when $\overline{\text{RESET}}$ is asserted by the VDD voltage lower than the threshold V_{IT} , or the $\overline{\text{MR}}$ pin is low. $\overline{\text{RESET}}$ will keep low for the reset delay time programmed by the CT pin after VDD is above V_{IT} , or $\overline{\text{MR}}$ pin is high. A pulled-up resistor from 10 k Ω to 1 M Ω should be connected to VDD.
2	GND	-	Ground.
3	$\overline{\text{MR}}$	I	Manual Reset Input $\overline{\text{MR}}$ low asserts the $\overline{\text{RESET}}$ pin. $\overline{\text{MR}}$ is internally tied to VDD by a 90-k Ω pull-up resistor.
4	CT	O	Reset Delay Time Programming Pin. Connecting this pin to ground referenced capacitor gives a user-programmable reset delay time.
5	VDD	I	Supply Voltage. A 0.1- μF ceramic capacitor placed as close as to the VDD pin.

Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Power Supply	VDD	-0.3	6.5	V
V _{CT} , V _{RESET} , V _{MR}	Input Voltage for CT, $\overline{\text{MR}}$, $\overline{\text{RESET}}$ pin	-0.3	6	V
I _{CT}	Current of CT pin		10	mA
I _{RESET}	Current of $\overline{\text{RESET}}$ pin		5	mA
T _J	Maximum Junction Temperature		150	°C
T _A	Operating Temperature Range	-45	125	°C
T _{STG}	Storage Temperature Range	-65	150	°C
T _L	Lead Temperature (Soldering 10 sec)		300	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
- (2) This data was taken with the JEDEC low effective thermal conductivity test board.
- (3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-5	118	52	°C/W

Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

Electrical Characteristics

All test conditions: $V_{DD} = 5\text{ V}$, $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
V_{DD}	Supply Voltage Range	$-40^\circ\text{C} < T_A < 125^\circ\text{C}$	1.6		6.0	V
V_{POR}	Power-up Reset Voltage			0.5	0.8	V
I_{DD}	Quiescent Current (I_Q)	$V_{DD} = 3.3\text{ V}$, $\overline{\text{RESET}}$ not asserted, $\overline{\text{MR}}$, $\overline{\text{RESET}}$, CT pin open		0.7	1.55	μA
		$V_{DD} = 6\text{ V}$, $\overline{\text{RESET}}$ not asserted, $\overline{\text{MR}}$, $\overline{\text{RESET}}$, CT pin open		0.8	1.65	μA
V_{OL}	Output Low Voltage of $\overline{\text{RESET}}$ Pin	$1.3\text{ V} \leq V_{DD} < 1.6\text{ V}$, $I_{OL} = 0.4\text{ mA}$			0.3	V
		$1.6\text{ V} \leq V_{DD} < 6.0\text{ V}$, $I_{OL} = 1.0\text{ mA}$			0.4	V
$V_{IT, ERR}$	Negative-going Input Threshold Accuracy	$T_A = 25^\circ\text{C}$	-1.5		1.5	%
		$-40^\circ\text{C} < T_A < 125^\circ\text{C}$	-2.5		2.5	%
V_{HYS}	Hysteresis on V_{IT}			150		mV
R_{MR}	$\overline{\text{MR}}$ Internal Pull-up Resistance			90		k Ω
I_{OH}	$\overline{\text{RESET}}$ Leakage Current	$V_{\overline{\text{RESET}}} = 5.5\text{ V}$			300	nA
C_{IN}	Input Capacitance, any pin	CT pin $V_{IN} = 0\text{ V}$ to V_{DD}		5		pF
		Other pins $V_{IN} = 0\text{ V}$ to 6.0 V		5		pF
V_{IL}	$\overline{\text{MR}}$ Logic Low Input		0		$0.3V_{DD}$	
V_{IH}	$\overline{\text{MR}}$ Logic High Input		$0.7V_{DD}$		V_{DD}	
Switching Electrical Specification						
t_w	Input Pulse Width to Assert $\overline{\text{RESET}}$ Pin	VDD	$V_{IH} = 3.15\text{ V}$, $V_{IL} = 2.85\text{ V}$		80	μs
		$\overline{\text{MR}}$	$V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$		340	ns
t_D	Reset Delay Time	$C_T = \text{Open}$		0.4		ms
		$C_T = 100\text{ pF}$		0.67		ms
		$C_T = 1000\text{ pF}$		2.9		ms
t_{MR}	Propagation Delay from $\overline{\text{MR}}$ to Reset	$V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$		350		ns
t_{RP}	Propagation Delay from VDD Drop to Reset			100		μs

Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

Typical Performance Characteristics

All test conditions: $V_{DD} = 5\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

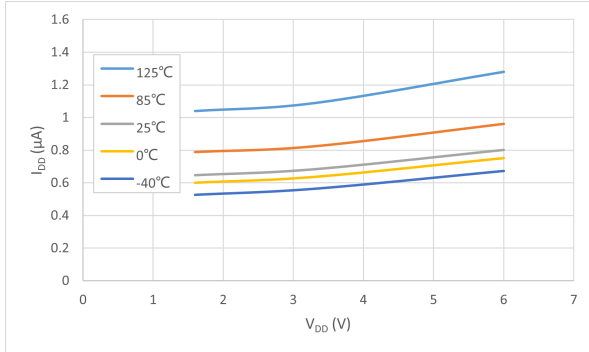


Figure 1. Supply Current vs Supply Voltage

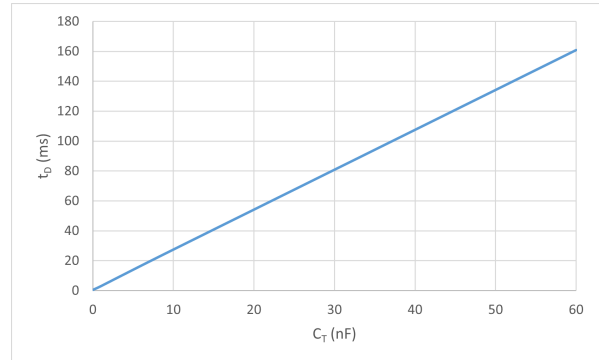


Figure 2. Reset Delay Time vs C_T

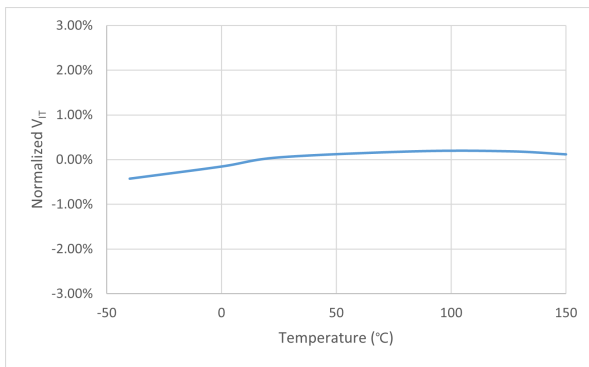


Figure 3. Normalized Threshold Voltage vs Temperature

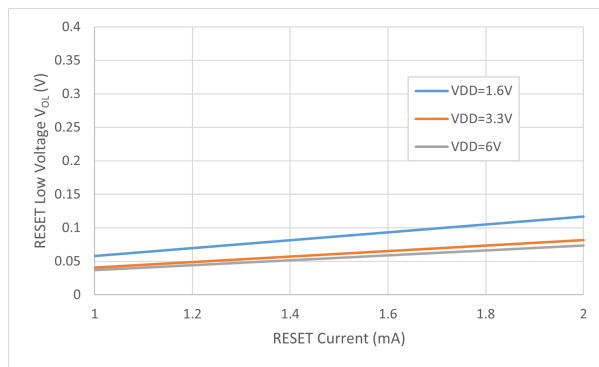


Figure 4. Low-level Reset Voltage vs Reset Current

Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

Detailed Description

Overview

The TPV8318 is a family of supervisory circuits to monitor a voltage rail from 1.6 V to 6 V, asserting an active low open drain $\overline{\text{RESET}}$ output when the VDD voltage drops below the reset threshold, or when manual reset pin MR is logic low. The $\overline{\text{RESET}}$ output remains low for the user adjusted delay time by an external capacitor after the VDD voltage returns above the fixed threshold with a hysteresis, or manual reset MR returns to logic high.

Functional Block Diagram

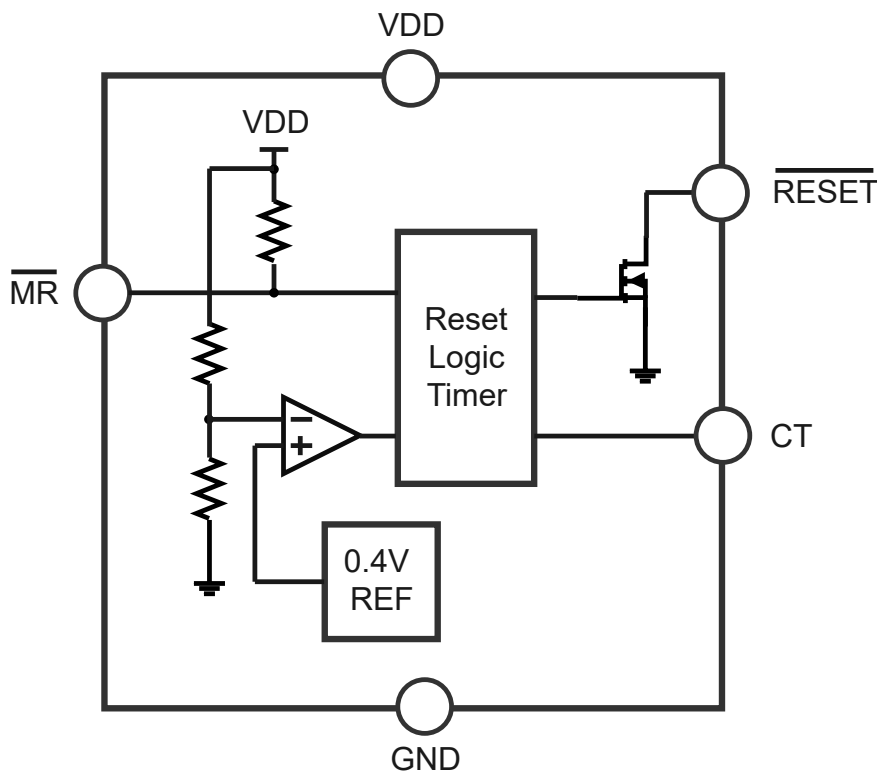


Figure 5. Functional Block Diagram

Feature Description

RESET Output

The reset threshold voltage can be set by the factory from 1.6 V to 4.2 V. The VDD pin monitors the system voltage. If the voltage on this pin drops below V_{IT} , the $\overline{\text{RESET}}$ is asserted.

The TPV8318 features an active-low output. For active-low output, the reset signal is guaranteed to be logic low for VDD down to V_{IT} . Reset remains asserted for the duration of the reset delay time (t_D) after VDD rises above the reset threshold. [Figure 6](#) shows the reset outputs.

Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

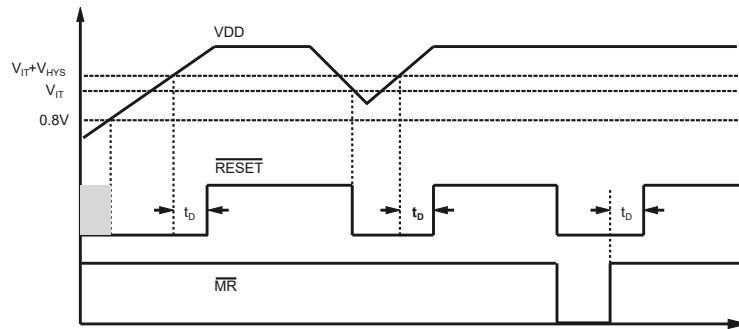


Figure 6. Reset and MR Reset Timing

RESET Delay Time

The TPV8318 provides programmable reset delay time (t_D), which is realized by selecting a capacitor between CT and GND to allow the designer to set any reset delay time from 43 μs to 150 ms. The reset delay time (t_D) under a given capacitor value is calculated using [Equation 1](#).

$$t_D (\mu\text{s}) = 2.7 \times 10^6 \times C_{CT} (\mu\text{F}) + 430 (\mu\text{s}) \quad (1)$$

Manual RESET ($\overline{\text{MR}}$) Input

The manual reset ($\overline{\text{MR}}$) input allows a microcontroller to initiate a reset. A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to logic high, $\overline{\text{RESET}}$ is de-asserted after the reset delay time. $\overline{\text{MR}}$ can be left unconnected if not used.

Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPV8318 is a family of supervisory circuits to monitor a voltage rail from 1.6 V to 6 V, asserting an active low open drain $\overline{\text{RESET}}$ output when VDD voltage drops below the reset threshold or when manual reset pin $\overline{\text{MR}}$ is logic low. The $\overline{\text{RESET}}$ output remains low for the user-adjusted delay time by an external capacitor after the VDD voltage returns above the fixed threshold with a 150-mV hysteresis or manual reset $\overline{\text{MR}}$ returns to logic high.

Typical Application

Figure 7 shows the typical application schematic.

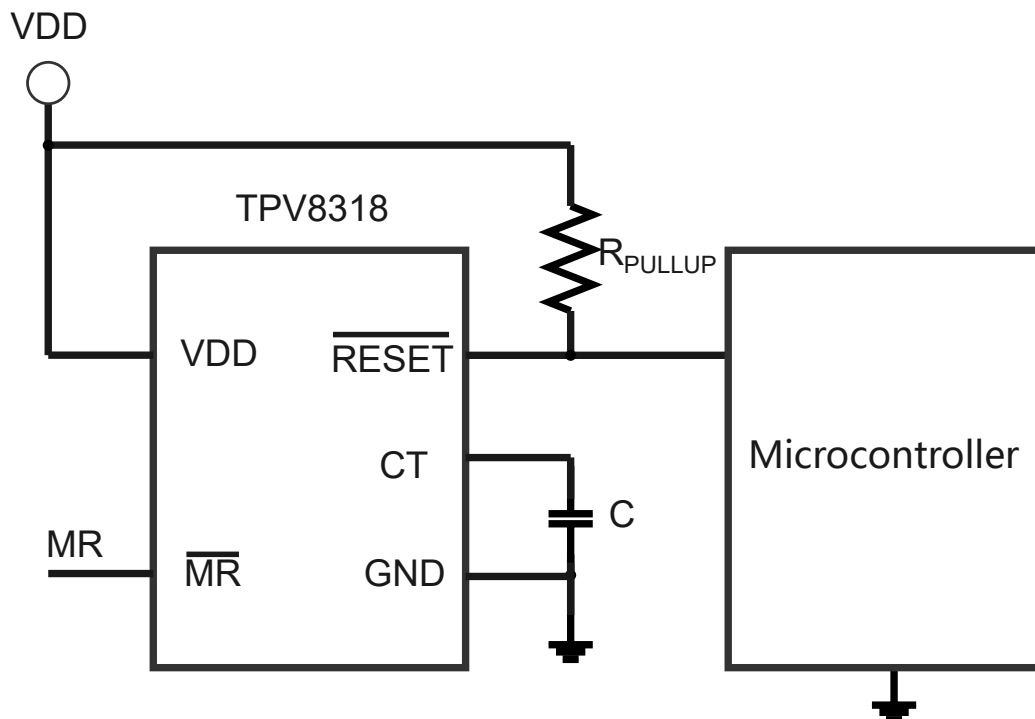
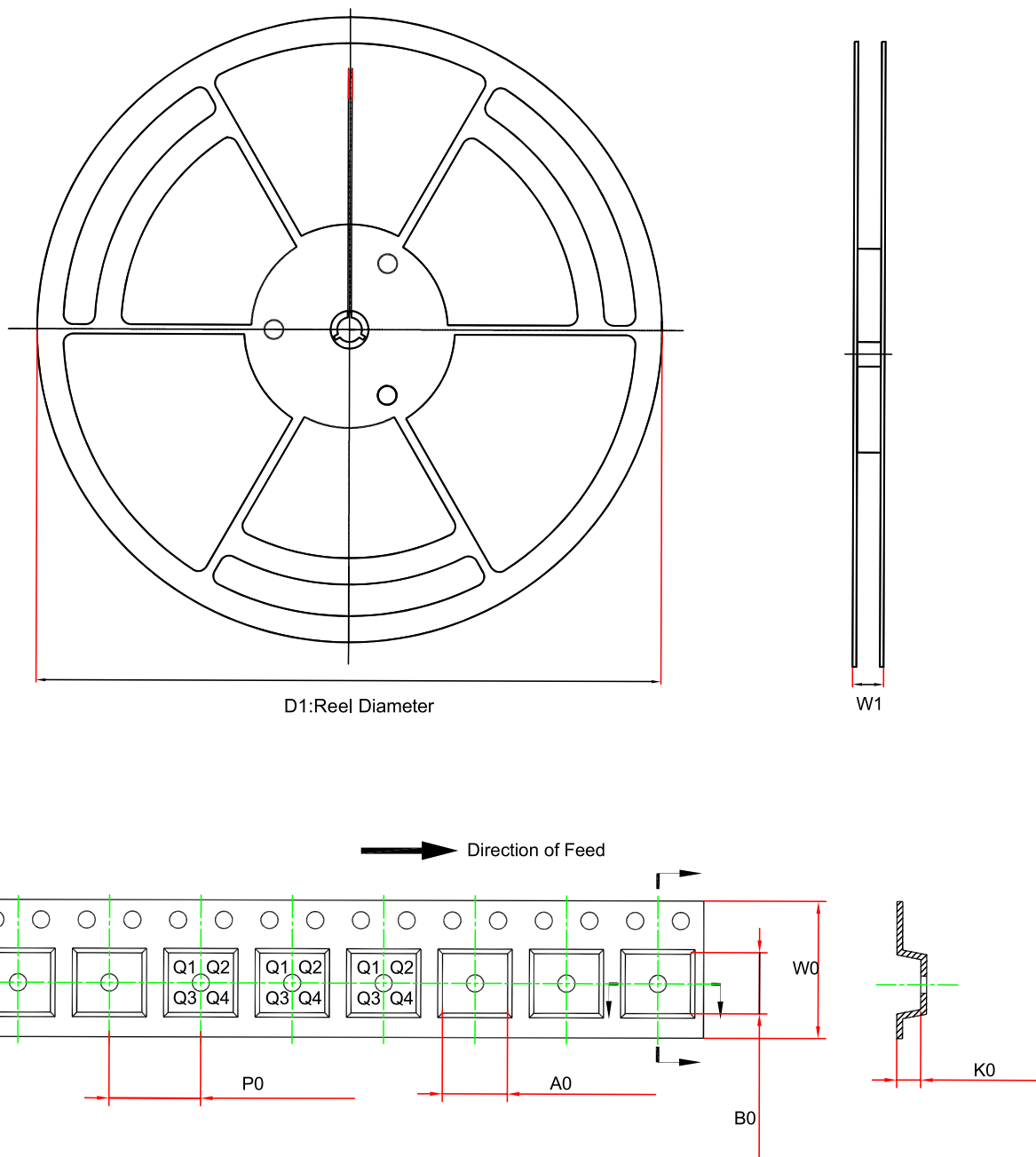


Figure 7. Typical Application Circuit

Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

Tape and Reel Information

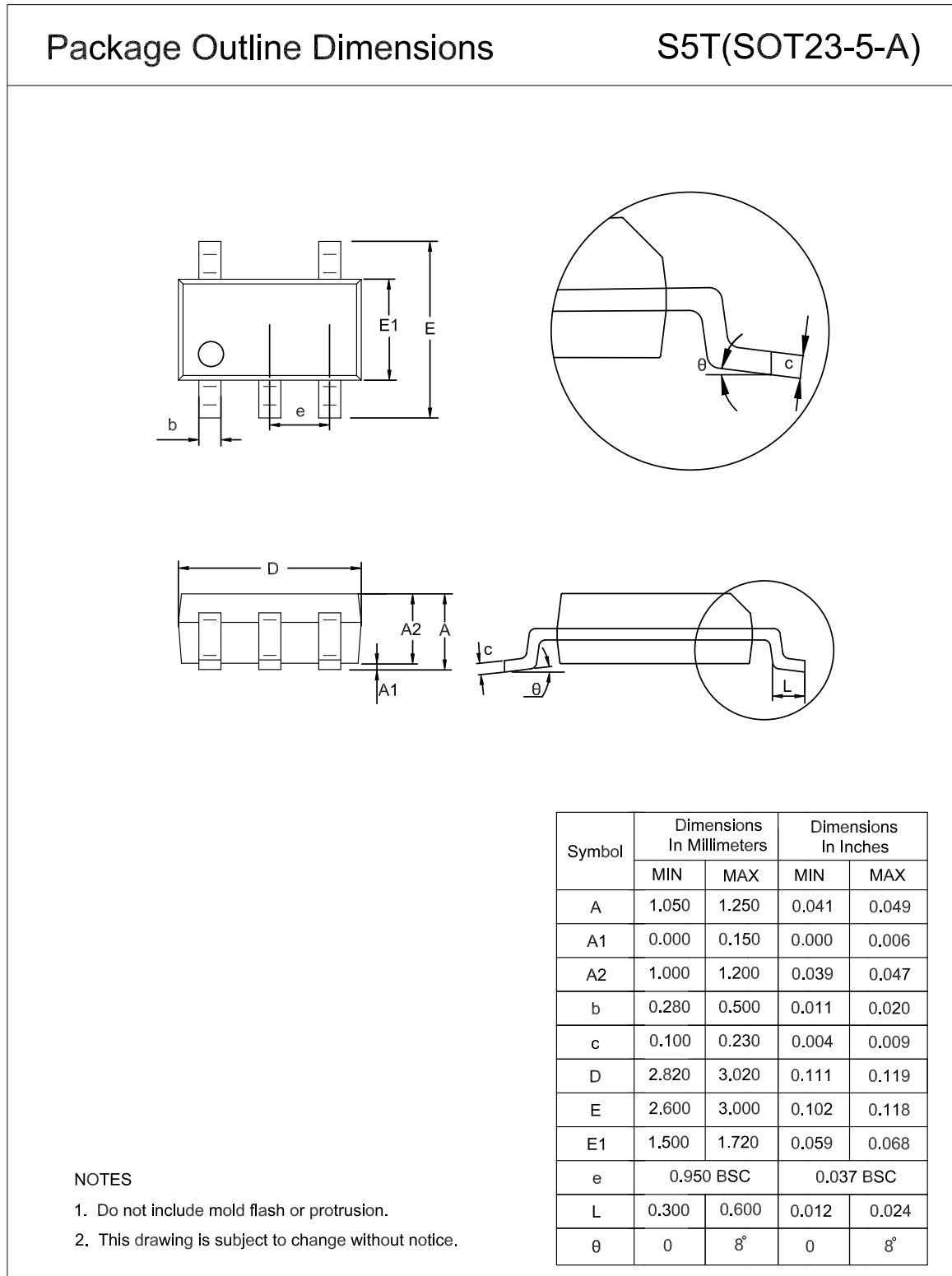


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPV8318LDxx x-S5TR-S	SOT23-5	180.0	13.1	3.2	3.2	1.4	4	8	Q3

Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

Package Outline Dimensions

SOT23-5



Low Quiescent Current Supervisory Circuits with Programmable Reset Delay**Order Information**

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPV8318LD300-S5TR-S	-40 to 125°C	SOT23-5	L30	3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

**Low Quiescent Current Supervisory Circuits with Programmable
Reset Delay****IMPORTANT NOTICE AND DISCLAIMER**

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