Auto Grade Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

Features

- Qualified for Automotive Applications
  - AEC-Q100 Grade 1: T_A=−40°C to 125°C
- Wide-Supply Voltage Range: 1.6 V to 6.0 V
- Very Low Quiescent Current: 600 nA typ
- Fixed Threshold Voltage from 0.6 V to 5 V with 100 mV Step
- Adjustable Version with Low Threshold Voltage 0.405 V (min)
- Power-on Reset Generator with Adjustable Delay Time from 1.25 ms to 10 s
- High Threshold Accuracy 1% Typ
- Manual Reset $\overline{MR}$ Input
- Open-drain Active Low $\overline{RESET}$ Output
- Green Product, SOT23-6 Package

Applications

- DSP or Microcontroller Applications
- FPGA and ASIC Applications
- Automotive Radar
- T-box
- Automotive Vision

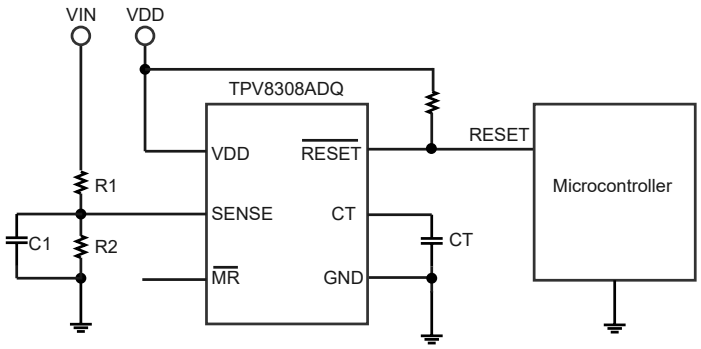
Description

The TPV8308Q is a family of auto-grade supervisory circuits to monitor a voltage rail from 0.405 V to 5 V, asserting an active low open-drain $\overline{RESET}$ /RESET output when the voltage of the sense pin drops below a fixed threshold or when the manual reset pin $\overline{MR}$ is logic low. The $\overline{RESET}$ output remains low for the user-adjusted delay time by the external capacitor after the sense voltage returns above the fixed threshold with a hysteresis and the manual reset MR returns to logic high.

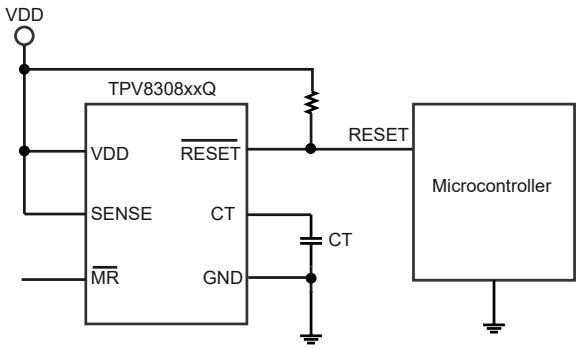
The threshold voltage of the TPV8308Q device can achieve 1% accuracy. The delay time can be set to 1.25 ms to 10 s by connecting the external capacitor to the CT pin. The TPV8308Q family has a very low typical quiescent current of 600 nA.

The TPV8308Q is available in the SOT23-6 package. Its operating temperature range is from −40°C to +125°C.

Typical Application Circuit



TPV8308Q Adjustable Version Typical Application Circuit



TPV8308Q Fixed Version Typical Application Circuit

Table of Contents

Product Family Table

Order Number	Threshold Voltage (V_{IT})	Nominal Monitored Voltage	Marking	Package
TPV8308ADQ-S6TR-S	0.405 V	Adjustable	QAJ	SOT23-6
TPV830816Q-S6TR-S	1.6 V	1.8 V	Q16	SOT23-6
TPV830830Q-S6TR-S	3.0 V	3.3 V	Q30	SOT23-6

Revision History

Date	Revision	Notes
2024-10-30	Rev.A.0	Initial version

Pin Configuration and Functions

TPV8308Q
SOT23-6 Package
Top View

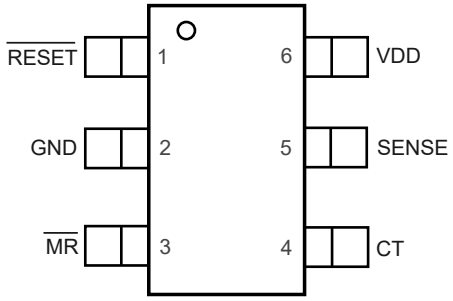


Table 1. Pin Functions: TPV8308Q

Pin No.	Name	I/O	Description
1	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$ Output. This pin is active low open drain output. It is driven to a low impedance state when $\overline{\text{RESET}}$ is asserted by the voltage of the sense pin lower than the threshold V_{IT}, or $\overline{\text{MR}}$ pin is low. $\overline{\text{RESET}}$ will keep low for the reset delay time programmed by the CT pin after both of the sense pin is above V_{IT} and $\overline{\text{MR}}$ pin is high. A pulled-up resistor from 10 kΩ to 1 MΩ should be connected to VDD if it is open drain output.
2	GND	G	Ground. This pin should be connected to ground reference.
3	$\overline{\text{MR}}$	I	Manual Reset Input $\overline{\text{MR}}$ low asserts $\overline{\text{RESET}}$ pin. $\overline{\text{MR}}$ is internal tied to VDD by a 90 kΩ pull-up resistor.
4	CT	I/O	Reset Delay Time Programming Pin. Connecting this pin to VDD through a 40 kΩ to 200 kΩ resistor or leaving it open results in fixed reset delay times. Connecting this pin to ground referenced capacitor (≥ 100 pF) gives a user-programmable reset delay time.
5	SENSE	I	Sense Pin. It is used for monitoring voltage. If the voltage drops below the threshold voltage VIT, the $\overline{\text{RESET}}$ is asserted. The sense pin can be connected to any voltage by configuring an external resistor divider.
6	VDD	P	Supply Voltage. A 0.1-μF ceramic capacitor was placed as close as to the VDD pin.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Power Supply, V_{DD} to GND		−0.3	6.5	V
V_{CT}	Input Voltage for CT, $\overline{MR}$, $\overline{RESET}$ pin	−0.3 to V_{DD} + 0.3 V, max 6 V		
V_{RESET}				
V_{MR}				
V_{SENSE}	Input Voltage for SENSE Pin	−0.3	6.5	V
I_{RESET}	Current of $\overline{RESET}$ Pin		5	mA
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		300	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-6	128.8	67	°C/W

Electrical Characteristics

All test conditions: V_{DD} = 5 V, T_A = −40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

Parameter			Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range		−40°C < T_A < 125°C	1.6		6.0	V
$V_{DD(min)}$	Minimum VDD to Guaranteed $\overline{RESET}$ Output Valid (1)				0.5	0.8	V
I_{DD}	Quiescent Current (I_Q)		V_{DD} = 5.5V, $\overline{RESET}$ not asserted, $\overline{MR}$, $\overline{RESET}$, CT pin open		0.6	1.5	μA
V_{OL}	Output Low Voltage of $\overline{RESET}$ Pin		1.6 V ≤ V_{DD} < 6.0 V, I_{OL} = 2.0 mA			0.3	V
$V_{IT,ERR}$	Negative-going Input Threshold Accuracy		−40°C < T_A < 125°C	−3	±1	3	%
V_{HYS}	Hysteresis on V_{IT}		1.6 ≤ V_{DD} ≤ 4.2 V		1.0	3.0	%
			4.2 ≤ V_{DD} ≤ 6.0 V		1.75	3.75	%
R_{MR}	MR Internal Pull-up Resistance				90		kΩ
I_{SENSE}	Input Current at SENSE Pin	TPV8308ADQ	V_{SENSE} = V_{IT}		5		nA
		Fixed version	V_{SENSE} = 5.5 V		110		nA
I_{OH}	$\overline{RESET}$ Leakage Current		V_{RESET} = 5.5 V			300	nA
C_{IN}	Input Capacitance, any pin	CT pin	V_{IN} = 0 V to V_{DD}		5		pF
		Other pins	V_{IN} = 0 V to 6.0 V		5		pF
V_{IL}	$\overline{MR}$ Logic Low Input			0		0.3V_{DD}	
V_{IH}	$\overline{MR}$ Logic High Input			0.7V_{DD}		V_{DD}	
Switching Electrical Specifications							
t_w	Input Pulse Width to Assert $\overline{RESET}$ Pin	SENSE	V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		12		μs
		$\overline{MR}$	V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		300		ns
t_D	Reset Delay Time	C_T = Open	Guaranteed by design and characterization		20		ms
		C_T = V_{DD}			300		ms
		C_T = 100 pF			1.25		ms
		C_T = 180 nF			1200		ms
t_{P1}	Propagation Delay from $\overline{MR}$	$\overline{MR}$ to $\overline{RESET}$	V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		300		ns
t_{P2}	Propagation Delay from SENSE	SENSE to $\overline{RESET}$	V_{IH} = 1.05 V_{DD}, V_{IL} = 0.95 V_{DD}		12		μs

(1) Guaranteed by bench test.

Typical Performance Characteristics

All test conditions: V_{DD} = 5 V, T_A = + 25°C, unless otherwise noted.

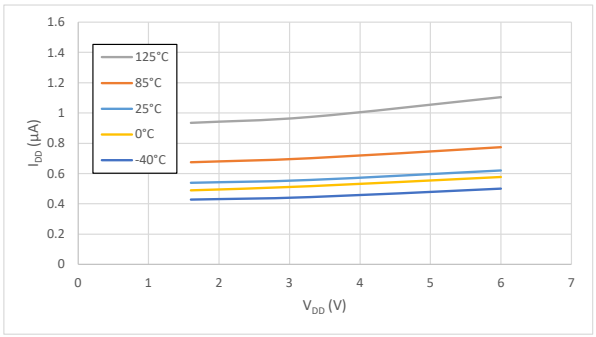


Figure 1. Supply Current vs. Supply Voltage

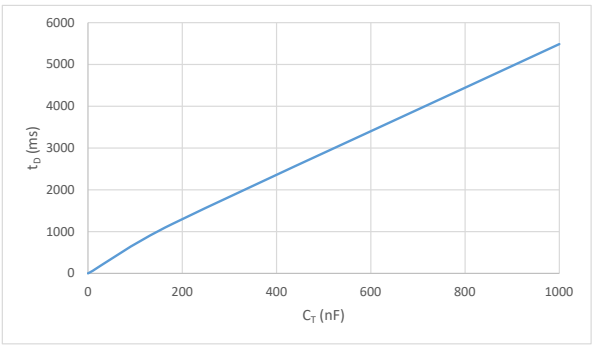


Figure 2. Reset Delay Time vs. C_T

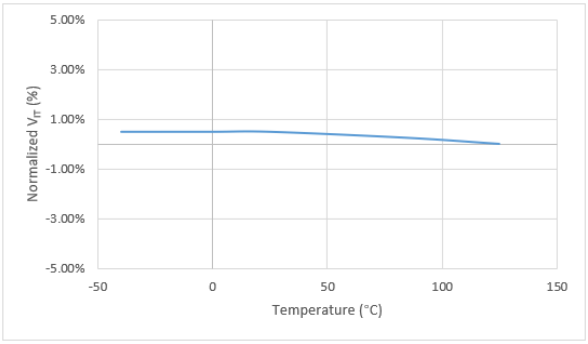


Figure 3. Normalized Sense Threshold Voltage vs. Temperature

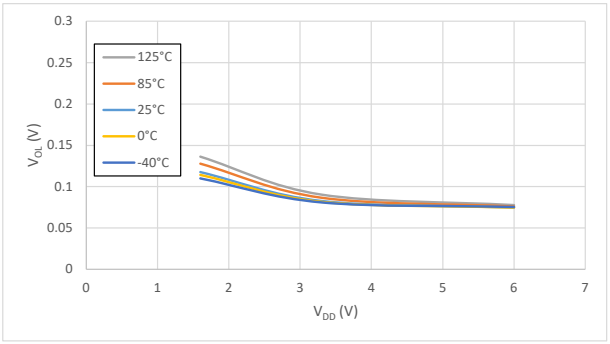


Figure 4. Low-level Reset Voltage vs. Supply Voltage

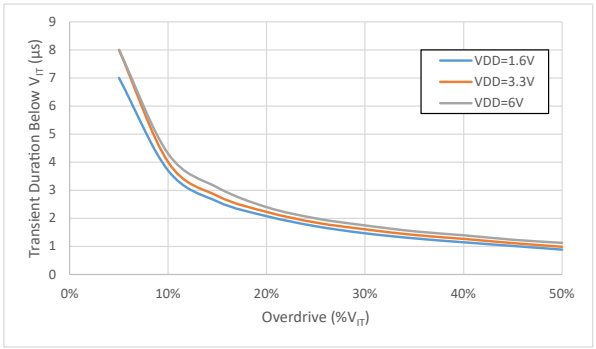


Figure 5. Sense Maximum Transient Duration vs. Threshold Overdrive Voltage

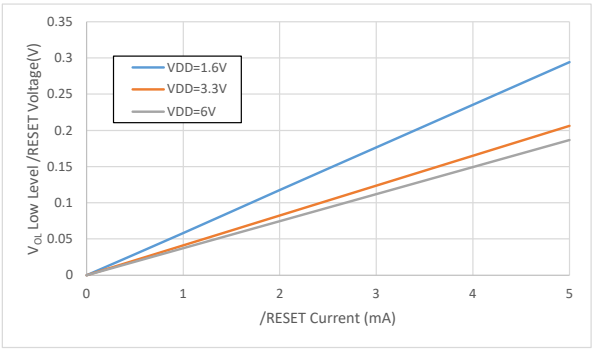


Figure 6. Low-level Reset Voltage vs. Reset Current

Detailed Description

Overview

The TPV8308Q is a family of auto-grade supervisory circuits to monitor a voltage rail from 0.405 V to 5 V, asserting an active low open-drain $\overline{\text{RESET}}$ output when the voltage of the sense pin drops below a fixed threshold or when the manual reset pin $\overline{\text{MR}}$ is logic low. The $\overline{\text{RESET}}$ output remains low for the user-adjusted delay time by an external capacitor after the sense voltage returns above the fixed threshold with a hysteresis and the manual reset $\overline{\text{MR}}$ returns to logic high.

Functional Block Diagram

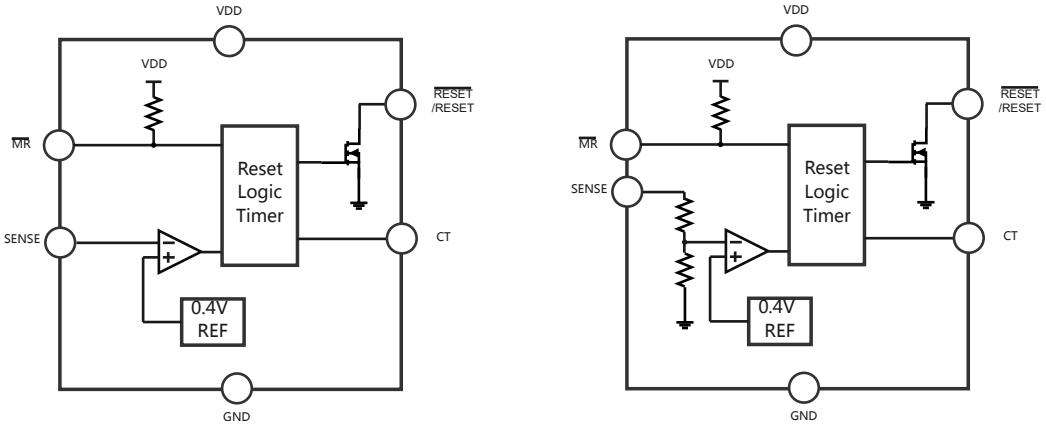


Figure 7. Functional Block Diagram

Feature Description

RESET Output

The reset threshold voltage can be set by the factory from 0.6 V to 5.0 V or be set to any voltage above 0.405 V using an external resistor divider. The sense pin monitors the system voltage. If the voltage on this pin drops below V_{IT}, the $\overline{\text{RESET}}$ is asserted.

The TPV8308Q features an active-low output. For active-low output, the reset signal is guaranteed to be logic low for VSENSE down to V_{IT}. Reset remains asserted for the duration of the reset delay time (t_D) after VSENSE rises above the reset threshold. Figure 8 shows the reset outputs.

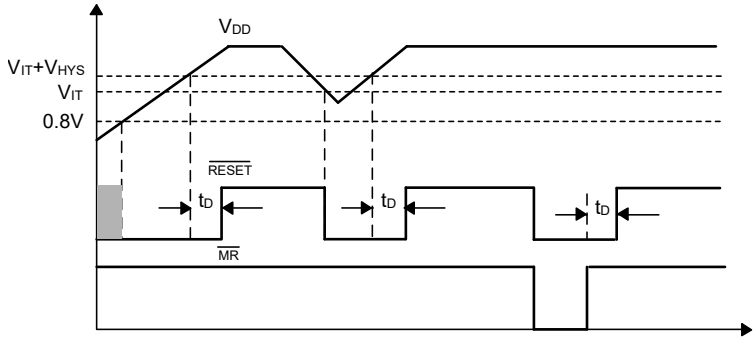


Figure 8. SENSE Reset and MR Reset Timing

RESET Delay Time

The TPV8308 provides programmable reset delay time (t_D), which is realized by selecting a capacitor between CT and GND to allow the designer to set any reset delay time from 1.25 ms to 10 s. The reset delay time (t_D) under a given capacitor value is calculated using Equation 1.

$$t_D\,(\mu s) = 6 \times C_{CT}\,(pF) + 500\ (\mu s) \quad (1)$$

Manual RESET ($\overline{MR}$) Input

The manual reset ($\overline{MR}$) input allows a microcontroller to initiate a reset. A logic low on $\overline{MR}$ causes $\overline{RESET}$ to assert. After $\overline{MR}$ returns to logic high and SENSE is above the reset threshold, $\overline{RESET}$ is de-asserted after the reset delay time. $\overline{MR}$ can be left unconnected if not used.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Figure 9 shows the typical application circuit of TPV8308Q with a reset threshold voltage set by the external resistor divider. Figure 10 shows the application circuit of TPV8308Q with the reset threshold voltage set by the factory.

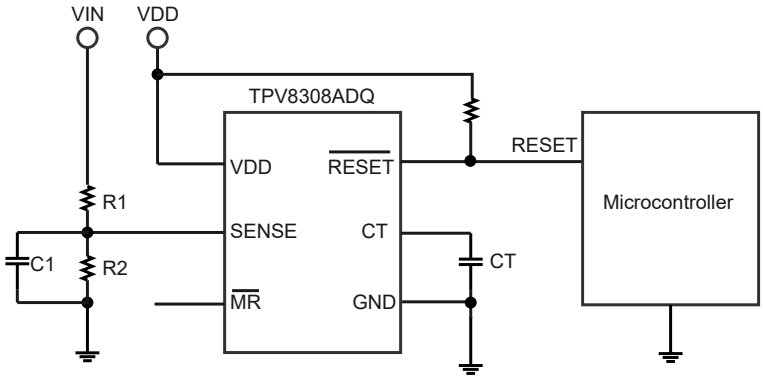


Figure 9. TPV8308 Adjustable Version Typical Application Circuit

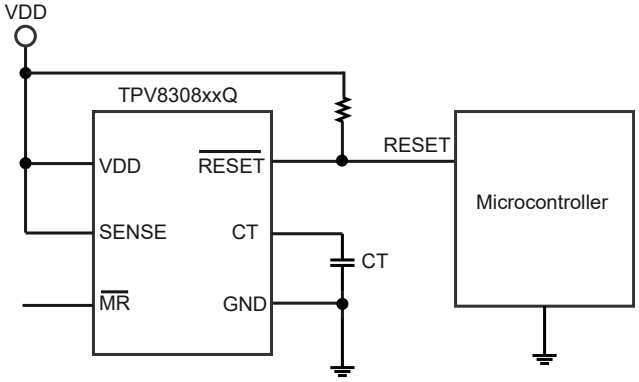
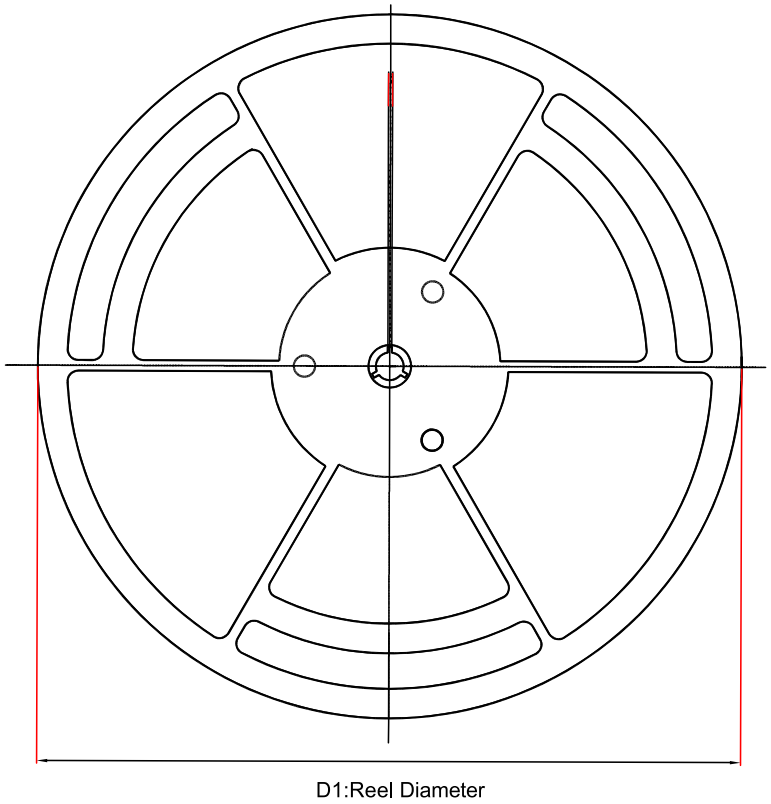
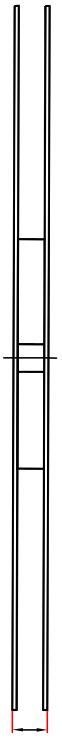
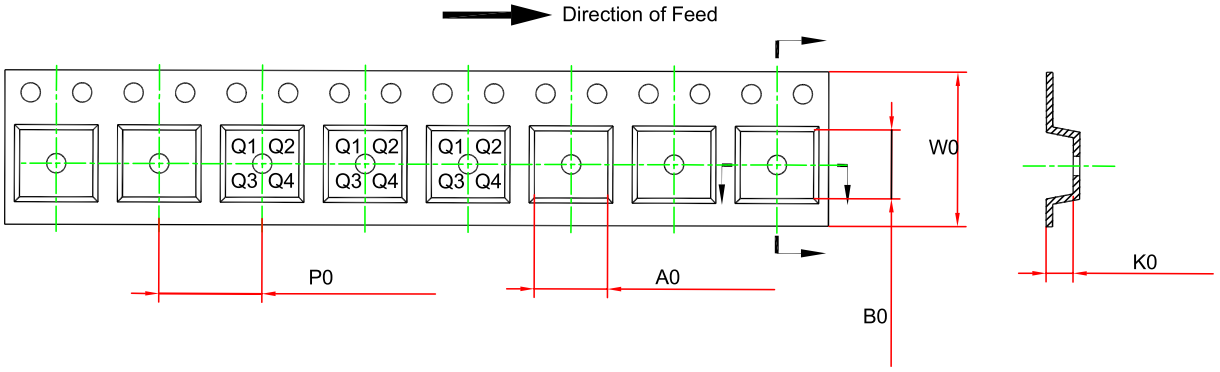


Figure 10. TPV8308 Fixed Version Typical Application Circuit

Tape and Reel Information





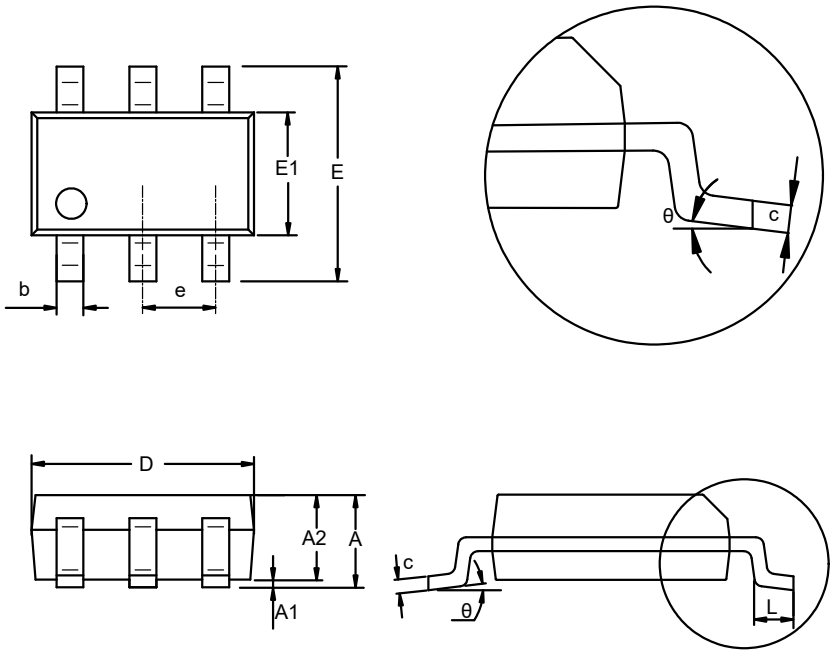


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPV8308xxQ-S6TR-S	SOT23-6	180	12	3.3	3.2	1.4	4	8	Q3

Package Outline Dimensions

SOT23-6

Package Outline Dimensions S6T(SOT23-6-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPV8308ADQ-S6TR-S	−40 to 125°C	SOT23-6	QAJ	3	Tape and Reel, 3000	Green
TPV830816Q-S6TR-S	−40 to 125°C	SOT23-6	Q16	3	Tape and Reel, 3000	Green
TPV830830Q-S6TR-S	−40 to 125°C	SOT23-6	Q30	3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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