

Features

- Precision Low-Voltage Monitoring and Power-Fail Detector
- 200-ms (typical) Reset Timeout
- Manual Reset Input
- Active High and Active Low Reset Output
- Low Power Consumption: 4 μ A
- Guaranteed Reset Output Valid to VCC = 1 V
- Power Supply Glitch Immunity
- Temperature Range: -40°C to 125°C
- 8-Pin SOP Package

Applications

- Microprocessor Systems
- Computers
- Controllers
- Intelligent Instruments
- Portable Equipment

Description

The TPV708 is a family of supervisory circuits to monitor power supply voltage levels and provides a power-on reset signal.

A reset signal can be asserted by an external manual reset input.

In addition, there is a power-fail detector with a 1.25-V threshold, which can be used to monitor an additional power supply.

The reset periods are fixed at 200 ms (typical). The TPV708 is available in an 8-pin SOP package and typically consumes only 4 μ A, which is suitable for low-power and portable applications.

Typical Application Circuit

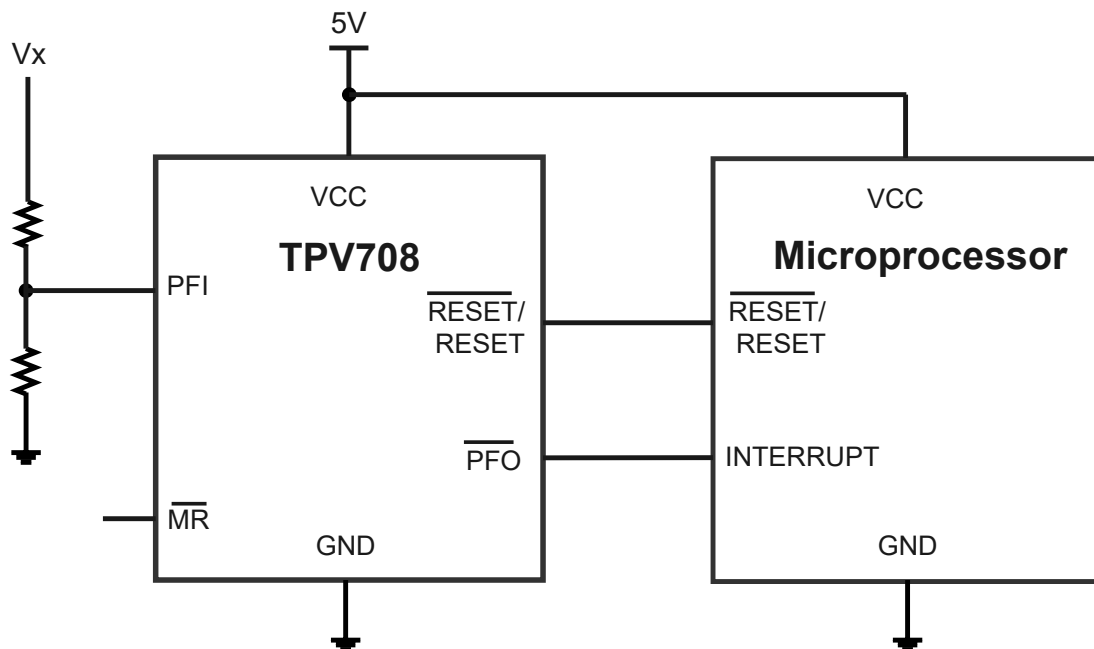


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Product Family Table

Order Number	Threshold Voltage (V_{TH})	Marking	Package
TPV708V-SO1R ⁽¹⁾	1.58 V	V8V	SOP8
TPV708W-SO1R ⁽¹⁾	1.67 V	V8W	SOP8
TPV708Y-SO1R ⁽¹⁾	2.19 V	V8Y	SOP8
TPV708Z-SO1R ⁽¹⁾	2.32 V	V8Z	SOP8
TPV708R-SO1R ⁽¹⁾	2.63 V	V8R	SOP8
TPV708S-SO1R	2.93 V	V8S	SOP8
TPV708T-SO1R	3.08 V	V8T	SOP8
TPV708M-SO1R	4.38 V	V8M	SOP8
TPV708L-SO1R ⁽¹⁾	4.63 V	V8L	SOP8

(1) For future products, contact the 3PEAK factory for more information and samples.

Revision History

Date	Revision	Notes
2022-01-26	Rev.Pre.0	Pre-Release Version.
2022-10-21	Rev.Pre.1	Updated V_{TH} in EC.
2022-10-30	Rev.Pre.2	Updated M version V_{TH} in EC.
2022-12-05	Rev.Pre.3	Updated MR to reset delay time, typical 2 μ s, max 10 μ s.
2022-12-20	Rev.A.0	Updated typical application circuit.
2023-02-17	Rev.A.1	Corrected typo.

Pin Configuration and Functions

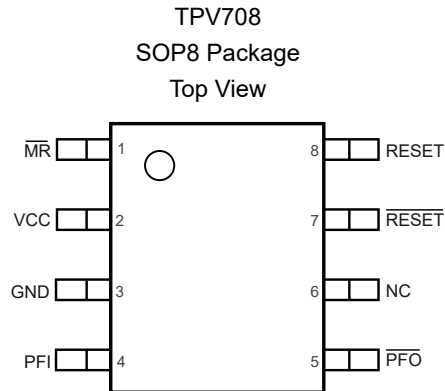


Table 1. Pin Functions: TPV708

Pin		I/O	Description
No.	Name		
1	$\overline{\text{MR}}$	I	Manual Reset Input. $\overline{\text{MR}}$ low asserts $\overline{\text{RESET}}/\text{RESET}$ pin. It features an internal pull-up current.
2	VCC	P	Power supply voltage being monitored.
3	GND	G	Ground. This pin should be connected to ground reference.
4	PFI	I	Power fail input. When PFI is less than 1.25 V, $\overline{\text{PFO}}$ goes low. If unused, connect PFI to GND.
5	$\overline{\text{PFO}}$	O	Power fail output. It goes low when PFI is less than 1.25 V, otherwise stays high.
6	NC	-	Not connected.
7	$\overline{\text{RESET}}$	O	Active low reset push-pull output stage. Asserted whenever VCC is below the reset threshold or by low signal on the $\overline{\text{MR}}$ input. It remains low for 200 ms after VCC goes above the reset threshold or $\overline{\text{MR}}$ goes from low to high.
8	RESET	O	Active high reset push-pull output stage. Asserted whenever VCC is below the reset threshold or by low signal on the $\overline{\text{MR}}$ input. It remains high for 200 ms after VCC goes above the reset threshold or $\overline{\text{MR}}$ goes from low to high.

Low-Voltage Supervisory Circuits with Power-Fail Detector

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Power Supply, VCC to GND		-0.3	6	V
Input Voltage	PFI, \overline{MR}	-0.3	6	V
Output Current	RESET, \overline{RESET} , PFO		20	mA
T _J	Maximum Junction Temperature	-40	150	°C
T _A	Operating Temperature Range	-40	125	°C
T _{STG}	Storage Temperature Range	-65	150	°C
T _L	Lead Temperature (Soldering 10 sec)		300	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) This data was taken with the JEDEC low effective thermal conductivity test board.

(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8	143	60	°C/W

Low-Voltage Supervisory Circuits with Power-Fail Detector
Electrical Characteristics

 All test conditions: $V_{CC} = 5\text{ V}$, $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit	
V_{CC}	Supply Voltage Range	$-40^\circ\text{C} < T_A < 125^\circ\text{C}$	1		5.5	V	
I_{CC}	Quiescent Current	\overline{MR} is unconnected ($V_{CC} = 1.8\text{ V}$)		4	15	μA	
		\overline{MR} is unconnected ($V_{CC} = 5\text{ V}$)		6	20	μA	
V_{TH}	Reset Threshold Voltage of V_{CC}	TPV708V-SO1R		1.51	1.58	1.63	V
		TPV708W-SO1R		1.62	1.67	1.71	V
		TPV708Y-SO1R		2.12	2.19	2.25	V
		TPV708Z-SO1R		2.25	2.32	2.38	V
		TPV708R-SO1R		2.55	2.63	2.70	V
		TPV708S-SO1R		2.82	2.93	3.00	V
		TPV708T-SO1R		3.00	3.08	3.15	V
		TPV708M-SO1R		4.18	4.38	4.47	V
	TPV708L-SO1R		4.50	4.63	4.75	V	
	V_{TH} Temperature Coefficient			80		ppm/ $^\circ\text{C}$	
V_{HYS}	Hysteresis on V_{TH}	$1.6 \leq V_{DD} \leq 4.2\text{ V}$		$2 \times V_{TH}$		mV	
t_{RD}	V_{CC} Falling to Reset Delay Time	$V_{TH} - V_{CC} = 100\text{ mV}$		20		μs	
t_{RP}	Reset Timeout Period		140	200	280	ms	
V_{OL}	$\overline{RESET}/\overline{RESET}$ Output Low	$V_{CC} \geq 1\text{ V}$, $I_{SINK} = 50\ \mu\text{A}$			0.3	V	
		$I_{SINK} = 1.2\text{ mA}$, $V_{CC} \geq 2\text{ V}$			0.4	V	
V_{OH}	$\overline{RESET}/\overline{RESET}$ Output Low	$I_{SOURCE} = 800\ \mu\text{A}$, $V_{CC} \geq 5\text{ V}$	$0.7 \times V_{CC}$			V	
Manual Reset Function							
V_{IL}	\overline{MR} Logic Low Input		0		$0.3V_{CC}$	V	
V_{IH}	\overline{MR} Logic High Input		$0.7V_{CC}$			V	
t_{PW}	\overline{MR} Input Pulse Width		6			μs	
t_{GR}	\overline{MR} Glitch Rejection				100	ns	
t_{MD}	\overline{MR} to Reset Delay			2	10	μs	
I_{PU}	\overline{MR} Pull-up Current	$V_{CC} = 3\text{ V}$		80		μA	
Power Fail Function							
V_{PF}	Power Fail Input Threshold	PFI falling	1.18	1.25	1.33	V	
V_{OL_PF}	\overline{PFO} Output Low	$I_{SINK} = 1.6\text{ mA}$, $V_{CC} \geq 5\text{ V}$			0.4	V	
V_{OH_PF}	\overline{PFO} Output High	$I_{SOURCE} = 800\ \mu\text{A}$, $V_{CC} \geq 5\text{ V}$	$0.7 \times V_{CC}$			V	

Low-Voltage Supervisory Circuits with Power-Fail Detector

Typical Performance Characteristics

All test conditions: $V_{CC} = 5\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

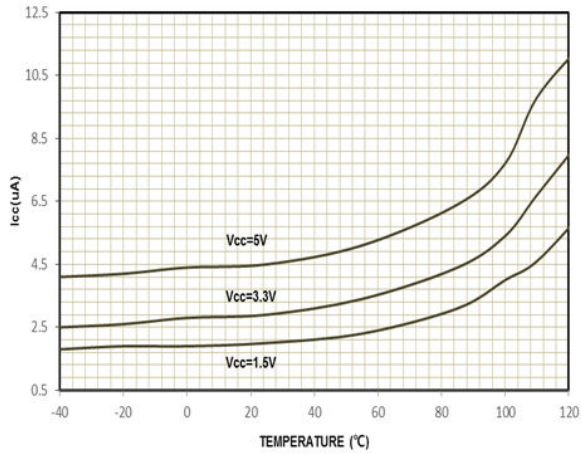


Figure 1. Supply Current vs Temperature

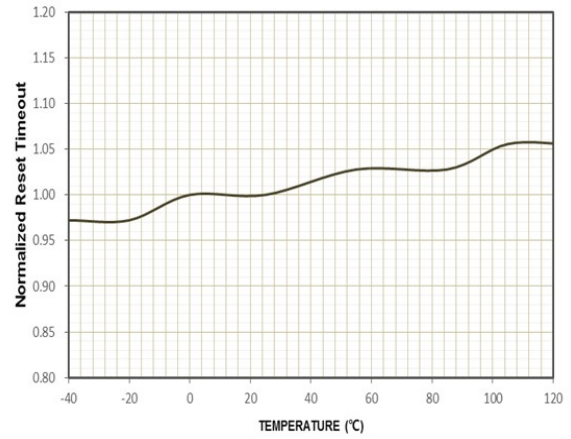


Figure 2. Normalized RESET Timeout Period vs. Temperature

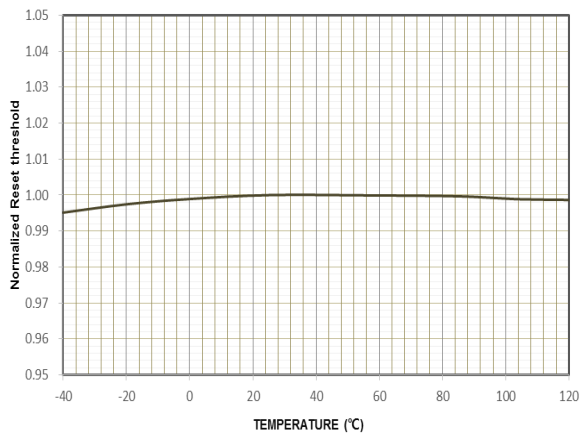


Figure 3. Normalized RESET Threshold vs Temperature

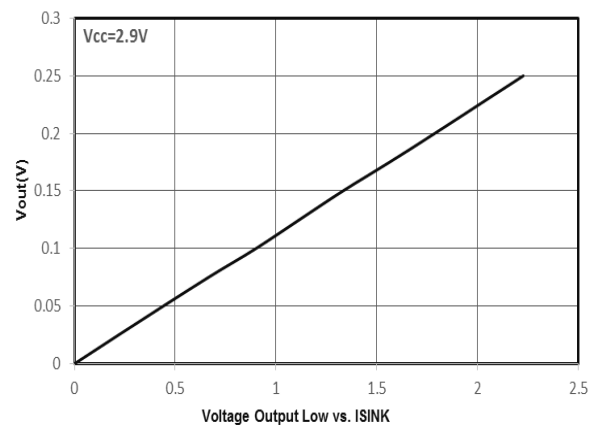


Figure 4. Voltage Output Low vs ISINK

Detailed Description

Overview

The TPV708 series provides supply voltage supervision, manual reset function as well as a 1.25-V power-fail detector.

Functional Block Diagram

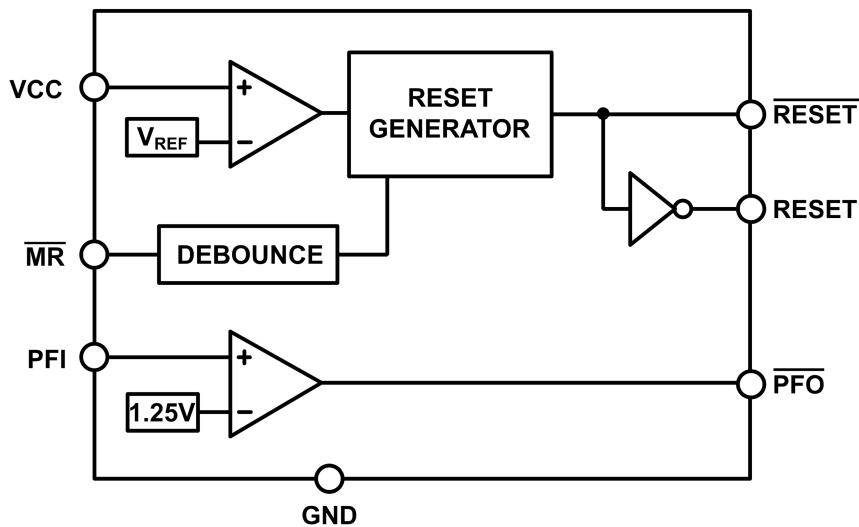


Figure 5. Functional Block Diagram

Feature Description

RESET Output

The TPV708 features an active-low and active-high push-pull output. The reset output is asserted when VCC is below the reset threshold (V_{TH}), or when \overline{MR} is driven low. Reset remains asserted for the duration of the reset delay time (t_{RP}) after VCC rises above the reset threshold, or after \overline{MR} transitions from low to high. Figure 6 shows the reset outputs.

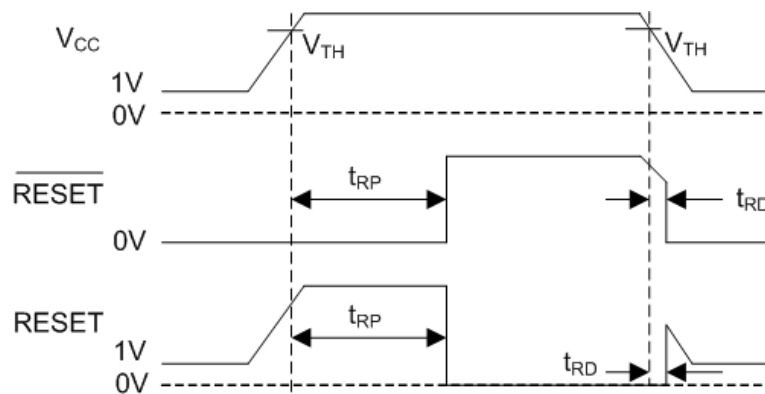


Figure 6. Reset Timing Diagram

Low-Voltage Supervisory Circuits with Power-Fail Detector**Power-Fail Detector**

The power-fail detector is a 1.25-V comparator, which can monitor an external power supply through a resistive divider. When the voltage on the PFI is lower than 1.25 V, the comparator output goes low, indicating a power fail, which can be used as an early warning of the power fail.

Manual RESET ($\overline{\text{MR}}$) Input

The TPV708 features a manual reset input ($\overline{\text{MR}}$), which, when driven low, asserts the reset output. When $\overline{\text{MR}}$ transitions from low to high, reset remains asserted for the duration of the reset active timeout period before de-asserting.

The $\overline{\text{MR}}$ input has an internal pull-up current so that the input is always high when unconnected. Noise immunity is provided on the $\overline{\text{MR}}$ input, and the fast and negative-going transients are ignored. A 0.1- μF capacitor between $\overline{\text{MR}}$ and ground provides additional noise immunity.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Figure 7 shows the typical application circuit of TPV708.

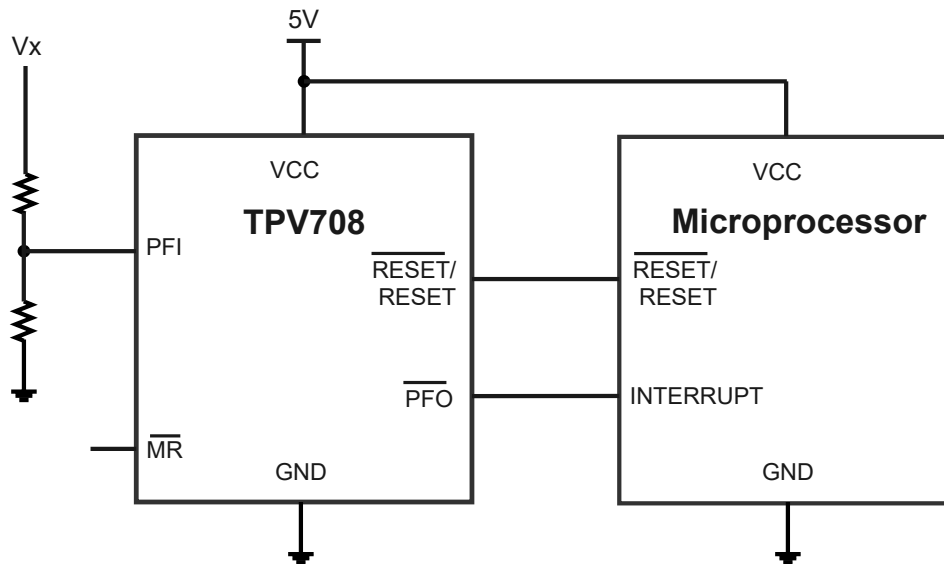
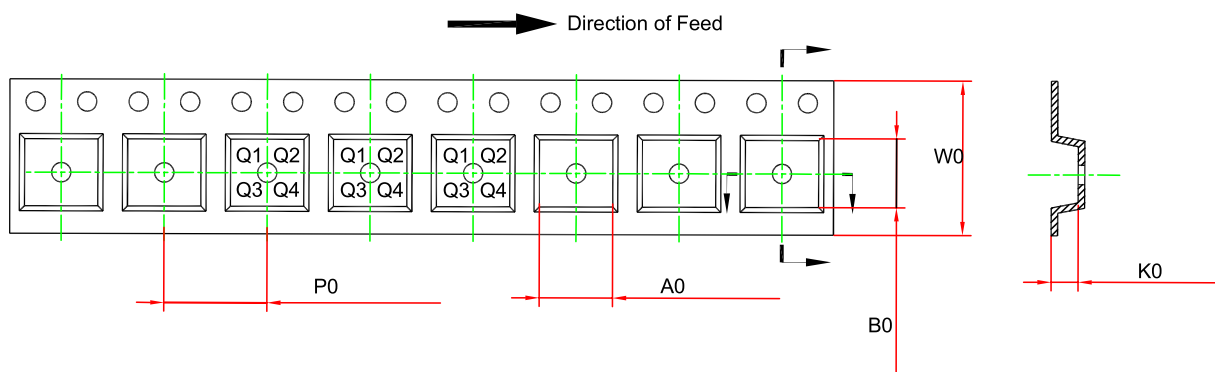
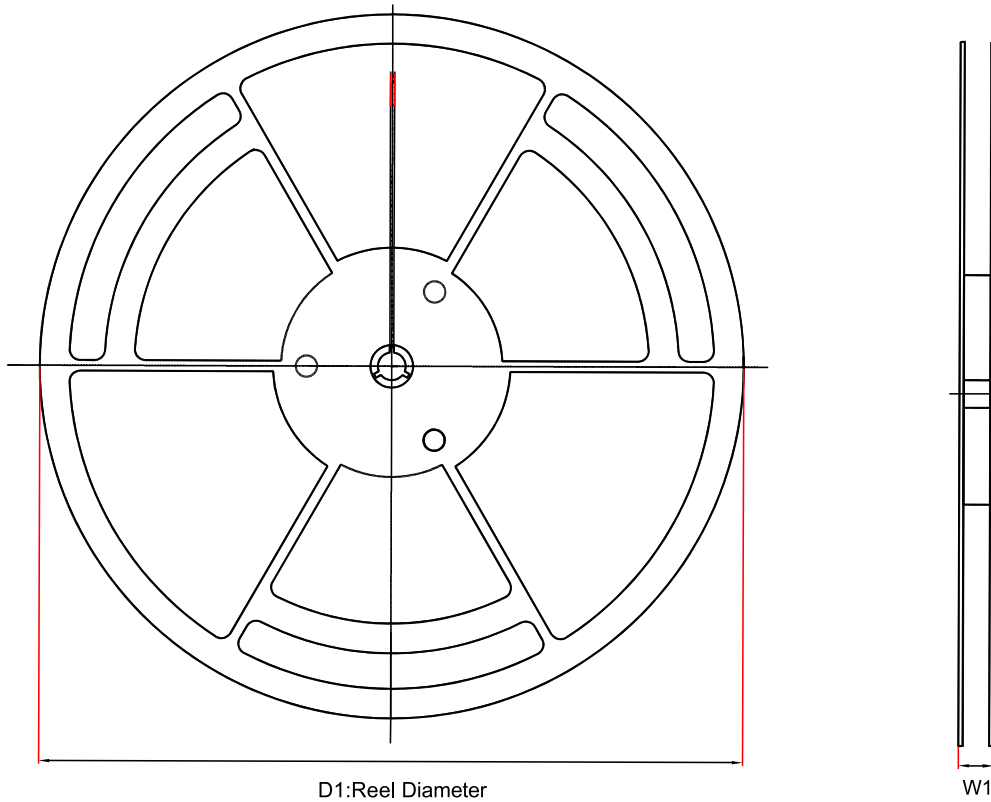


Figure 7. TPV708 Typical Application Circuit

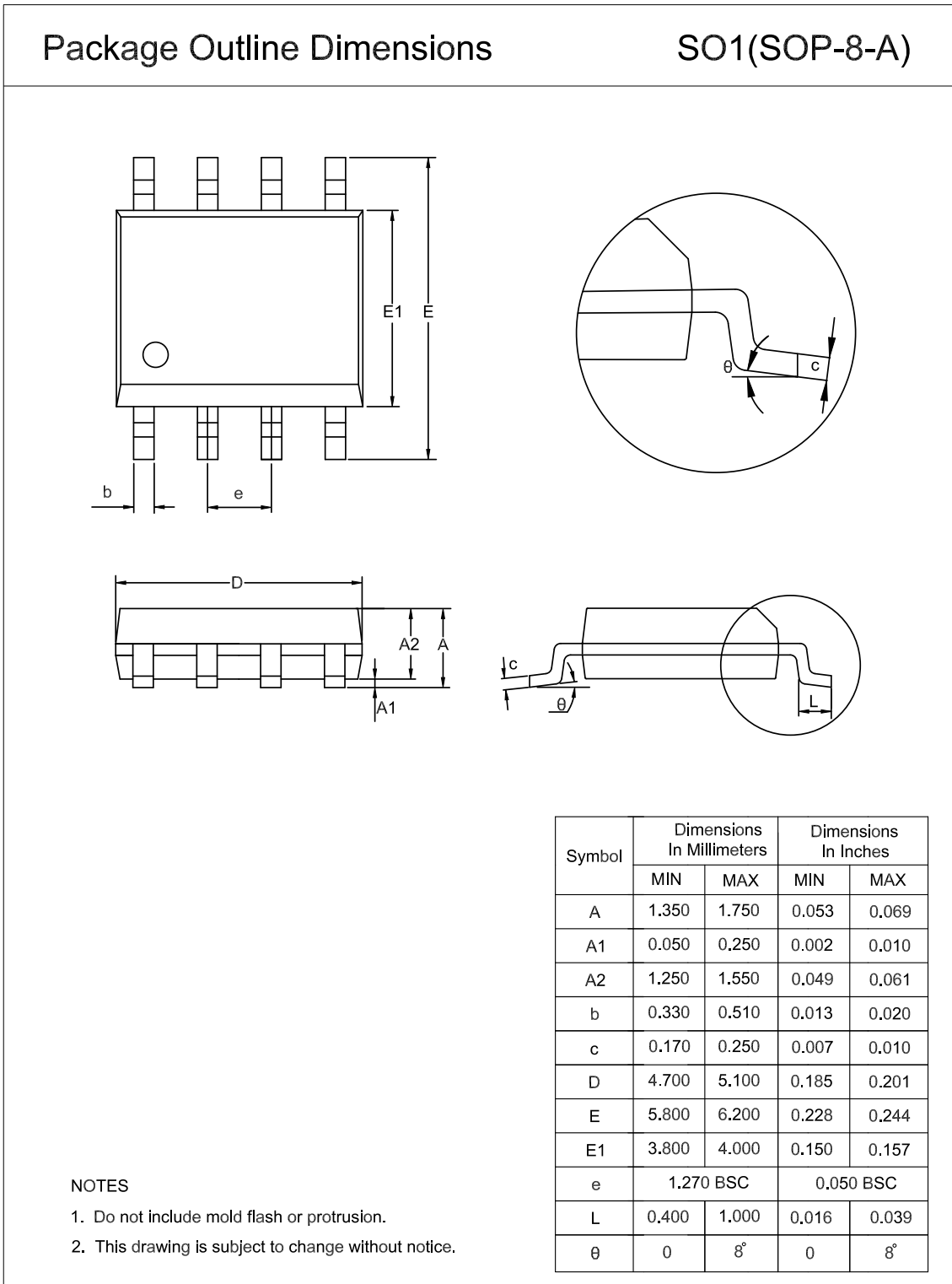
Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPV708x-SO1R	SOP8	330	17.6	6.4	5.4	2.1	8	12	Q1

Package Outline Dimensions

SOP8



Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPV708V-SO1R ⁽¹⁾	-40 to 125°C	SOP8	V8V	1	Tape and Reel, 4000	Green
TPV708W-SO1R ⁽¹⁾	-40 to 125°C	SOP8	V8W	1	Tape and Reel, 4000	Green
TPV708Y-SO1R ⁽¹⁾	-40 to 125°C	SOP8	V8Y	1	Tape and Reel, 4000	Green
TPV708Z-SO1R ⁽¹⁾	-40 to 125°C	SOP8	V8Z	1	Tape and Reel, 4000	Green
TPV708R-SO1R ⁽¹⁾	-40 to 125°C	SOP8	V8R	1	Tape and Reel, 4000	Green
TPV708S-SO1R	-40 to 125°C	SOP8	V8S	1	Tape and Reel, 4000	Green
TPV708T-SO1R	-40 to 125°C	SOP8	V8T	1	Tape and Reel, 4000	Green
TPV708M-SO1R	-40 to 125°C	SOP8	V8M	1	Tape and Reel, 4000	Green
TPV708L-SO1R ⁽¹⁾	-40 to 125°C	SOP8	V8L	1	Tape and Reel, 4000	Green

(1) For future products, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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