Multipoint-LVDS Line Driver and Receiver

Features

- Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange
- Low-Voltage Differential 30-Ω to 55-Ω Line Drivers and Receivers for Signaling Rates, up to 200 Mbps
- Type-2 Receivers Provide an Offset (80 mV) Threshold to Detect Open-Circuit and Idle-Bus
- Conditions:
  - −1-V to 3.4-V Common-Mode Voltage Range
- Allows Data Transfer with 2 V of Ground Noise
- Bus Pins High Impedance when Disabled or V_{CC} ≤ 1.5 V
- Bus-Pin Protection: ±8-kV HBM Model
- −40°C to 85°C Operation Temperature Range

Applications

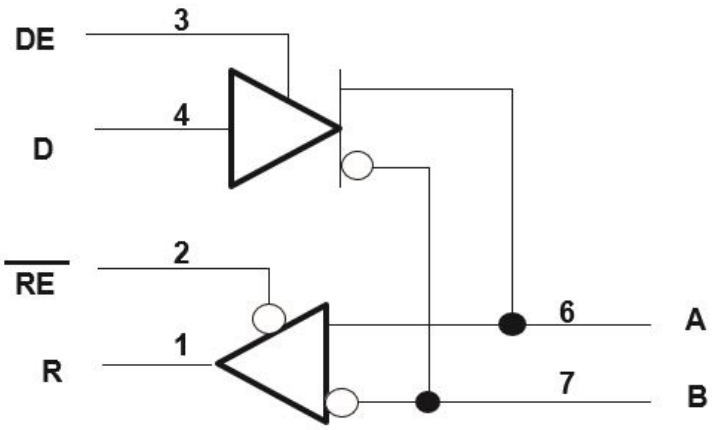
- Backplane Multipoint Data/ Clock Transmission
- Cellular Base Stations
- Network Switches and Routers
- Industrial Control
- Communication Infrastructure

Description

The TPT9H221A is a 3.3-V Multipoint-Low-Voltage Differential (M-LVDS) line driver and receiver, which can operate at signaling rates up to 200 Mbps. Driver outputs and receiver inputs are protected against ±8-kV ESD strikes without latch-up. The driver output has been designed to support multipoint buses presenting loads as low as 30 Ω, and incorporates controlled transition times to allow for stubs off of the backbone transmission line.

The TPT9H221A is a Type-2 receiver that detects the bus state with a differential input of 50 mV over a common-mode voltage range from −1 V to 3.4 V. Type-2 receiver includes an offset threshold to provide a known output state under open-circuit fail-safe, idle-bus fail-safe. The device is characterized for operation from −40°C to 85°C. The device is available as a half-duplex in an 8-pin SOP package.

Typical Application Circuits



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Revision History

Date	Revision	Notes
2024-03-21	Rev. A. 0	Released version

Pin Configuration and Functions

TPT9H221A
SOP8 Package
Top View

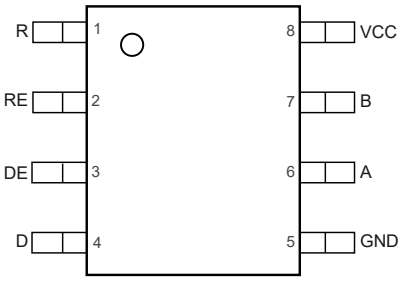


Table 1. Pin Functions: TPT9H221A

Pin No.	Name	I/O	Description
1	R	Digital output	Receiver Output
2	/RE	Digital input	Receiver Output Enable
3	DE	Digital input	Driver Output Enable
4	D	Digital input	Driver Input
5	GND	Ground	Ground
6	A	Bus input	Noninverting Receiver Input
7	B	Bus input	Inverting Receiver Input
8	V_{CC}	Power	Power Supply

Device Function Tables

Table 2. Truth Table Abbreviations

Abbreviation	Description
H	High level
L	Low level
X	Don’t care
I	Indeterminate
Z	High impedance (off)
NC	Disconnected

Table 3. Driver

Input	Enable	Outputs	
D	**DE**	**A**	**B**
L	H	L	H
H	H	H	L
OPEN	H	L	H
X	OPEN	Z	Z
X	L	Z	Z

(1) H = high level
(2) L = low level
(3) Z = high impedance
(4) X = Don't care
(5) ? = indeterminate

Table 4. Type-2 Receiver

Inputs		Output
V_{ID}= V_A- V_B	**RE**	**R**
V_{ID} ≥ 150 mV	L	H
50 mV < V_{ID} < 150 mV	L	?
V_{ID} ≤ 50 mV	L	L
X	H	Z
X	Open	Z
Open Circuit	L	L

Table 5. Type-2 Receiver Input Threshold Test Voltages

Applied Voltage		Differential Input Voltages	Common Mode Input Voltage	Receiver Output (1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.800	3.650	0.150	3.725	H
3.800	3.750	0.050	3.775	L
–1.250	–1.400	0.150	–1.325	H
–1.350	–1.400	0.050	–1.375	L

(1) H = high level, L = low level, output state assumes receiver is enabled (RE = L).

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
	V_{CC} to GND	−0.5	4	V
	Voltage at Logic pin: D, DE, /RE, R (2)	−0.3	4	V
	Voltage at Bus pin: A, B	−1.8	4	V
	Operating Temeprature Range	−40	85	°C
T_{stg}	Storage Temperature Range	−65	150	°C
T_J	Maximum Junction Temperature		150	°C
	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM,	ANSI/ESDA/JEDEC JS-001	Bus Pin	8	kV
		All Pin Except Bus Pin	4	kV
CDM	ANSI/ESDA/JEDEC JS-002	All Pin	1	kV

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3	3.3	3.6	V
V_{IH}	High-Level Input Voltage	2		VCC	V
V_{IL}	Low-Level Input Voltage	GND		0.8	V
	Voltage at any Bus Terminal V_A,V_B	–1.4		3.8	V
$\lvert V_{ID} \rvert$	Magnitude of Differential Input Voltage	0.05		VCC	V
T_A	Operating Temperature Range	–40		85	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8	130	52	°C/W

(1) θ_{JA} = 130°C/W is typical value of SOP8 provided by package assembly house.

Electrical Characteristics

All test conditions: V_{CC} = 3.0 V ~ 3.6 V, T_A = −40 ~ +85°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply						
V_{CC}	Supply Voltage		3		3.6	V
Icc Supply Current	Driver only	RE and DE at V_{CC}, R_L = 50 Ω, All others open		13	22	mA
	Both Disabled	RE at V_{CC}, DE at 0 V, R_L = No Load, All others open		2	4	mA
	Both Enabled	RE at 0 V, DE at V_{CC}, R_L = 50 Ω, All others open		15	24	mA
	Receiver only	RE at 0 V, DE at 0 V, R_L= 50 Ω, All others open		4	13	mA
I_{Am}	Receiver or Transceiver with Driver Disabled Input Current	V_A = 3.8 V, V_B = 1.2 V,	0		32	μA
		V_A= 0 V or 2.4 V, V_B = 1.2 V	–20		20	μA
		V_A = –1.4 V, V_B = 1.2 V	–32		0	μA
I_B	Receiver or Transceiver with Driver Disabled Input Current	V_B = 3.8 V, V_A = 1.2 V	0		32	μA
		V_B = 0 V or 2.4 V, V_A = 1.2 V	–20		20	μA
		V_B = –1.4 V, V_A = 1.2 V	–32		0	μA
I_{AB}	Receiver or Transceiver with Driver Disabled Differential Input Current (I_A– I_B)	V_A = V_B, 1.4 ≤ V_A ≤ 3.8 V	-4		4	μA
$I_{A\ (OFF)}$	Receiver or Transceiver Power-off Input Current	V_A = 3.8 V, V_B = 1.2 V, 0 V ≤ V_{CC} ≤ 1.5 V	0		32	μA
		V_A = 0 V or 2.4 V, V_B = 1.2 V, 0 V ≤ V_{CC} ≤ 1.5 V	–20		20	μA
		V_A = –1.4 V, V_B = 1.2 V, 0 V ≤ V_{CC} ≤ 1.5 V	–32		0	μA
$I_{B\ (OFF)}$	Receiver or Transceiver Power-off Input Current	V_B = 3.8 V, V_A = 1.2 V, 0 V ≤ V_{CC} ≤ 1.5 V	0		32	μA
		V_B = 0 V or 2.4 V, V_A = 1.2 V, 0 V ≤ V_{CC} ≤ 1.5 V	–20		20	μA
		V_B = –1.4 V, V_A = 1.2 V, 0 V ≤ V_{CC} ≤ 1.5 V	–32		0	μA
$I_{AB(OFF)}$	Receiver Input or Transceiver Power-off Differential Input Current (I_A – I_B)	V_A = V_B, 0 V ≤ V_{CC} ≤ 1.5 V, –1.4 ≤ V_A ≤ 3.8 V	–4		4	μA
Driver Electrical Characteristics						

Parameter		Conditions	Min	Typ	Max	Unit
$\|V_{AB}\|$	Differential Output Voltage Magnitude	See Figure 1	480		650	mV
$\Delta\|V_{AB}\|$	Change in Differential Output Voltage Magnitude between Logic States		–50		50	mV
$V_{OS(SS)}$	Steady-state Common-Mode Output Voltage	See Figure 2	0.8		1.2	V
$\Delta V_{OS(SS)}$	Change in Steady-State Common-Mode Output Voltage Between Logic States		–50		50	mV
$V_{OS(PP)}$	Peak-to-peak Common-Mode Output Voltage				150	mV
$V_{A(OC)}$	Maximum Steady-State Open-Circuit Output Voltage	See Figure 6	0		VCC	V
$V_{B(OC)}$	Maximum Steady-State Open-Circuit Output Voltage		0		VCC	V
$V_{P(H)}$	Voltage Overshoot, Low-to-High-Level Output	See Figure 4			1.2 V_{SS}	V
$V_{P(L)}$	Voltage Overshoot, High-to-Low-Level Output		–0.2 V_{SS}			V
I_{IH}	High-Level Input Current (D, DE)	V_{IH} = 2 V	0		10	μA
I_{IL}	Low-Level Input Current (D, DE)	V_{IL} = 0.8 V	0		10	μA
$\|I_{OS}\|$	Differential Short-Circuit Output Current Magnitude	See Figure 3			75	mA
I_{OZ}	High-Impedance State Output Current (driver only)	–1.4 V ≤ V_A or V_B ≤ 3.8 V, Other output = 1.2 V	–32		32	μA
Driver Switching Characteristics						
t_{PLH}	Propagation Delay Time, Low-To-High-Level Output (1)	See Figure 4		2.8		ns
t_{PHL}	Propagation Delay Time, High-To-Low-Level Output (1)			3.2		ns
t_r	Differential Output Signal Rise Time (1)			1.6		ns
t_f	Differential Output Signal Fall Time (1)			1.8		ns
$t_{sk(p)}$	Pulse Skew ($\|t_{PHL} – t_{PLH}\|$) (1)			433		ps
$t_{jit(per)}$	Period Jitter, rms (1 standard deviation) (1)	100 MHz clock input		1		ps

Parameter		Conditions	Min	Typ	Max	Unit
t_{PHZ}	Disable Time, High-Level-To-High-Impedance Output (1)	See Figure 5		4.5		ns
t_{PLZ}	Disable Time, Low-Level-To-High-Impedance Output (1)			3.2		ns
t_{PZH}	Enable Time, High-Impedance-To-High-Level Output (1)			3.2		ns
t_{PZL}	Enable Time, High-Impedance-To-Low-Level Output (1)			5		ns
Receiver Electrical Characteristics						
V_{IT+}	Positive-Going Differential Input Voltage Threshold	See Figure 8 and Table 1 and Table 2			150	mV
V_{IT-}	Negative-Going Differential Input Voltage Threshold		50			mV
V_{HYS}	Differential Input Voltage Hysteresis, (V_{IT+}– V_{IT}) (1)			0		mV
V_{OH}	High-Level Output Voltage	I_{OH} = –8 mA	2.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 8 mA			0.4	V
I_{IH}	High-Level Input Current (RE)	V_{IH} = 2 V	–10		0	μA
I_{IL}	Low-Level Input Current (RE)	V_{IL} = 0.8 V	–10		0	μA
$C_A$or C_B	Input Capacitance (1)	V_I= 0.4 sin(30E6πt) + 0.5 V, Other input at 1.2 V		7		pF
C_{AB}	Differential Input Capacitance (1)	V_{AB}= 0.4 sin(30E6πt) V		7		pF
$C_{A/B}$	Input Capacitance Balance, (C_A/C_B) (1)		0.99		1.01	
Receiver Switching Characteristics						
t_{pLH}	Propagation Delay Time, Low-to-High-Level Output (1)	C_L = 15 pF, See Figure 9	4	6	8	ns
t_{pHL}	Propagation Delay Time, High-to-Low-Level Output (1)		4	6	8	ns
t_r	Output Signal Rise Time			0.9	2.3	ns
t_f	Output Signal Fall Time			0.8	2.3	ns
$t_{sk(p)}$	Pulse Skew (|t_{phl}– t_{plh}|)			200		ps
$t_{jit(per)}$	Period Jitter, rms (1 standard deviation) (1)	100 MHz clock input		1		ps

Parameter		Conditions	Min	Typ	Max	Unit
t_{pHZ}	Disable Time, High-Level-to-High-Impedance Output (1)	See Figure 10		4.5		ns
t_{pLZ}	Disable Time, Low-Level-to-High-Impedance Output (1)			3.5		ns
t_{pZH}	Enable Time, High-Impedance-to-High-Level Output (1)			7.5		ns
t_{pZL}	Enable Time, High-Impedance-to-Low-Level Output (1)			3.5		ns

(1) Spec data is provided by lab bench test, NOT test in production.

Test Circuits, Configurations and Waveforms

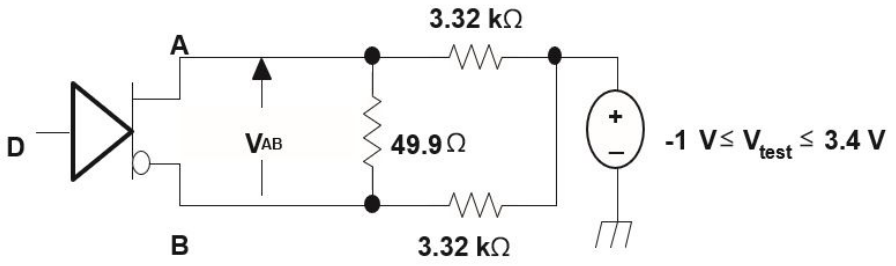


Figure 1. Differential Output Voltage Test Circuit

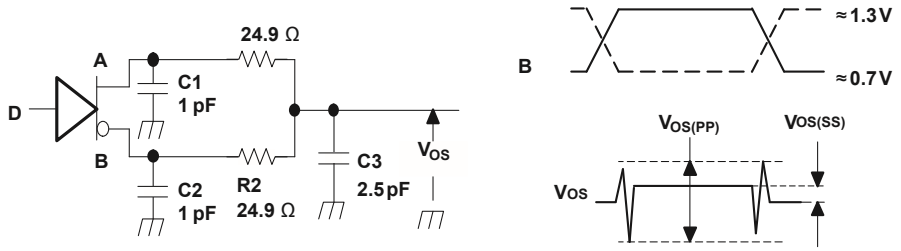


Figure 2. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

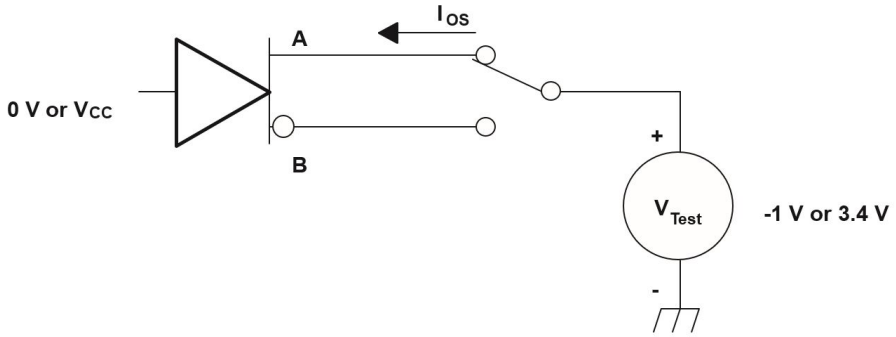


Figure 3. Driver Short-Circuit Test Circuit

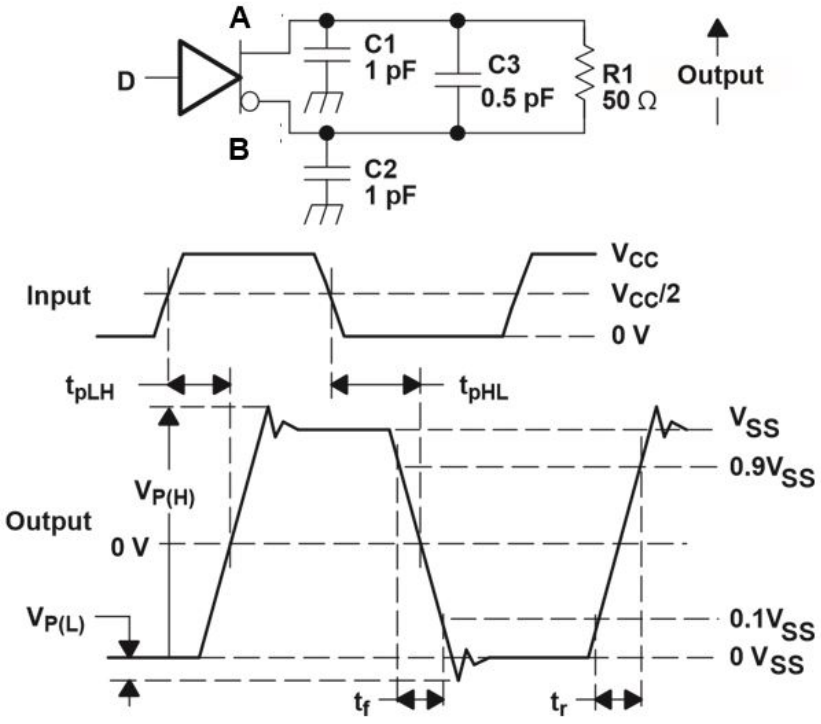


Figure 4. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

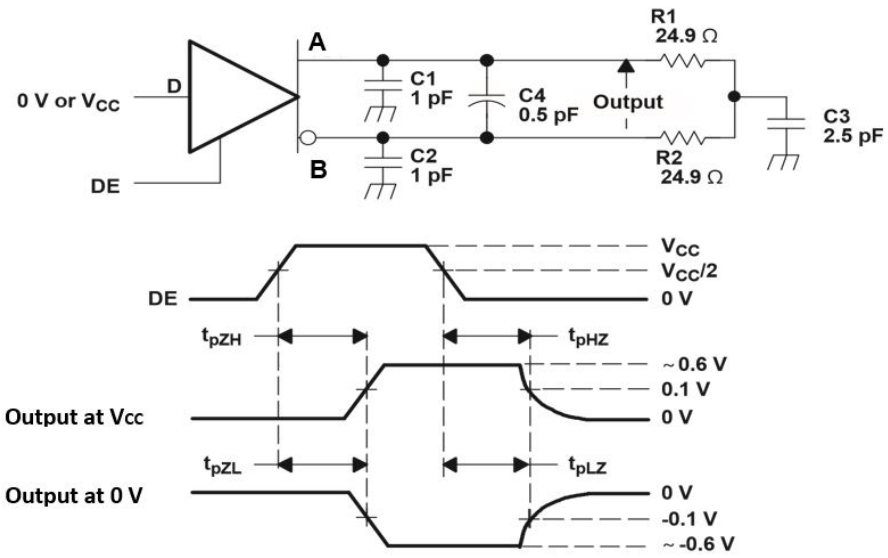


Figure 5. Driver Enable and Disable Time Circuit and Definitions

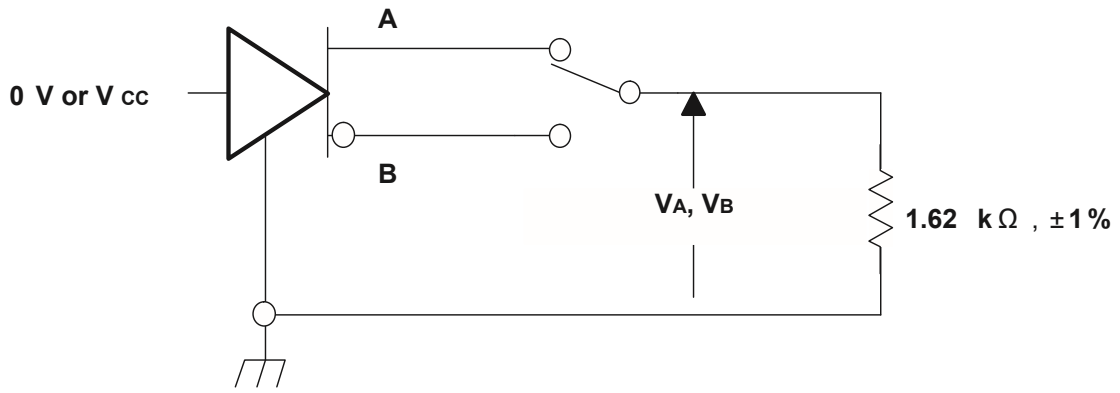


Figure 6. Maximum Steady State Output Voltage

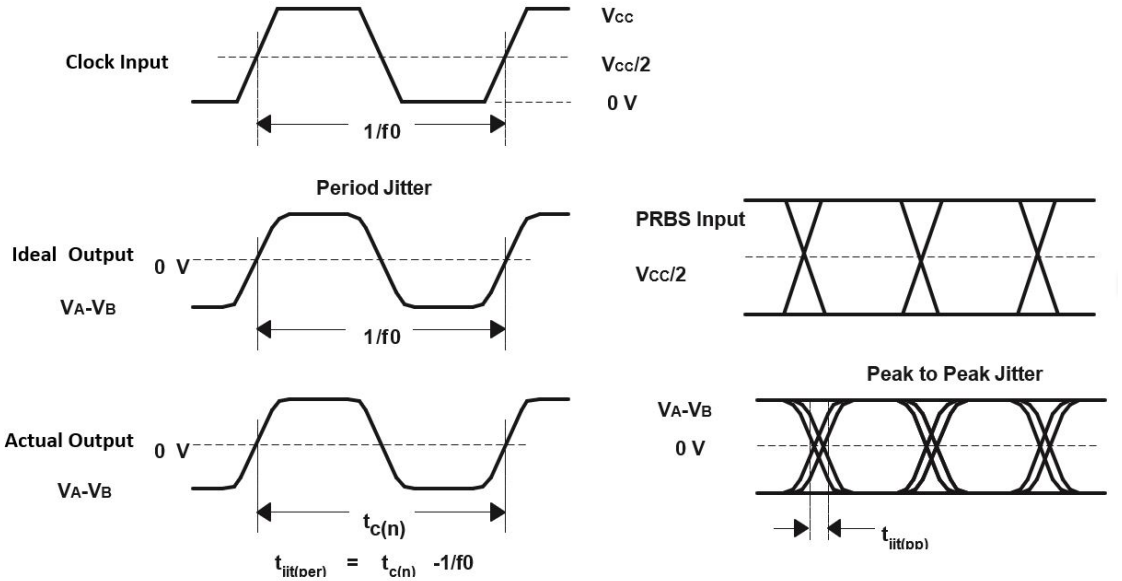


Figure 7. Driver Jitter Measurement Waveforms

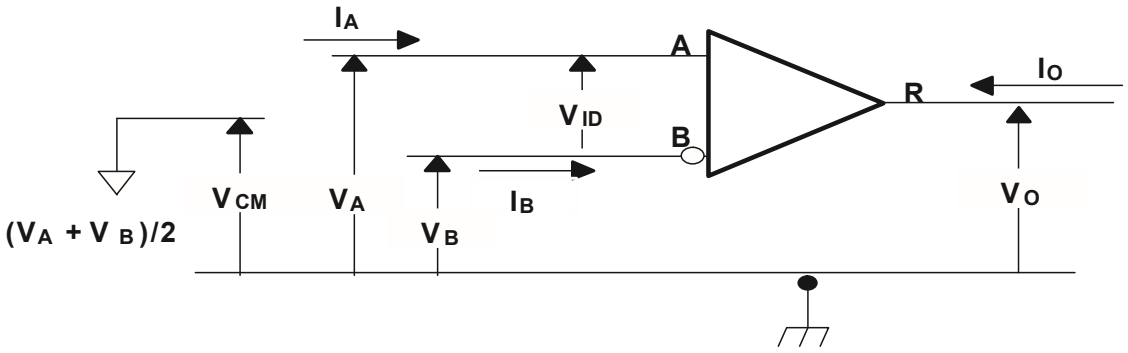


Figure 8. Receiver Voltage and Current Definitions

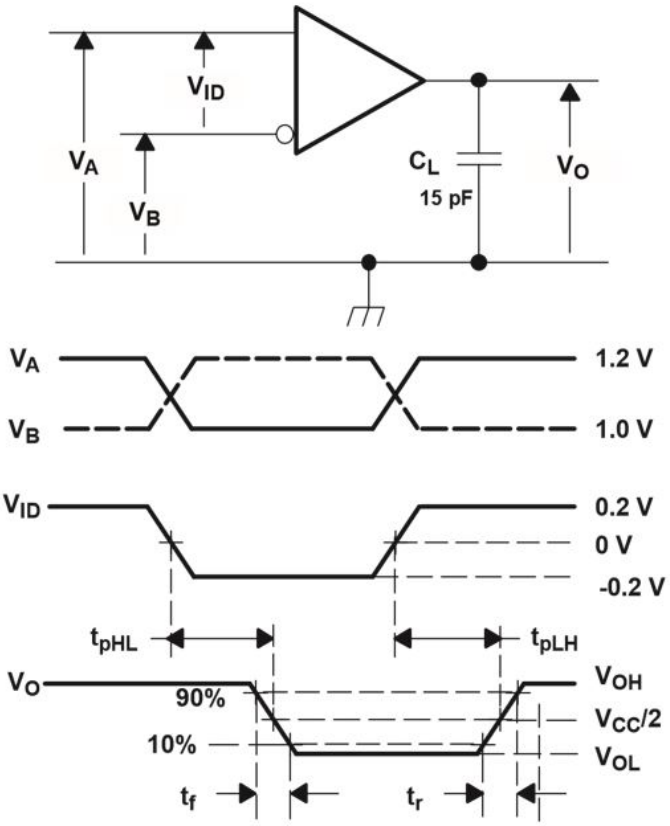


Figure 9. Receiver Timing Test Circuit and Waveforms

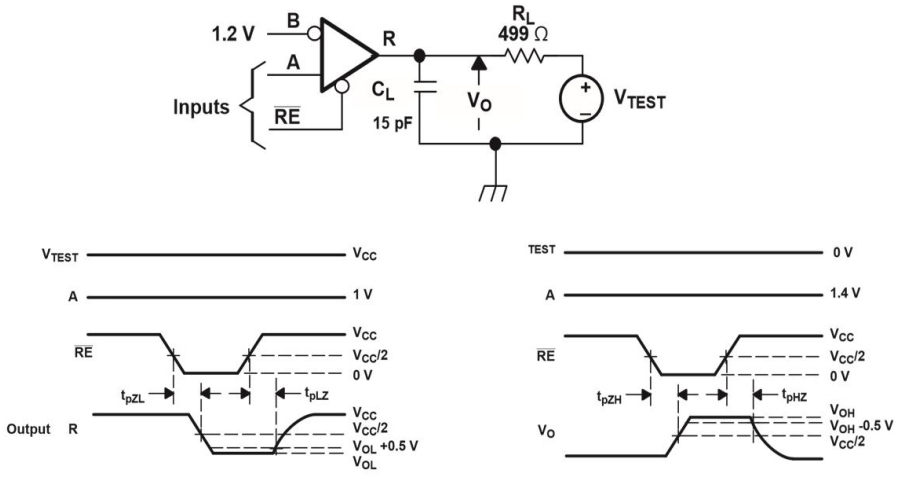


Figure 10. Receiver Timing Test Circuit and Waveforms

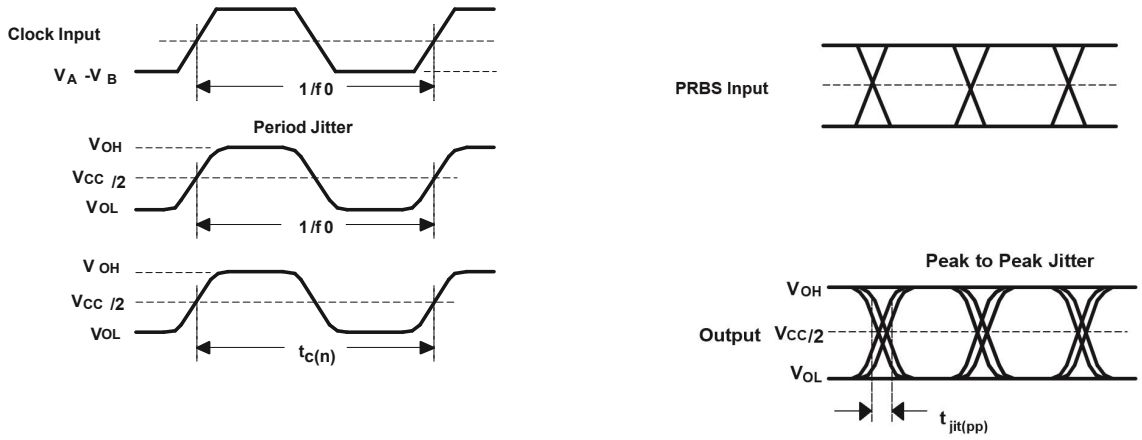


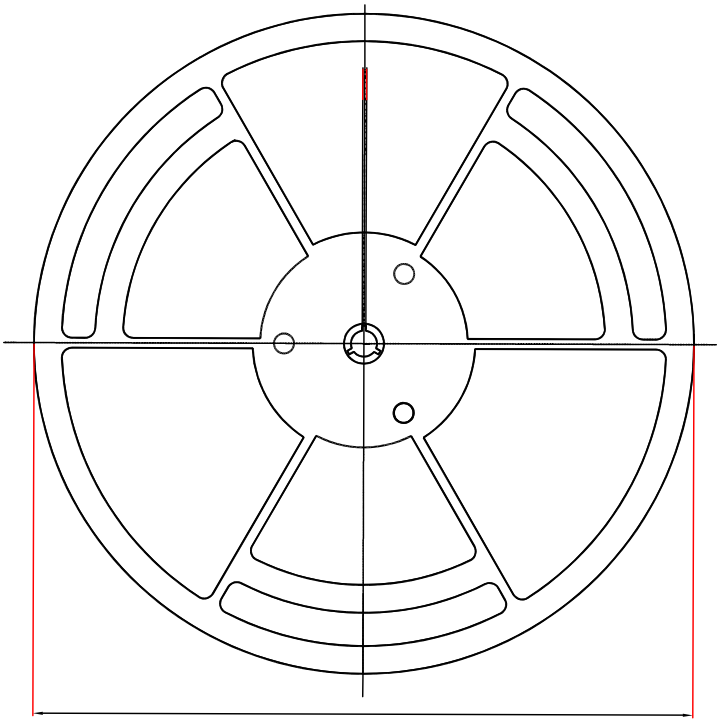
Figure 11. Receiver Jitter Measurement Waveforms

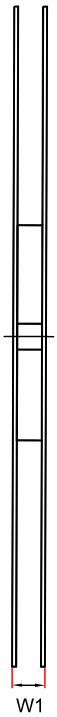
Detailed Description

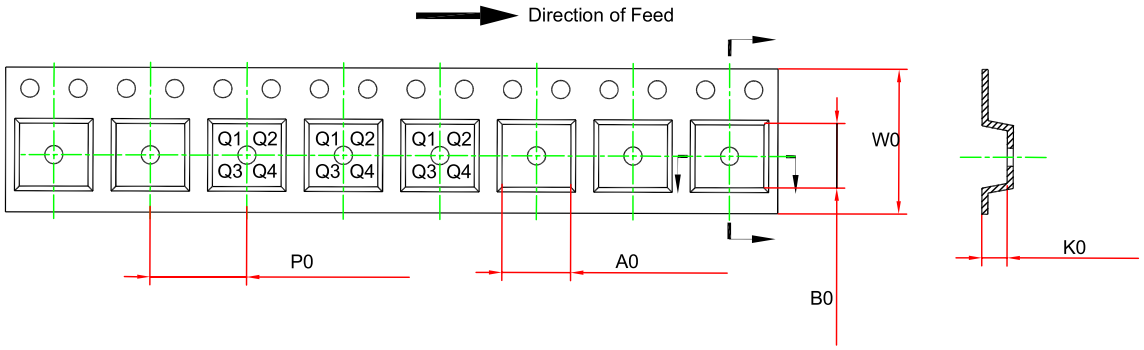
Overview

The TPT9H221A is a 3.3-V Multipoint-Low-Voltage Differential (M-LVDS) line driver and receiver, which can operate at signaling rates up to 200 Mbps. Driver outputs and receiver inputs are protected against ±8-kV ESD strikes without latch-up. The driver output has been designed to support multipoint buses presenting loads as low as 30 Ω, and incorporates controlled transition times to allow for stubs off of the backbone transmission line.

Tape and Reel Information





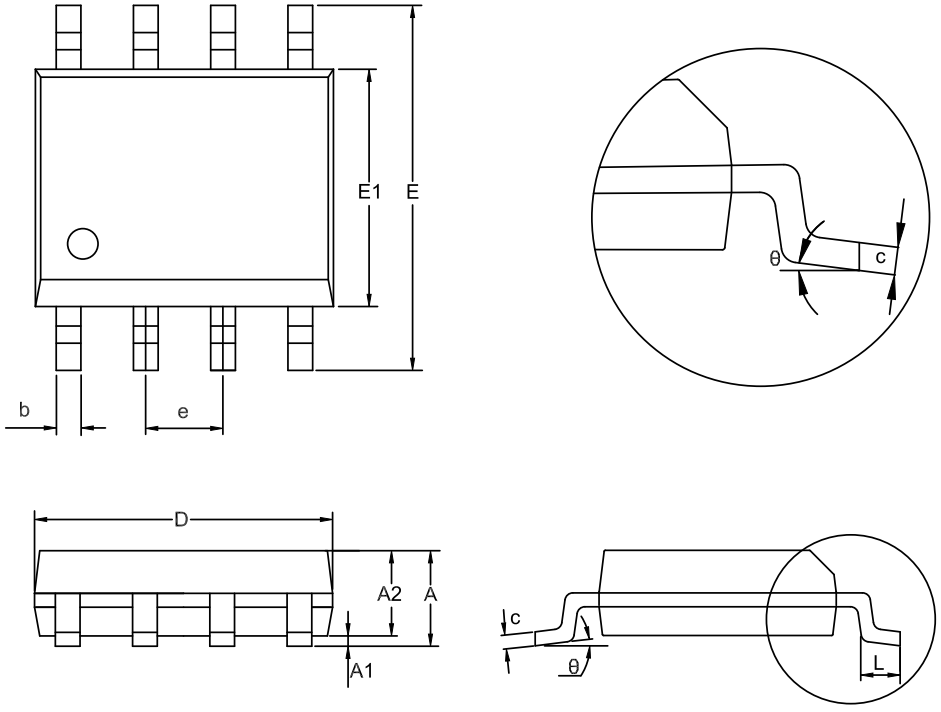


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT9H221A-SO1R-S	SOP8	330.0	17.6	6.5	5.4	2.0	8.0	12.0	Q1

Package Outline Dimensions

SOP8

Package Outline Dimensions SO1(SOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT9H221A-SO1R-S	−40 to 85°C	SOP8	H221A	1	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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