Features

- Exceeds Requirements of EIA-485 Standard
- Data Rate: 20Mbps or 500Kbps
- Up to 256 Nodes on a Bus (1/8 unit load)
- Full Fail-safe Receiver (Open, Short, Terminated)
- Wide Supply Voltage 3V to 5.5V
- 1.65V to Vcc Supply for Digital IOs
- Bus-Pin Protection:
  - ±18 kV HBM ESD
  - ±15 kV IEC61000-4-2 Contact Discharge
  - ±15 kV IEC61000-4-2 Air Discharge

Description

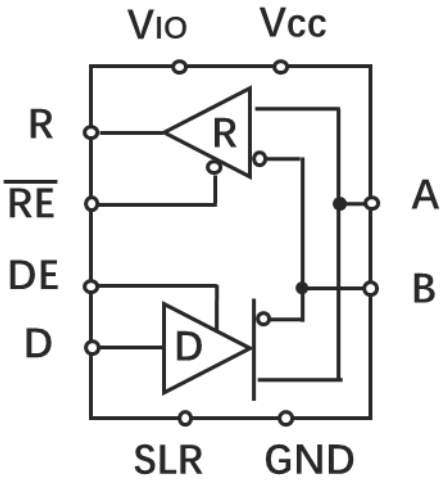
The TPT4181 is a 3.0 V to 5.5 V, IEC electrostatic discharge (ESD) protected RS-485 transceiver, and the device can support ±15 kV Contact Discharge on the transceiver bus pins without damage. The TPT4181 features a VIO logic supply pin allowing a flexible digital interface capable of operating as low as 1.65 V.

Transmitters in this family deliver exceptional differential output voltages into the RS-485 required 54Ω load. Receiver (Rx) inputs feature a “Full Fail-Safe” design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or on a terminated but undriven bus. The TPT4181 is available in an DFN3X3-10L package, and is characterized from –40°C to 125°C.

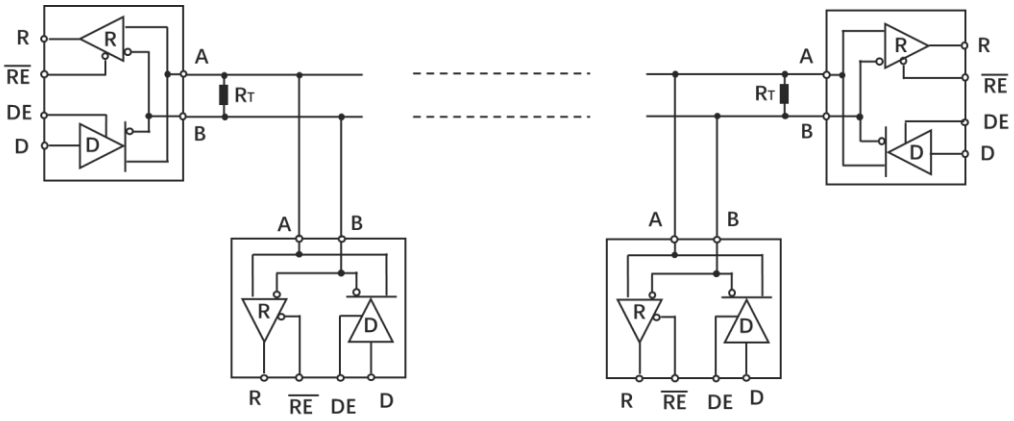
Applications

- Factory Automation
- Field Bus Networks
- Industrial/Process Control Networks
- Communication Infrastructure

Simplified Schematic



Typical RS-485 Network

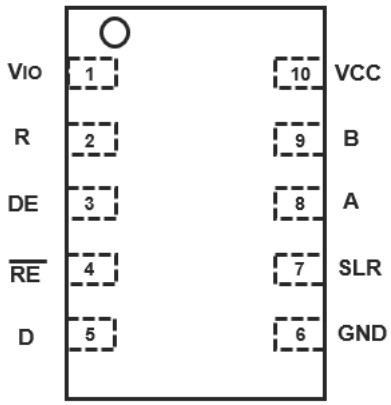


Revision History

Date	Revision	Notes
2018/12/20	Rev. Pre 0	Initial Definition
2019/04/08	Rev. Pre 0.1	Add package information
2019/08/06	Rev. Pre 0.2	Update ESD data
2019/09/03	Rev. Pre 0.3	Update Electrical data
2019/09/27	Rev. Pre 0.4	Update thermal data
2019/09/30	Rev. 0	Final datasheet Rev. 0
2019/12/30	Rev. A	Production update t_{sk} spec
2020/3/24	Rev. B	Update ESD data, absolute rating for A/B bus pin
2020/10/21	Rev. C	Update the package information

Pin Configuration and Functions

TPT4181
DFN3X3-10L



Pin No.	Pin Name	I/O	Description
1	VIO	Logic Supply	1.65 V to Vcc supply for logic I/O signals R, RE, D, DE, and SLR)
2	R	Digital Output	Receive data output
3	DE	Digital Input	Driver enable input
4	/RE	Digital Input	Receiver enable input
5	D	Digital Input	Transmission data input
6	GND	Reference Potential	Local device ground
7	SLR	Digital Input	Slew rate select: Low = 20 Mbps, High = 500 kbps. Default output is 20 Mbps if SLR is floated
8	A	Bus I/O	Digital bus I/O, A
9	B	Bus I/O	Digital bus I/O, B
10	VCC	Bus Supply	3 V to 5.5 V supply for A and B bus lines

Order Information

Model Name	Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TPT4181	TPT4181L1-DF8R	-40 to 125°C	10-Pin DFN3X3	T4181	MSL1	Tape and Reel, 4000

Absolute Maximum Ratings

Parameters	Rating
V_{IO} to GND	-0.3V to +7V
V_{CC} to GND	-0.3V to +7V
Voltage at Logic pin: DI, DE, /RE, RO	-0.3V to V_{CC} + 0.3V
Voltage at Bus pin: A, B	-15V to +15V
Operating Temperature Range	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C

(1) Stresses beyond the *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*.

ESD Rating

		Value	Unit
IEC-61000-4-2, Contact Discharge	Bus Pin	15	kV
IEC-61000-4-2, Air-Gap Discharge	Bus Pin	15	kV
HBM, per ANSI/ESDA/JEDEC JS-001 / ANSI/ESD STM5.5.1	Bus Pin	18	kV
	All Pin Except Bus Pin	4	kV
CDM, per ANSI/ESDA/JEDEC JS-002	All Pin	1	kV

Recommended Operating Conditions

Parameters	Spec
V_{IO}	1.65V to VCC
V_{CC}	3V to 5.5V
Voltage at Logic pin: DI, DE, /RE, RO	= V_{IO}
Voltage at Bus pin: A, B	-7V to +12V
Operating Temperature Range	-40°C to 125°C

Electrical Characteristics

All test condition is V_{CC} = 3.3V~5.0V, T_A = -40 ~ +125°C

Symbol	PARAMETER	TEST CONDITIONS		Min		MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	RL = 60 Ω, 375 Ω on A/B: –7 V to 12V, VCC=3.3V		1.5	1.9		V
		RL = 60 Ω, 375 Ω on A/B: –7 V to 12V, VCC=5V		2.0	3.0		V
		R_L = 54 Ω , VCC=3.3V		1.5	2.0		V
		R_L = 54 Ω , VCC=5.0V		2.0	3.0		
		R_L = 100 Ω, V_{CC} = 3.3V		1.5	2.3		
		R_L = 100 Ω, V_{CC} = 5.0V		2.0	3.5		V
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF， 375 Ω on A/B: –7 V to 12V, VCC=3.3V		–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors		1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage [1]				500		mV
C_{OD}	Differential output capacitance [1]				15		pF
V_{IT+}	Positive-going receiver differential input voltage threshold				-100	–20	mV
$V_{IT–}$	Negative-going receiver differential input voltage threshold			–220	–150		mV
V_{HYS}	Receiver differential input voltage threshold hysteresis (V_{IT+} – $V_{IT–}$) [1]				50		mV
V_{OH}	Receiver high-level output voltage	V_L = 1.65 V, I_{OH} = -2 mA		1.3	1.5		V
		V_L = 3 V, I_{OH} = -2 mA		2.8	2.9		
V_{OL}	Receiver low-level output voltage	V_L = 1.65 V, I_{OL} = 2 mA			0.13	0.35	V
		V_L = 3 V, I_{OL} = 2 mA			0.07	0.2	
V_{IH}	Input High Logic Leve	D, DE, /RE		2/3 VL			V
V_{IL}	Input Low Logic Leve	D, DE, /RE				1/3 VL	V
I_{IN}	Driver input, driver enable, and receiver enable input current	D, DE, /RE		–5		5	μA
I_{OZ}	Receiver output high-Z current	V_O = 0 V or V_L, RE at V_L		–1		1	μA
I_{OS}	Driver short-circuit output current	V_A V_B = -7V ~ 12V		–250		250	mA
		A, B short		-120		120	mA
$I_{IA/B}$	Bus input current (disabled driver)	V_L = 1.8 V, DE at 0 V	V_I = 12 V,		100	150	μA
		V_{CC} = 5.0 V, or V_{CC} = 0 V	V_I = –7 V,	-100	-50		μA
I_{CC}	Supply current (quiescent), 20Mbps	Driver and Receiver enabled	DE=V_L, RE = GND, No load			2200	μA
		Driver enabled, receiver disabled	DE=V_{CC}, RE = V_L, No load		350	560	μA
		Driver disabled, receiver enabled	DE=GND, RE = GND, No load		1000	2000	μA
		Driver and receiver disabled	DE=GND, RE = V_L, No load	-2		2	μA

I_{CC}	Supply current (quiescent), 500Kbps	Driver and Receiver enabled	DE=V_L, RE = GND, No load		850	μA
		Driver enabled, receiver disabled	DE=V_{CC}, RE = V_L, No load	400	600	μA
		Driver disabled, receiver enabled	DE=GND, RE = GND, No load	400	600	μA
		Driver and receiver disabled	DE=GND, RE = V_L, No load	-2	2	μA

Note:

[1]. Parameters are provided by lab bench test and design simulation

Switching Characteristics, Vcc=VL=3.0V (Test in 20Mbps mode)

Parameter		Conditions		Min	Typ	Max	Units
Driver							
t_r, t_f	Driver differential-output rise and fall times [1]	RL = 54 Ω, CL=50pF	See Figure 2		10		ns
t_{PHL}, t_{PLH}	Driver propagation delay				22	40	
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				3	10	
t_{PHZ}, t_{PLZ}	Driver disable time	Receiver enabled	See Figure 3		26	50	ns
		Receiver disabled			26	50	
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			26	50	ns
		Receiver disabled			2400	3500	
Receiver							
t_{PHL}, t_{PLH}	Receiver propagation delay time				40	80	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				7	15	
t_{PHZ}, t_{PLZ}	Receiver disable time	Driver enabled	See Figure 6		25	50	ns
		Driver disabled			25	50	
t_{PZH}, t_{PZL}	Receiver enable time	Driver enabled			80	125	ns
		Driver disabled			2500	3500	

Note:

[1]. Parameters are provided by lab bench test and design simulation

Switching Characteristics, Vcc=VL=3.0V (Test in 500Kbps mode)

Parameter		Conditions		Min	Typ	Max	Units
Driver							
t_r, t_f	Driver differential-output rise and fall times [1]	RL = 54 Ω, CL=50pF	See Figure 2		400		ns
t_{PHL}, t_{PLH}	Driver propagation delay				280	400	
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				5	20	
t_{PHZ}, t_{PLZ}	Driver disable time	Receiver enabled	See Figure 3		48	90	ns
		Receiver disabled			48	90	
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			300	500	ns
		Receiver disabled			2700	3500	
Receiver							
t_{PHL}, t_{PLH}	Receiver propagation delay time				110	200	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				15	28	
t_{PHZ}, t_{PLZ}	Receiver disable time	Driver enabled	See Figure 6		28	50	ns
		Driver disabled			28	50	
t_{PZL}, t_{PZH}	Receiver enable time	Driver enabled			135	180	ns
		Driver disabled			2600	3500	

Note:

[1]. Parameters are provided by lab bench test and design simulation

Test Circuits and Waveforms

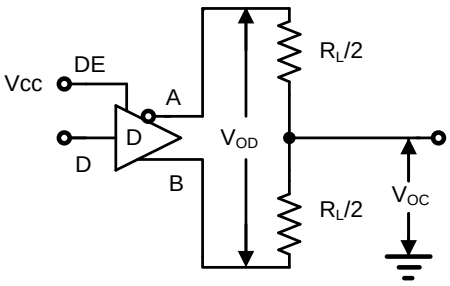


Figure 1A. VOD and VOC

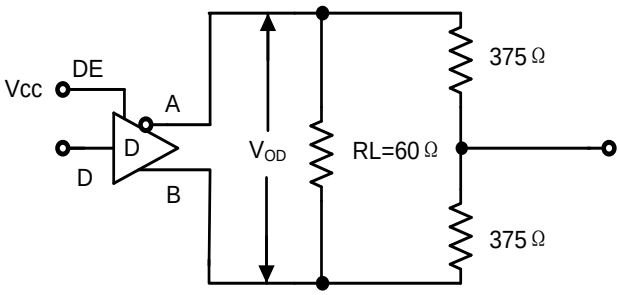


Figure 1B. VOD with Common Mode Load

Figure 1. DC Driver Test Circuits

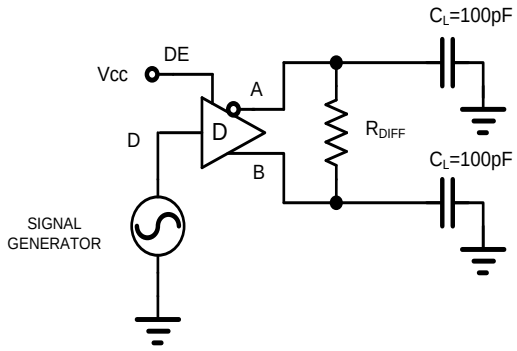


Figure 2A. Test Circuit

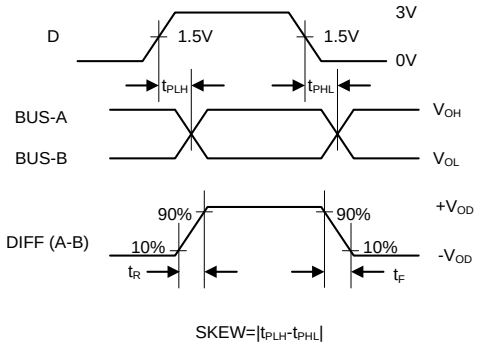
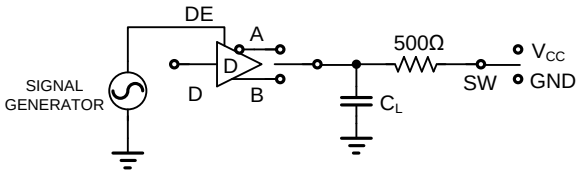


Figure 2B. Measurement Points

Figure 2. Driver Propagation Delay and Differential Transition Times



PARAMETER	OUTPUT	RE	DI	SW	CL (pF)
tPHZ	A/B	X	1/0	GND	15
tPLZ	A/B	X	0/1	VCC	15
tPZH	A/B	0	1/0	GND	100
tPZL	A/B	0	0/1	VCC	100
tPZH(SHDN)	A/B	1	1/0	GND	100
tPZL(SHDN)	A/B	1	0/1	VCC	100

Figure 3A. Test Circuit

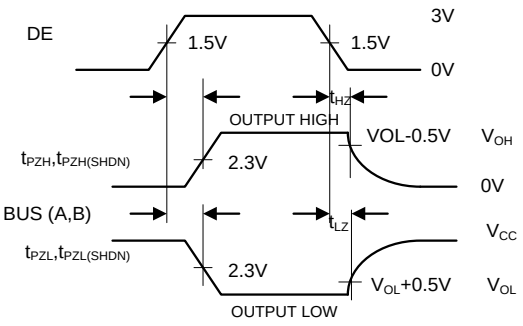


Figure 3B. Measurement Points

Figure 3. Driver Enable and Disable Times

Test Circuits and Waveforms (continue)

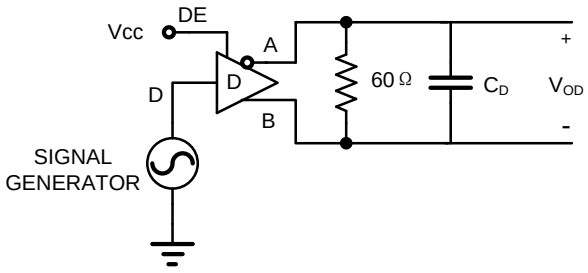


Figure 4A. Test Circuit

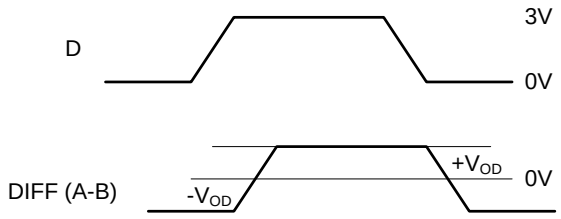


Figure 4B. Measurement Points

Figure 4. Driver Data rate

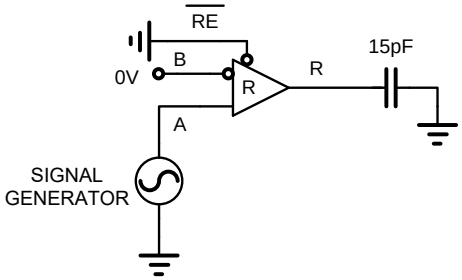


Figure 5A. Test Circuit

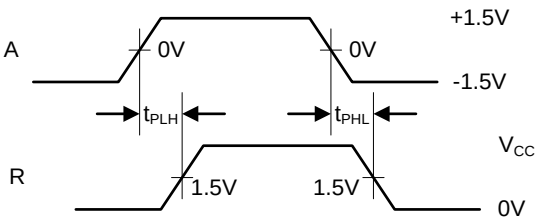
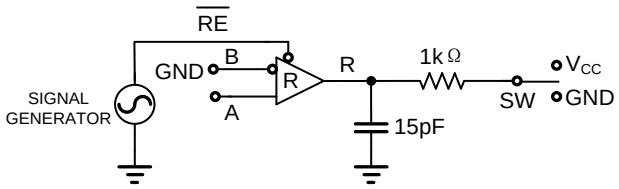


Figure 5B. Measurement Points

Figure 5. Receiver Propagation Delay and Data rate



PARAMETER	DE	A	SW
tPHZ	1	+1.5V	GND
tPLZ	1	-1.5V	VCC
tPZH	1	+1.5V	GND
tPZL	1	-1.5V	VCC
tPZH(SHDN)	0	+1.5V	GND
tPZL(SHDN)	0	-1.5V	VCC

Figure 6A. Test Circuit

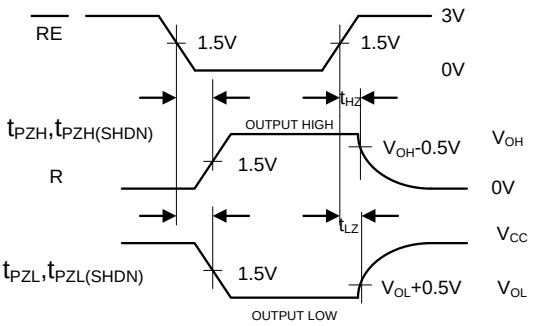
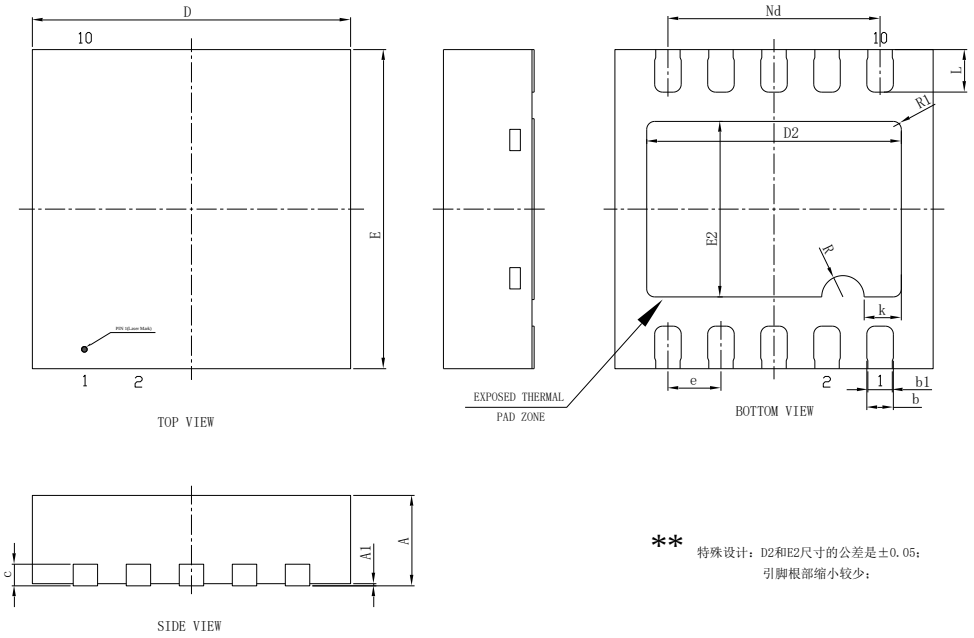


Figure 6B. Measurement Points

Figure 6. Receiver Enable and Disable Times

Package Outline Dimensions

DF8R (DFN3X3-10L)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.23REF	
c		0.203REF	
D	2.90	3.00	3.10
D2	2.35	2.40	2.45
e		0.50BSC	
Nd		2.00BSC	
E	2.90	3.00	3.10
E2	1.60	1.65	1.70
L	0.35	0.40	0.45
R		0.20REF	
R1		0.075REF	
k		0.35REF	

** 特殊设计：D2和E2尺寸的公差是±0.05；
引脚根部缩小较少；

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