3.3V~5.0V Full Duplex RS-485 Transceivers with polarity control

Features

- Exceeds Requirements of EIA-485 Standard
- Hot Plug Circuitry - Tx and Rx Outputs Remain Three-State During Power-up/Power-down
- Supply voltage: 3.0V ~ 5.5V
- Data Rate: 32Mbps or 500Kbps
- Up to 256 Nodes on a Bus (1/8 unit load)
- Full Fail-safe Receiver (Open, Short, Terminated)
- H/F control to support Half and Full Duplex RS485
- Polarity Control to Correct for Bus Reversal through RXP/TXP Pins
- Bus-Pin Protection:
  - ±12 kV IEC61000-4-2 Contact Discharge
  - ±15 kV IEC61000-4-2 Air Discharge
  - ±2 kV IEC61000-4-4 Fast Transient Burst
- –40°C to 125°C Operation Temperature Range

Description

The TPT4089 is IEC61000 ESD protected, 5V transceivers that meet the RS-485 and RS-422 standards for Half and Full Duplex communication.

The TPT4089 features a fail-safe receiver, which support the output of the receiver to be logic high when the differential input (bus pin A/B) of the receiver is open, short or idle when RXP=0V.

Transmitters in this family deliver exceptional differential output voltages into the RS-485 required 54Ω load. The 10Mbps devices have very low bus currents so they present a true “1/8 unit load” to the RS-485 bus. This allows up to 256 transceivers on the network without using repeaters. Receiver (Rx) inputs feature a “Full Fail-Safe” design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or on a terminated but undriven bus. The TPT48x is characterized from –40°C to 125°C.

Applications

- Home Appliance
- Motor Drives
- Industrial Control
- Communication Infrastructure

Device Table

Part	Duplex	Enable	Data Rate	Package
TPT4089	Half or Full	Yes	32Mbps or 500Kbps	SOP14

Simplified Schematic

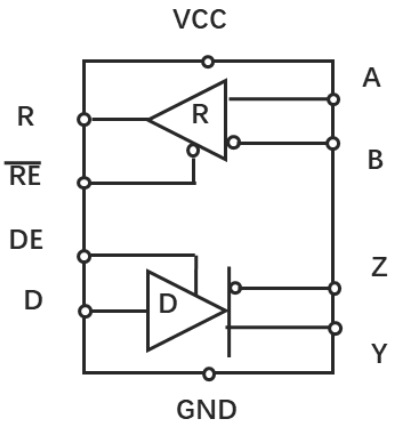


Table of Contents

Revision History

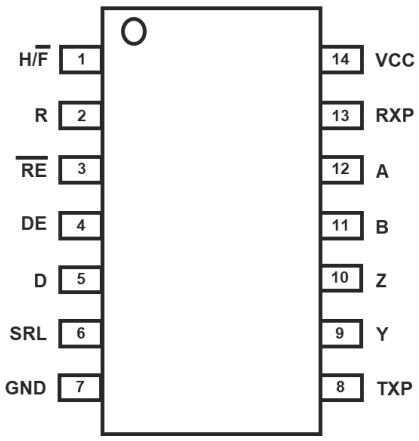
Date	Revision	Notes
2020/12/18	Rev. Pre.0	Definition Version Pre.0
2022/4/22	Rev. A0	Released version

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TPT4089-SO2R	-40 to 125°C	SOP14	T4089	3	Tape and Reel, 2,500

Pin Configuration and Functions

TPT4089
SOP14



Pin No.	Pin Name	I/O	Description
1	H/F	Digital input	Half-/Full-Duplex Select Input. Connect H/F to VCC for half-duplex mode; connect H/F to GND or leave unconnected for full-duplex mode
2	R	Digital output	Receiver Output
3	/RE	Digital input	Receiver Output Enable
4	DE	Digital input	Driver Output Enable
5	D	Digital input	Driver Input
6	SRL	Digital input	Slew-Rate Limit Selector Input. Connect SRL to ground for 32Mpbs data rate; connect SRL to VCC or Leave SRL unconnected for 500kbps data rate
7	GND	Ground	Ground
8	TXP	Digital input	Transmitter Phase. Connect TXP to ground or leave TXP unconnected for normal transmitter phase/polarity. Connect TXP to VCC to invert the transmitter phase/polarity
9	Y	Bus output	Noninverting Driver Output
10	Z	Bus output	Inverting Driver Output
11	B	Bus input	Inverting Receiver Input
12	A	Bus input	Noninverting Receiver Input
13	RXP	Digital input	Receiver Phase. Connect RXP to GND or leave RXP unconnected for normal transmitter phase/polarity. Connect RXP to VCC to invert receiver phase/polarity
14	VCC	Power	Power Supply

Functional Table

Functional Table of TPT4089

Driver Function Table

Input	Enable	Output	Output	Description
D	DE	A	B	
H	H	H	L	Actively drives bus High
L	H	L	H	Actively drives bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
Open	H	H	L	Actively drives bus High by default

X = don't care

Z = high impedance

Receiver Function Table

Input	Input	Output	Description
A-B	/RE	R	
>-50mV	L	H	Receive valid bus High
-200mV<Input<-50mV	L	?	Indeterminate bus state
<-200mV	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled in default
Open	L	H	Fail-safe high output
Short	L	H	Fail-safe high output
Idle (Terminated)	L	H	Fail-safe high output

X = don't care

Z = high impedance

Absolute Maximum Ratings

Parameters	Rating
VCC to GND	-0.3V to +7V
Voltage at Logic pin: D, DE, /RE, R	-0.3V to VCC + 0.3V
Voltage at Bus pin: A, B, Y, Z (1)	-15V to +15V
Operating Temperature Range	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C

(1) Support ±15V in receiver mode, and -8 ~+13V in driver mode

(2) Stresses beyond the *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*.

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	3.0		5.5	V
V_I	Input voltage at any bus terminal(1)	-7		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)	2		VCC	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V
V_{ID}	Differential input voltage	-7		12	V
R_L	Differential load resistance	54			Ω
T_A	Operating ambient temperature	-40		125	°C
T_J	Junction temperature	-40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ESD Rating

		Value	Unit
IEC-61000-4-2, Contact Discharge	Bus Pin	±12	kV
IEC-61000-4-2, Air-Gap Discharge	Bus Pin	±15	kV
HBM, per ANSI/ESDA/JEDEC JS-001 / ANSI/ESD STM5.5.1	Bus Pin	±18	kV
	All Pin Except Bus Pin	±4	kV
CDM, per ANSI/ESDA/JEDEC JS-002	All Pin	±1.5	kV

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
14-Pin SOIC	120	36	°C/W

Electrical Characteristics

All test condition is VCC = 3.3V~5.0V, T_A = -40 ~ +125°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		Min		MAX	Unit
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 54 Ω , VCC=3.3V		1.5	2.2		V
		R_L = 54 Ω , VCC=5.0V		2.0	3.3		V
		R_L = 100 Ω, VCC = 3.3V		1.5	2.6		V
		R_L = 100 Ω, VCC = 5.0V		3.0	3.9		V
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage			–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors		1	VCC/2	2	V
ΔV_{OC}	Change in differential driver output common-mode voltage			–200		200	mV
C_{OD}	Differential output capacitance [1]				15		pF
V_{IT+}	Positive-going receiver differential input voltage threshold				-110	–50	mV
V_{IT-}	Negative-going receiver differential input voltage threshold			–200	–130		mV
V_{HYS}	Receiver differential input voltage threshold hysteresis ($V_{IT+} - V_{IT-}$) [1]				50		mV
V_{OH}	Receiver high-level output voltage	VCC = 3.3 V, I_{OH} = -8 mA		2.6	3.0		V
		VCC = 5 V, I_{OH} = -8 mA		4.1	4.8		
V_{OL}	Receiver low-level output voltage	VCC = 3.3 V, I_{OH} = -8 mA			0.19	0.4	V
		VCC = 5 V, I_{OH} = -8 mA			0.02	0.4	
V_{IH}	Input High Logic Leve	D, DE, /RE, TXP, RXP, SRL, H/F		2.0			V
V_{IL}	Input Low Logic Leve	D, DE, /RE, TXP, RXP, SRL, H/F				0.8	V
I_{IN}	Driver input, driver enable, and receiver enable input current	D, DE, /RE		–5		5	μA
I_{IN}	Driver input, driver enable, and receiver enable input current	TXP, RXP, H/F		–1		40	μA
I_{IN}	Driver input, driver enable, and receiver enable input current	SRL		–15		15	μA
I_{OZ}	Driver output high-Z current	V_O = -7V		–100		0	μA
		V_O = 12V		0		125	
I_{OZ}	Receiver high-Z current	V_O = 0 V or VCC		–1		1	μA
I_{OS}	Driver short-circuit output current	VY, VZ= -7V ~ 12V		–250		250	mA
		R=0V or VCC		-180		180	mA
$I_{IA/B}$	Bus input current (disabled driver)	DE = 0 V, RE=VCC	V_I = 12 V,		55	125	μA
			V_I = –7 V,	-100	-50		μA
I_{CC}	Supply current (quiescent), 32Mpbs	Driver and Receiver enabled	DE=VCC, RE = GND, No load		1200	2500	μA
		Driver enabled, receiver disabled	DE=VCC, RE = VCC, No load		1200	2500	μA
		Driver disabled, receiver enabled	DE=GND, RE = GND, No load		1000	2200	μA
		Driver and receiver disabled	DE=GND, RE = VCC, No load	-5		5	μA

I_{CC}	Supply current (quiescent), 500Kbps	Driver and Receiver enabled	DE=VCC, RE = GND, No load		1000	μA
		Driver enabled, receiver disabled	DE=VCC, RE = VCC, No load	400	1000	μA
		Driver disabled, receiver enabled	DE=GND, RE = GND, No load	400	1000	μA
		Driver and receiver disabled	DE=GND, RE = VCC, No load	-5	5	μA

Note:

[1]. Parameters are provided by lab bench test and design simulation

Switching Characteristics, VCC= 5.0V — TPT4089 in 32Mbps

Parameter		Conditions		Min	Typ	Max	Units
Driver							
t_r, t_f	Driver differential-output rise and fall times [1]	RL = 54 Ω, CL=50pF	See Figure 2		5		ns
t_{PHL}, t_{PLH}	Driver propagation delay				19	30	
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$ [1]				1		
t_{PHZ}, t_{PLZ}	Driver disable time	/RE=0 or VCC	See Figure 3		37	50	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			21	40	ns
		Receiver disabled			1760	2500	
Receiver							
t_r, t_f	Driver differential-output rise and fall times [1]				4		ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				36	45	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				4		
t_{PHZ}, t_{PLZ}	Receiver disable time	DE=0 or VCC	See Figure 6		15	25	ns
t_{PZH}, t_{PZL}	Receiver enable time	Driver enabled			14	25	ns
		Driver disabled			1750	2500	

Note:

[1]. Parameters are provided by lab bench test and design simulation

Switching Characteristics, VCC=3.3V — TPT4089 in 32Mpbs

Parameter		Conditions		Min	Typ	Max	Units
Driver							
t_r, t_f	Driver differential-output rise and fall times [1]	RL = 54 Ω, CL=50pF	See Figure 2		6		ns
t_{PHL}, t_{PLH}	Driver propagation delay				22	30	

Parameter		Conditions		Min	Typ	Max	Units
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				1		
t_{PHZ}, t_{PLZ}	Driver disable time	/RE=0 or VCC	See Figure 3		40	55	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			30	50	ns
		Receiver disabled			2560	4000	
Receiver							
t_r, t_f	Driver differential-output rise and fall times [1]				4		ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				47	60	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				6		
t_{PHZ}, t_{PLZ}	Receiver disable time	DE=0 or VCC	See Figure 6		21	30	ns
t_{PZH}, t_{PZL}	Receiver enable time	Driver enabled			17	30	ns
		Driver disabled			2550	4000	

Note:

[1]. Parameters are provided by lab bench test and design simulation

Switching Characteristics, VCC= 5.0V — TPT4089 in 500Kbps

Parameter		Conditions		Min	Typ	Max	Units
Driver							
t_r, t_f	Driver differential-output rise and fall times [1]	RL = 54 Ω, CL=50pF	See Figure 2		470		ns
t_{PHL}, t_{PLH}	Driver propagation delay				450	600	
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				6		
t_{PHZ}, t_{PLZ}	Driver disable time	/RE=0 or VCC	See Figure 3		61	100	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			216	500	ns
		Receiver disabled			1960	4000	
Receiver							
t_r, t_f	Driver differential-output rise and fall times [1]				15		ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				100	150	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				5		
t_{PHZ}, t_{PLZ}	Receiver disable time	DE=0 or VCC	See Figure 6		20	50	ns
t_{PZL}, t_{PZH}	Receiver enable time	Driver enabled			25	50	ns
		Driver disabled			1760	4000	

Note:

[1]. Parameters are provided by lab bench test and design simulation

Switching Characteristics, VCC=3.3V — TPT4089 in 500Kbps

Parameter		Conditions		Min	Typ	Max	Units
Driver							
t_r, t_f	Driver differential-output rise and fall times [1]	RL = 54 Ω, CL=50pF	See Figure 2		460		ns
t_{PHL}, t_{PLH}	Driver propagation delay				460	700	
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				4		
t_{PHZ}, t_{PLZ}	Driver disable time	/RE=0 or VCC	See Figure 3		67	200	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			350	1000	ns
		Receiver disabled			2870	4000	
Receiver							
t_r, t_f	Driver differential-output rise and fall times [1]				20		ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				115	200	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				8		
t_{PHZ}, t_{PLZ}	Receiver disable time	DE=0 or VCC	See Figure 6		21	40	ns
t_{PZL}, t_{PZH}	Receiver enable time	Driver enabled			33	50	ns
		Driver disabled			2560	4000	

Note:

[1]. Parameters are provided by lab bench test and design simulation

Test Circuits and Waveforms

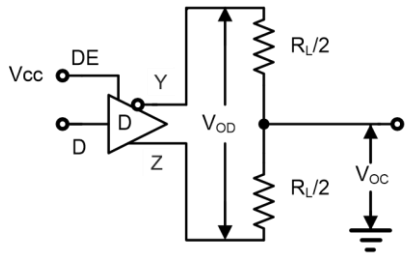


Figure 1A. VOD and VOC

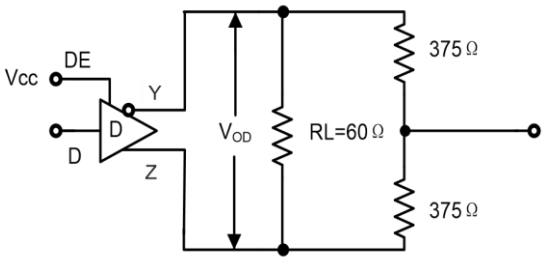


Figure 1B. VOD with Common Mode Load

Figure 1. DC Driver Test Circuits

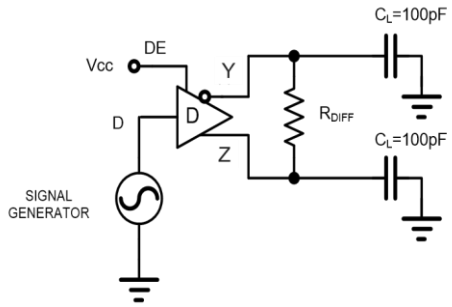


Figure 2A. Test Circuit

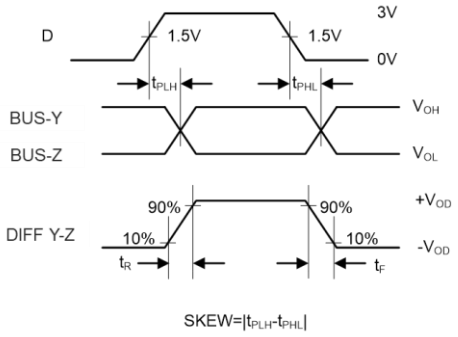


Figure 2B. Measurement Points

Figure 2. Driver Propagation Delay and Differential Transition Times

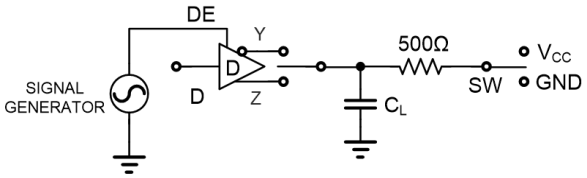


Figure 3A. Test Circuit

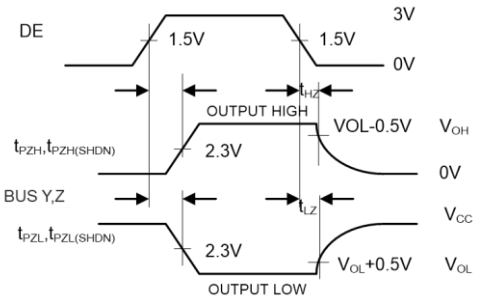


Figure 3B. Measurement Points

PARAMETER	OUTPUT	RE	DI	SW	CL (pF)
tPHZ	Y/Z	X	1/0	GND	15
tPLZ	Y/Z	X	0/1	VCC	15
tPZH	Y/Z	0	1/0	GND	100
tPZL	Y/Z	0	0/1	VCC	100
tPZH(SHDN)	Y/Z	1	1/0	GND	100
tPZL(SHDN)	Y/Z	1	0/1	VCC	100

Figure 3. Driver Enable and Disable Times

Test Circuits and Waveforms (continue)

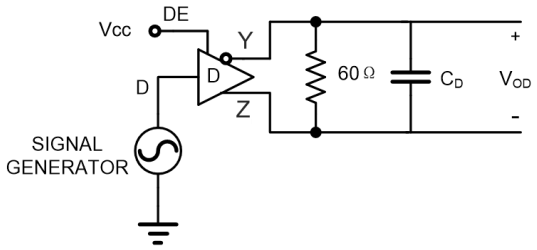


Figure 4A. Test Circuit

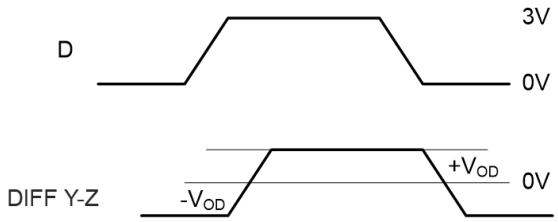


Figure 4B. Measurement Points

Figure 4. Driver Data rate

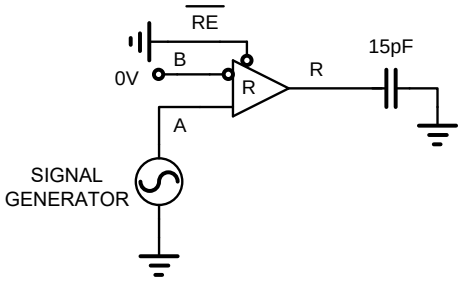


Figure 5A. Test Circuit

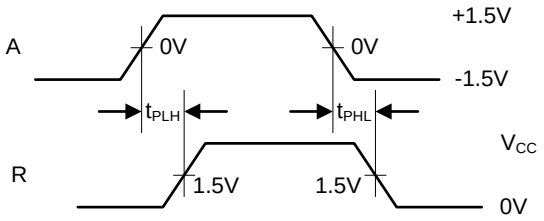
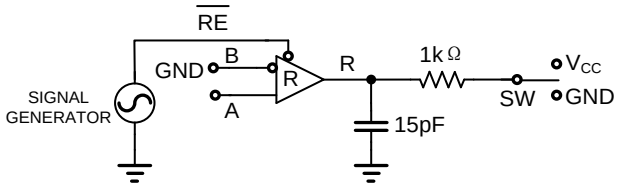


Figure 5B. Measurement Points

Figure 5. Receiver Propagation Delay and Data rate



PARAMETER	DE	A	SW
tPHZ	1	+1.5V	GND
tPLZ	1	-1.5V	VCC
tPZH	1	+1.5V	GND
tPZL	1	-1.5V	VCC
tPZH(SHDN)	0	+1.5V	GND
tPZL(SHDN)	0	-1.5V	VCC

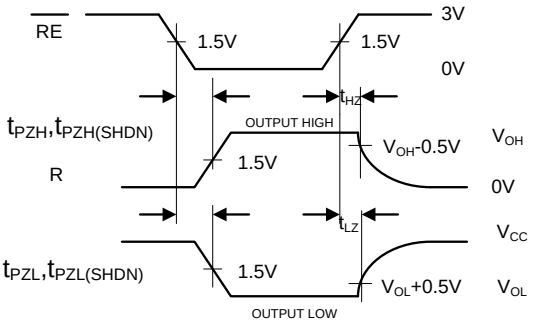
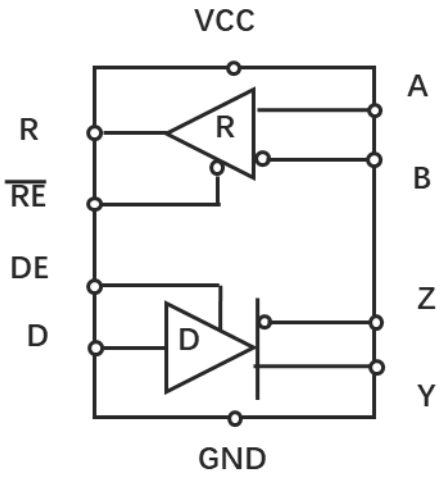


Figure 6A. Test Circuit

Figure 6B. Measurement Points

Figure 6. Receiver Enable and Disable Times

Function Block diagram:



Theory of Operation

General description

The TPT4089 is a RS-485/RS-422 transceivers with robust HBM and IEC 61000 ESD protection. The device build in fail-safe circuit, when the receiver input is open or shorted, or idle mode, it will generate a logic-high receiver output. The TPT4089 supports hot-swap function allowing line insertion to avoid wrong data transmission, and optimizes the drivers slew-rate to minimize EMI and reduce reflections caused by different terminated cables, then support the error-free data communication at 500Kbps data rate. As the driver slew rates is not limited, so the TPT4089 can support the high communication speed up to 32Mbps. Use the SRL pin (Slew-Rate Limit) to config the device in different data rate communication, connecting SRL to ground for 32Mpbs data rate; Connecting SRL to VCC or Leave SRL unconnected for 500kbps data rate.

The TPT4089 use a selector pin (H/F) high or low to select the status between half- and full-duplex communication.

The TPT4089 operates from a single +3.3V to 5.0V power supply, the driver is designed with output short-circuit current limitation, together with thermal-shutdown circuitry to protect drivers in the status of excessive power dissipation. In active mode, the thermal-shutdown circuitry places the driver outputs into a high-impedance state.

In the typical RS485 communication, twisted-pair lines are connected backward in the network. The TPT4089 has two pins that invert the phase of the driver and the receiver to correct this problem. For normal operation, drive TXP and RXP low, connect them to ground, or leave them unconnected with internal pulldown. Connect TXP as High to invert the driver phase. To invert the receiver phase, then the RXP should connect it to VCC, and note that the receiver threshold is positive in this status.

Application Information

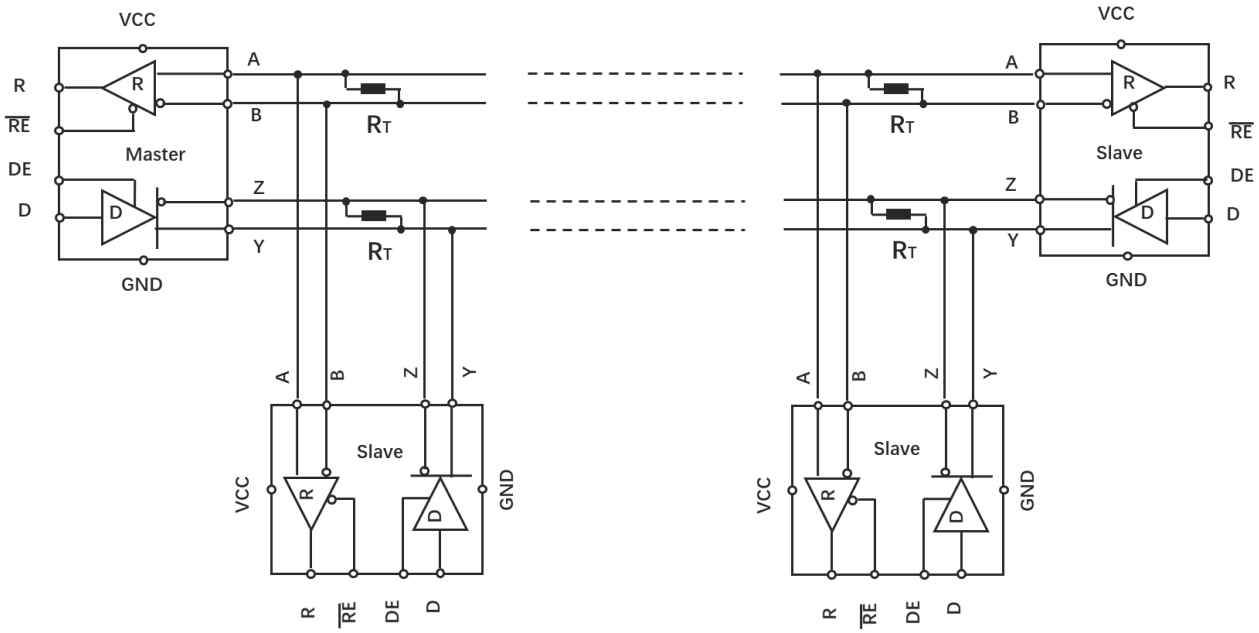
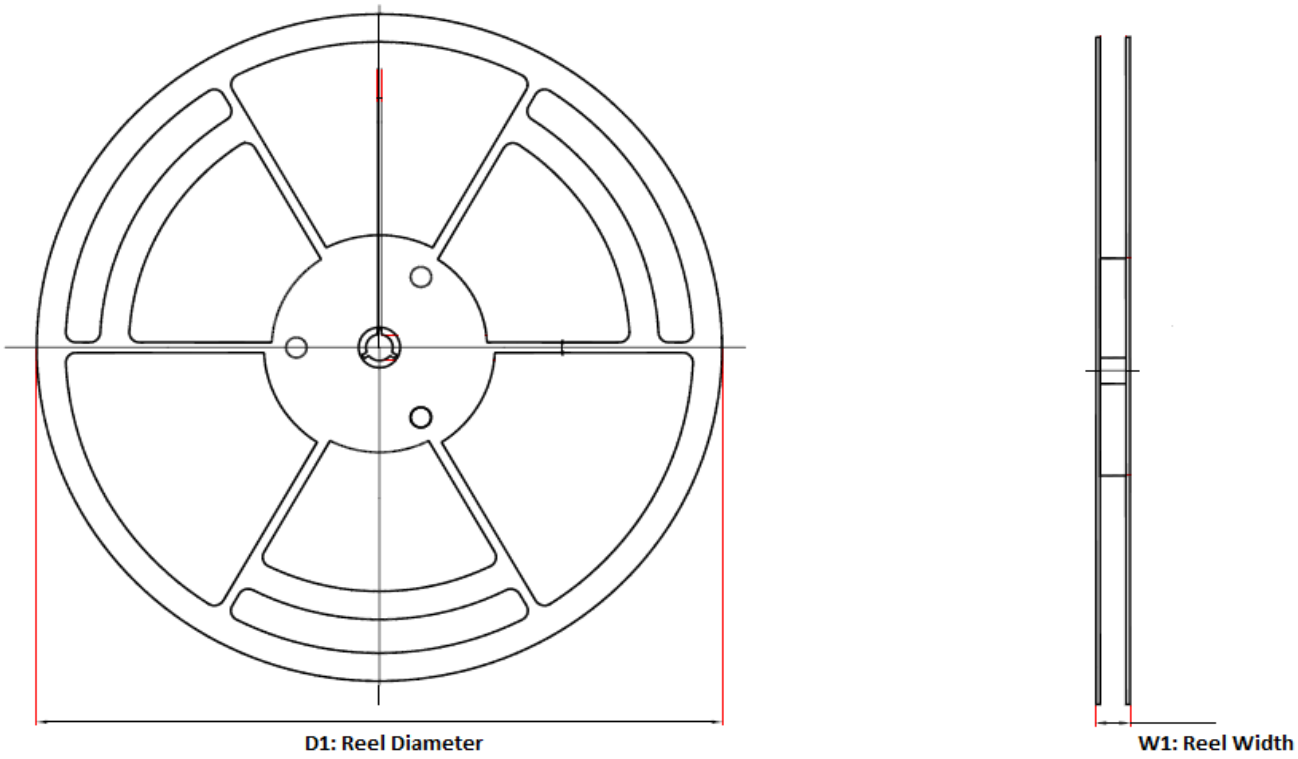


Figure 7. Typical RS485 communication network

The TPT4089 transceiver is designed for bidirectional RS485/422 data communications on multipoint bus transmission lines. Figures 7 shows typical network applications circuit to support up to 256 nodes. To minimize line reflections, terminate the line at both ends in its characteristic impedance, one 120ohm load in master side, and another 120ohm load in the end of slave side, and limit stub lengths off the main line as short as possible. TPT4089 is more tolerant of imperfect termination for 500Kbps low data rate and 32Mbps high data rate.

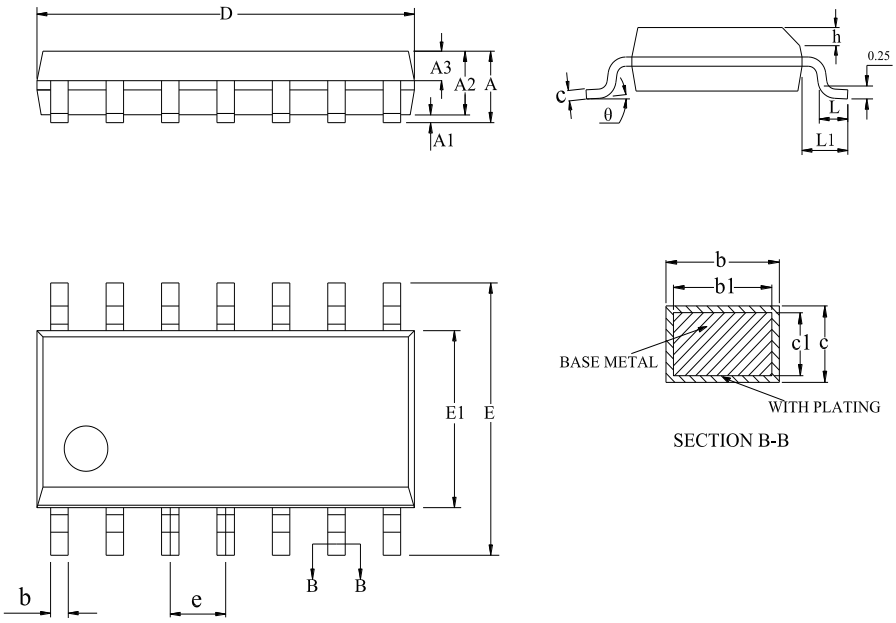
Tape and Reel Information



Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TPT4089-SO2R	14-Pin SOP	330.0	21.6	6.5	9.0	2.1	8.0	16.0	Q1

Package Outline Dimensions

SOP-14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

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