2-channel I²C-bus Master Arbiter

Features

- 2-to-1 Bidirectional Master Arbiter
- Channel Selection via I²C-bus
- Compatible with SMBus Standards
- 2 Active LOW Interrupt Outputs to Master Controllers
- Active LOW Reset Input
- Software Reset
- Four Address Pins Allowing up to 112 Different Addresses
- Arbitration Active when Two Masters Try to Take the Downstream I²C-bus at the Same Time
- The Winning Master Controls the Downstream Bus Until it is Done, as Long as It is within the Reserve Time
- Bus Time-out After 150 ms on an Inactive Downstream I²C-bus (Optional)
- Readable Device ID (Manufacturer, Device type, and Revision)
- Bus Initialization/Recovery Function
- Allows Voltage Level Translation Between 1.8-V, 2.3-V, 2.5-V, 3.3-V, and 3.6-V Buses
- Low Ron Switches
- No Glitch on Power-up
- Supports Hot Insertion
- Software Identical for both Masters
- Operating Power Supply Voltage Range of 2.3 V to 3.6 V
- All I/O Pins are 3.6 V Tolerant
- Up to 1 MHz Clock Frequency

Applications

- High Reliability Systems with Dual Masters
- Allows Masters without Arbitration Logic to Share Resources
- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets

Description

The TPT29641 is a 2-channel I²C bus master demultiplexer with an arbiter function. It allows masters without arbitration logic to share resources. The system maintains normal operation even when two masters issue their commands at the same time. The winning master gains control of the bus, while the losing master will wait to acquire control only after the winner releases the bus or when the reserve time expires. The TPT29641 also supports a master initiating requests and waiting while the other master retains control of the bus.

The TPT29641 supports hardware reset via an active-low $\overline{\text{RESET}}$ pin and software reset through the I²C bus. The device features two interrupt outputs ($\overline{\text{INT0}}$ and $\overline{\text{INT1}}$) and one interrupt input ($\overline{\text{INT\_IN}}$) to indicate bus control status, shared mailbox status, and downstream interrupt status. All interrupts can be disabled if the masking option is set.

The TPT29641 operates from 2.3 V to 3.6 V. The pass gates of the switches are constructed so that the V_{DD} terminal can be used to limit the maximum high voltage. It allows voltage level translation between 1.8-V, 2.3-V, 2.5-V, 3.3-V, and 3.6-V buses without any additional component. The TPT29641 does not isolate the capacitance on either side of the device. Pull-up resistors must be placed on all channels.

The TPT29641 is available in TSSOP16 and QFN3×3-16 packages, and is characterized from −40°C to +85°C.

Typical Application Circuit

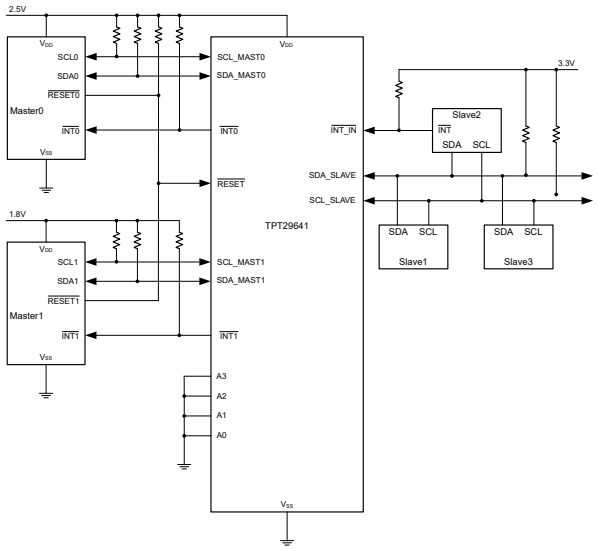


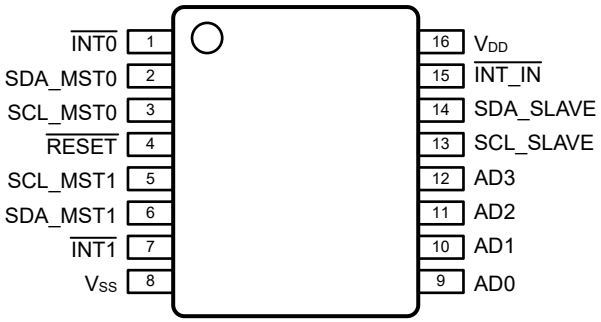
Table of Contents

Revision History

Date	Revision	Notes
2025-08-05	Rev.A.0	Released version.

Pin Configuration and Functions

TPT29641-TS3R
TSSOP16
Top View



TPT29641-QFNR
QFN3×3-16
Top View

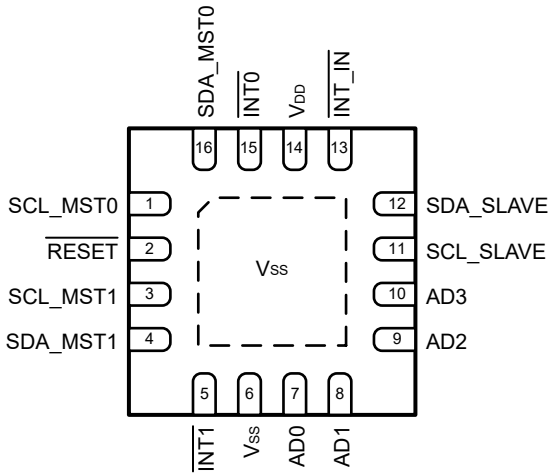


Table 1. Pin Functions: TPT29641

Pin No.		Name	I/O	Description
TSSOP16	QFN3×3-16			
1	15	$\overline{\text{INT0}}$	O	Active LOW interrupt output 0 (external pull-up required)
2	16	SDA_MST0	I/O	Serial data master 0 (external pull-up required)
3	1	SCL_MST0	I/O	Serial clock master 0 (external pull-up required)
4	2	$\overline{\text{RESET}}$	I	Active LOW reset input (external pull-up required)
5	3	SCL_MST1	I/O	Serial clock master 1 (external pull-up required)
6	4	SDA_MST1	I/O	Serial data master 1 (external pull-up required)
7	5	$\overline{\text{INT1}}$	O	Active LOW interrupt output 1 (external pull-up required)
8	6	V_{SS}	-	Supply ground
9	7	AD0	I	Address input 0 (externally held to VSS, VDD, pull-up to VDD or pull-down to VSS)
10	8	AD1	I	Address input 1 (externally held to VSS, VDD, pull-up to VDD or pull-down to VSS)
11	9	AD2	I	Address input 2 (externally held to VSS, VDD, pull-up to VDD or pull-down to VSS)
12	10	AD3	I	Address input 3 (externally held to VSS, VDD, pull-up to VDD or pull-down to VSS)

Pin No.		Name	I/O	Description
TSSOP16	QFN3×3-16			
13	11	SCL_SLAVE	I/O	Serial clock slave (external pull-up required)
14	12	SDA_SLAVE	I/O	Serial data slave (external pull-up required)
15	13	$\overline{\text{INT\_IN}}$	I	Active LOW interrupt input (external pull-up required)
16	14	V_{DD}	-	Supply voltage

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{DD}	Supply Voltage	−0.5	4	V
V_I	Input Voltage	−0.5	4	V
I_{IK}	Input Clamp Current, $V_I < 0$	−20	20	mA
I_{OK}	Output Clamp Current, $V_O < 0$	−25	25	mA
I_{DD}	Continuous Current Through GND	−100	100	mA
P_{tot}	Total Power Dissipation		400	mW
T_A	Operating Temperature Range	−40	85	°C
T_{stg}	Storage Temperature Range	−60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{DD}	Supply Voltage	2.3	3.6	V
T_A	Operating Temperature Range	−40	85	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP16	107	38	°C/W
QFN3X3-16	62	56	°C/W

Electrical Characteristics - DC Parameters

All test conditions: V_{DD} = 2.3 V to 3.6 V, V_{SS} = 0 V, T_A = −40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	Power Supply		2.3		3.6	V
I_{DD}	Supply Current in Operating Mode	V_{DD} = 2.3 V; No load; V_I = V_{DD} or V_{SS}; f_{SCL} = 1 MHz		122	210	μA
		V_{DD} = 3.6 V; No load; V_I = V_{DD} or V_{SS}; f_{SCL} = 1 MHz		177	325	μA
	Standby Current	V_{DD} = 2.3 V; No load; V_I = V_{DD} or V_{SS}; f_{SCL} = 0 kHz		102	160	μA
		V_{DD} = 3.6 V; No load; V_I = V_{DD} or V_{SS}; f_{SCL} = 0 kHz		131	275	μA
V_{POR}	Power-on Reset Voltage, V_{DD} Rising	No load; V_I = V_{DD} or V_{SS};		1.9	2.1	V
Input SCL_MSTn; Input/Output SDA_MSTn						
V_{IL}	Low-Level Input Voltage		−0.5		0.3×V_{DD}	V
V_{IH}	High-Level Input Voltage		0.7×V_{DD}		3.6	V
I_{OL}	Low-Level Output Current, SDA_MSTn	V_{OL} = 0.4 V	20	38		mA
I_L	Leakage Current	V_I = V_{DD} or V_{SS}	−1		1	μA
C_i	Input Capacitance (1)	V_I = V_{SS}		6	10	pF
Select Inputs A0 to A3, $\overline{\text{RESET}}$, $\overline{\text{INT\_IN}}$						
V_{IL}	Low-Level Input Voltage		−0.5		0.3×V_{DD}	V
V_{IH}	High-Level Input Voltage		0.7×V_{DD}		3.6	V
I_{LI}	Input Leakage Current	V_I = V_{DD} or V_{SS}	−1		1	μA
C_i	Input Capacitance (1)	V_I = V_{SS}		4	10	pF
Pass Gate						
R_{on}	On-State Resistance	V_{DD} = 3.0 V to 3.6 V; V_O = 0.4 V; I_O = 20 mA		6	11.5	Ω
		V_{DD} = 2.3 V to 2.7 V; V_O = 0.4 V; I_O = 20 mA		9	14.5	Ω
$V_{O\ (SW)}$	Switch Output Voltage	$V_{I\ (SW)}$ = V_{DD} = 3.6 V; $I_{O\ (SW)}$ = −100 μA	1.6	2.4	2.8	V
		$V_{I\ (SW)}$ = V_{DD} = 2.3 V; $I_{O\ (SW)}$ = −100 μA	1.1	1.3	2.2	V
I_L	Leakage Current, SDA_SLAVE, SCL_SLAVE	V_I = V_{DD} or V_{SS}	−1		1	μA
$\overline{\text{INT0}}$, $\overline{\text{INT1}}$						
I_{OL}	Low-Level Output Current	V_{OL} = 0.4 V	3			mA

(1) Parameters are provided by the lab bench test and design simulation.

Electrical Characteristics - AC Parameters

I²C Interface Timing Requirements

All test conditions: V_{DD} = 2.3 V to 3.6 V, V_{SS} = 0 V, unless otherwise noted.

Symbol	Description	Condition	Normal-mode		Fast-mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
t_{pd}	Propagation Delay Time (1)	from SDA_MSTn to SDA_SLAVE, or SCL_MSTn to SCL_SLAVE		0.3		0.3		0.3	ns
f_{scl}	I²C Clock Frequency		0	100	0	400	0	1000	kHz
$f_{scl(init/rec)}$	SCL Clock Frequency (Bus Initialization/Bus Recovery)		18	52	18	52	18	52	kHz
t_{buf}	I²C Bus Free Time Between Stop and Start		4.7		1.3		0.5		µs
t_{sch}	I²C Clock High Time		4		0.6		0.26		µs
t_{scl}	I²C Clock Low Time		4.7		1.3		0.5		µs
t_{sts}	I²C Start or Repeated Start Condition Setup Time		4.7		0.6		0.26		µs
t_{sth}	I²C Start or Repeated Start Condition Hold Time		4		0.6		0.26		µs
t_{sps}	I²C Stop Condition Setup Time		4		0.6		0.26		µs
t_{sds}	I²C Serial-Data Setup Time		250		100		50		ns
t_{sdh}	I²C Serial-Data Hold Time		0		0		0		ns
t_r	Rise Time of Both SDA and SCL			1000	20	300		120	ns
t_f	Fall Time of Both SDA and SCL (2)			300	20 × (V_{DD} / 3.3 V)	300	20 × (V_{DD} / 3.3 V)	120	ns
C_b	I²C Bus Capacitive Load (3)			400		400		500	pF
t_{sp}	I²C Spike Time			50		50		50	ns
$t_{vd(data)}$	Valid Data Time	SCL low to SDA output valid		1		1	0.05	0.45	µs
$t_{vd(ack)}$	Valid Data Time of ACK Condition	ACK signal from SCL low to SDA (out) low		1		1	0.05	0.45	µs

(1) The propagation delay is calculated from the 20-Ω typical Ron and the 15-pF load capacitance.
(2) All the parameters in the above table are requested by the I²C standard, not tested in production.
(3) C_b is the total capacitance of one bus line in pF.

Switching Characteristics

All test conditions: V_{DD} = 2.3 V to 3.6 V, V_{SS} = 0 V, C_L ≤ 100 pF, unless otherwise noted.

Symbol	Description	Condition	Min	Max	Unit
$\overline{\text{RESET}}$ Timing					
$t_{w(rst)L}$	Low-Level Reset Time		10		ns
t_{rst}	Reset Time	SDA clear		500	ns
$t_{REC;\ STA}$	Recovery Time to Start Condition (1) (2)			90	µs
$\overline{\text{INT}}$ Timing					
$t_{v(int)}$	Valid Time from Pin $\overline{\text{INT\_IN}}$ to $\overline{\text{INTn}}$			4	µs
$t_{w(rej)}$	$\overline{\text{INT\_IN}}$ Rejection Time		0.05		µs

(1) Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.

(2) Upon reset, the full delay will be the sum of t_{rst} and the RC time constant of the SDA bus.

Parameter Measurement Waveforms

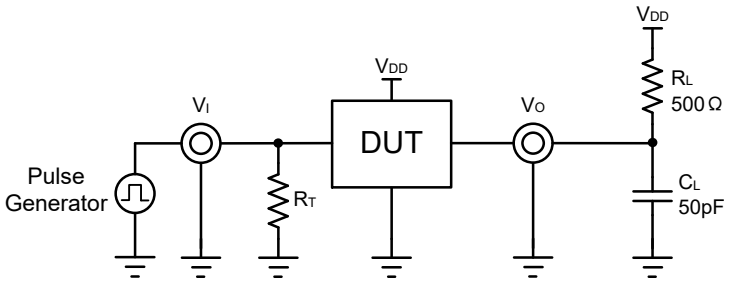


Figure 1. Test Circuitry for Switching Times

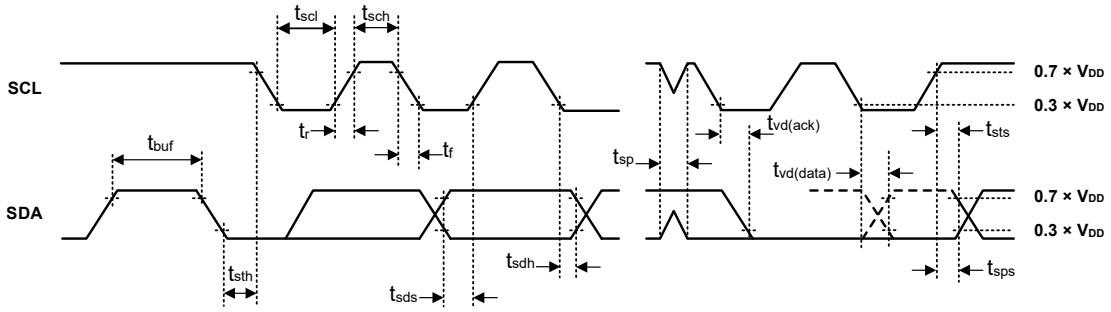


Figure 2. Definition of Timing on the I²C-bus

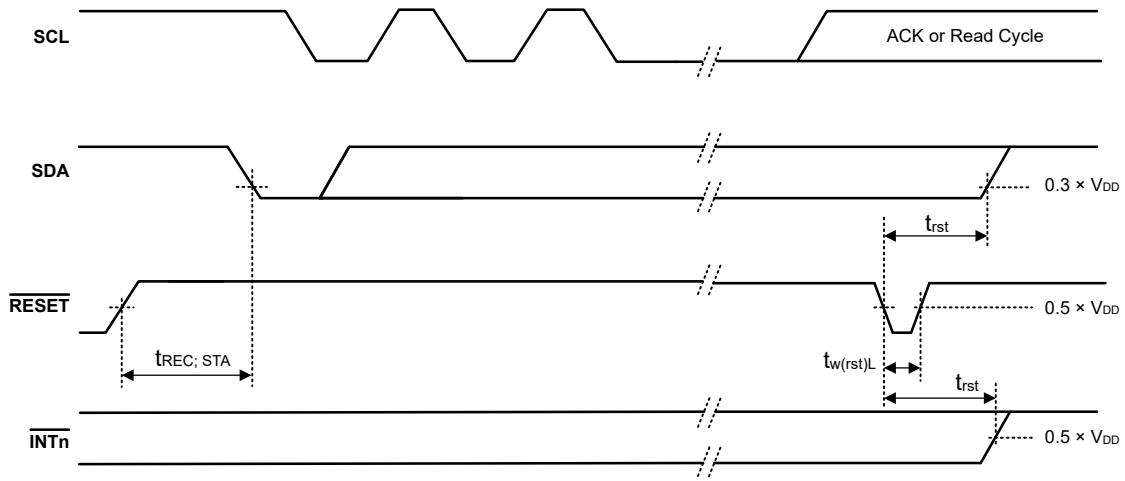


Figure 3. Definition of $\overline{\text{RESET}}$ Timing

Detailed Description

Overview

The TPT29641 is a 2-channel I²C bus master demultiplexer with an arbiter function. It allows masters without arbitration logic to share resources. The system maintains normal operation even when two masters issue their commands at the same time. The winning master gains control of the bus, while the losing master will wait to acquire control only after the winner releases the bus or when the reserve time expires. The TPT29641 also supports a master initiating requests and waiting while the other master retains control of the bus.

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The TPT29641 operates from 2.3 V to 3.6 V. The pass gates of the switches are constructed so that the V_{DD} terminal can be used to limit the maximum high voltage. It allows voltage level translation among 1.8-V, 2.3-V, 2.5-V, 3.3-V, and 3.6-V buses without any additional component. The TPT29641 does not isolate the capacitance on either side of the device. Pull-up resistors must be placed on all channels.

Functional Block Diagram

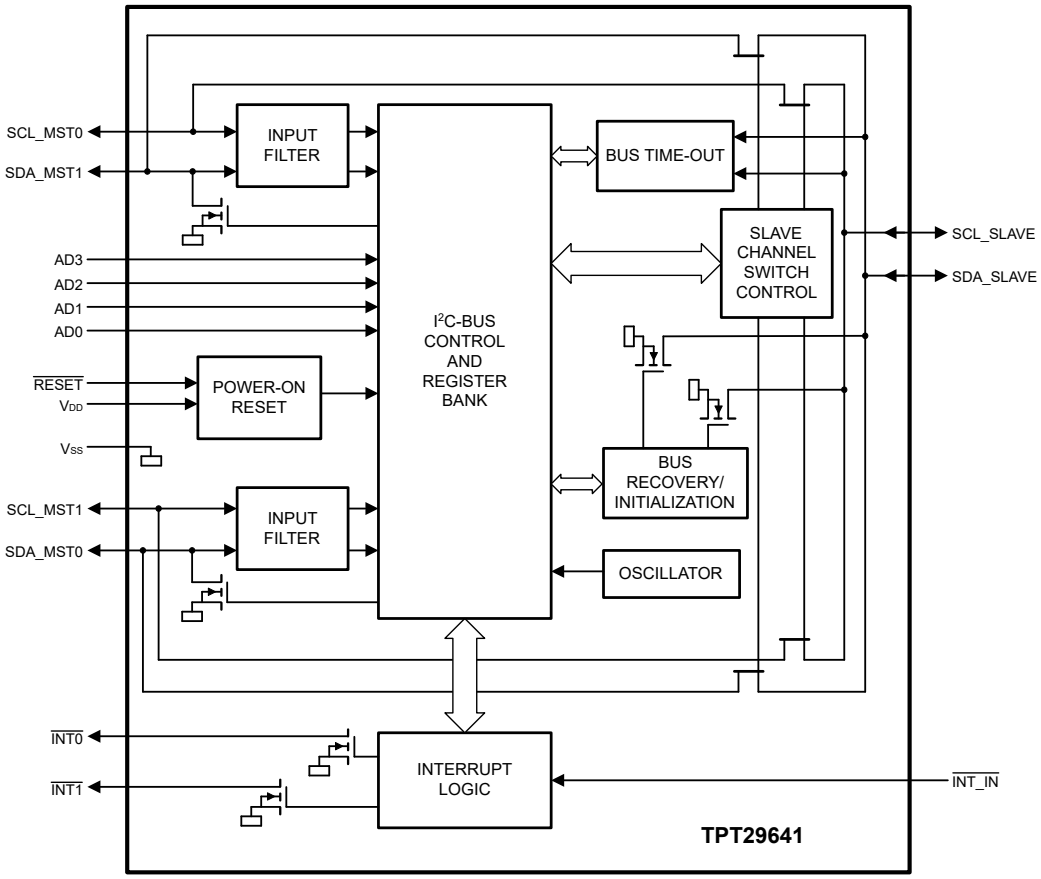


Figure 4. Functional Block Diagram

Feature Description

Device Address

Following a START condition, the bus master must output the address of the slave it has access to. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins, and they must be connected to VDD, VSS, pull-up to VDD (PU), or pull-down to VSS (PD). The TPT29641 supports 112 decodable addresses, configured by connections of input pads AD3, AD2, AD1, and AD0. The specific address mapping is defined in Table 3.

Upon device power-up or hardware/software reset, the states of the address input pins are sampled to configure the slave address of TPT29641. To conserve power, once the slave address is determined, the address input pads are turned off and will not be sampled until the next power-on. Table 2 specifies four connection configurations for the address input pins with the corresponding external resistor values required.

Table 2. Input Pad Connection

Pad Connection (AD3, AD2, AD1, AD0)	Mnemonic	External Resistor	
		Min	Max
tie to V_{SS}	VSS	0 kΩ	17.9 kΩ
resistor pull-down to V_{SS}	PD	34.8 kΩ	270 kΩ
resistor pull-up to V_{DD}	PU	31.7 kΩ	340 kΩ
tie to V_{DD}	VDD	0 kΩ	21 kΩ

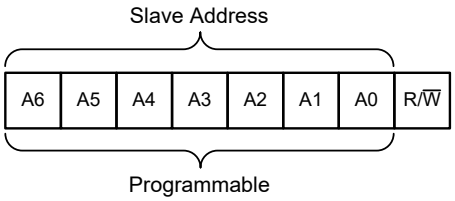


Figure 5. TPT29641 Address

Table 3. Address Maps

Pin Connectivity				Address of TPT29641								Address Byte Value		7-bit Hexadecimal Address Without R/W
AD3	AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	R/W	Write	Read	
VSS	VSS	VSS	VSS	1	1	1	0	0	0	0	-	E0h	E1h	70h
VSS	VSS	VSS	VDD	1	1	1	0	0	0	1	-	E2h	E3h	71h
VSS	VSS	VDD	VSS	1	1	1	0	0	1	0	-	E4h	E5h	72h
VSS	VSS	VDD	VDD	1	1	1	0	0	1	1	-	E6h	E7h	73h
VSS	VDD	VSS	VSS	1	1	1	0	1	0	0	-	E8h	E9h	74h
VSS	VDD	VSS	VDD	1	1	1	0	1	0	1	-	EAh	EBh	75h
VSS	VDD	VDD	VSS	1	1	1	0	1	1	0	-	ECh	EDh	76h
VSS	VDD	VDD	VDD	1	1	1	0	1	1	1	-	EEh	EFh	77h

Pin Connectivity				Address of TPT29641								Address Byte Value		7-bit Hexadecimal Address Without R/$\overline{W}$
AD3	AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$	Write	Read	
VDD	VSS	VSS	PD	0	0	0	1	0	0	0	-	10h	11h	08h
VDD	VSS	VSS	PU	0	0	0	1	0	0	1	-	12h	13h	09h
VDD	VSS	VDD	PD	0	0	0	1	0	1	0	-	14h	15h	0Ah
VDD	VSS	VDD	PU	0	0	0	1	0	1	1	-	16h	17h	0Bh
VDD	VDD	VSS	PD	0	0	0	1	1	0	0	-	18h	19h	0Ch
VDD	VDD	VSS	PU	0	0	0	1	1	0	1	-	1Ah	1Bh	0Dh
VDD	VDD	VDD	PD	0	0	0	1	1	1	0	-	1Ch	1Dh	0Eh
VDD	VDD	VDD	PU	0	0	0	1	1	1	1	-	1Eh	1Fh	0Fh
VSS	VSS	PD	VSS	0	0	1	0	0	0	0	-	20h	21h	10h
VSS	VSS	PD	VDD	0	0	1	0	0	0	1	-	22h	23h	11h
VSS	VSS	PU	VSS	0	0	1	0	0	1	0	-	24h	25h	12h
VSS	VSS	PU	VDD	0	0	1	0	0	1	1	-	26h	27h	13h
VSS	VDD	PD	VSS	0	0	1	0	1	0	0	-	28h	29h	14h
VSS	VDD	PD	VDD	0	0	1	0	1	0	1	-	2Ah	2Bh	15h
VSS	VDD	PU	VSS	0	0	1	0	1	1	0	-	2Ch	2Dh	16h
VSS	VDD	PU	VDD	0	0	1	0	1	1	1	-	2Eh	2Fh	17h
VDD	VSS	PD	VSS	0	0	1	1	0	0	0	-	30h	31h	18h
VDD	VSS	PD	VDD	0	0	1	1	0	0	1	-	32h	33h	19h
VDD	VSS	PU	VSS	0	0	1	1	0	1	0	-	34h	35h	1Ah
VDD	VSS	PU	VDD	0	0	1	1	0	1	1	-	36h	37h	1Bh
VDD	VDD	PD	VSS	0	0	1	1	1	0	0	-	38h	39h	1Ch
VDD	VDD	PD	VDD	0	0	1	1	1	0	1	-	3Ah	3Bh	1Dh
VDD	VDD	PU	VSS	0	0	1	1	1	1	0	-	3Ch	3Dh	1Eh
VDD	VDD	PU	VDD	0	0	1	1	1	1	1	-	3Eh	3Fh	1Fh
VSS	VSS	PD	PD	0	1	0	0	0	0	0	-	40h	41h	20h
VSS	VSS	PD	PU	0	1	0	0	0	0	1	-	42h	43h	21h
VSS	VSS	PU	PD	0	1	0	0	0	1	0	-	44h	45h	22h
VSS	VSS	PU	PU	0	1	0	0	0	1	1	-	46h	47h	23h
VSS	VDD	PD	PD	0	1	0	0	1	0	0	-	48h	49h	24h
VSS	VDD	PD	PU	0	1	0	0	1	0	1	-	4Ah	4Bh	25h
VSS	VDD	PU	PD	0	1	0	0	1	1	0	-	4Ch	4Dh	26h
VSS	VDD	PU	PU	0	1	0	0	1	1	1	-	4Eh	4Fh	27h
VDD	VSS	PD	PD	0	1	0	1	0	0	0	-	50h	51h	28h
VDD	VSS	PD	PU	0	1	0	1	0	0	1	-	52h	53h	29h
VDD	VSS	PU	PD	0	1	0	1	0	1	0	-	54h	55h	2Ah
VDD	VSS	PU	PU	0	1	0	1	0	1	1	-	56h	57h	2Bh

Pin Connectivity				Address of TPT29641								Address Byte Value		7-bit Hexadecimal Address Without R/$\overline{W}$
AD3	AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$	Write	Read	
VDD	VDD	PD	PD	0	1	0	1	1	0	0	-	58h	59h	2Ch
VDD	VDD	PD	PU	0	1	0	1	1	0	1	-	5Ah	5Bh	2Dh
VDD	VDD	PU	PD	0	1	0	1	1	1	0	-	5Ch	5Dh	2Eh
VDD	VDD	PU	PU	0	1	0	1	1	1	1	-	5Eh	5Fh	2Fh
VSS	PD	VSS	VSS	0	1	1	0	0	0	0	-	60h	61h	30h
VSS	PD	VSS	VDD	0	1	1	0	0	0	1	-	62h	63h	31h
VSS	PD	VDD	VSS	0	1	1	0	0	1	0	-	64h	65h	32h
VSS	PD	VDD	VDD	0	1	1	0	0	1	1	-	66h	67h	33h
VSS	PU	VSS	VSS	0	1	1	0	1	0	0	-	68h	69h	34h
VSS	PU	VSS	VDD	0	1	1	0	1	0	1	-	6Ah	6Bh	35h
VSS	PU	VDD	VSS	0	1	1	0	1	1	0	-	6Ch	6Dh	36h
VSS	PU	VDD	VDD	0	1	1	0	1	1	1	-	6Eh	6Fh	37h
VDD	PD	VSS	VSS	0	1	1	1	0	0	0	-	70h	71h	38h
VDD	PD	VSS	VDD	0	1	1	1	0	0	1	-	72h	73h	39h
VDD	PD	VDD	VSS	0	1	1	1	0	1	0	-	74h	75h	3Ah
VDD	PD	VDD	VDD	0	1	1	1	0	1	1	-	76h	77h	3Bh
VDD	PU	VSS	VSS	0	1	1	1	1	0	0	-	78h	79h	3Ch
VDD	PU	VSS	VDD	0	1	1	1	1	0	1	-	7 Ah	7Bh	3Dh
VDD	PU	VDD	VSS	0	1	1	1	1	1	0	-	7Ch	7Dh	3Eh
VDD	PU	VDD	VDD	0	1	1	1	1	1	1	-	7Eh	7Fh	3Fh
VSS	PD	VSS	PD	1	0	0	0	0	0	0	-	80h	81h	40h
VSS	PD	VSS	PU	1	0	0	0	0	0	1	-	82h	83h	41h
VSS	PD	VDD	PD	1	0	0	0	0	1	0	-	84h	85h	42h
VSS	PD	VDD	PU	1	0	0	0	0	1	1	-	86h	87h	43h
VSS	PU	VSS	PD	1	0	0	0	1	0	0	-	88h	89h	44h
VSS	PU	VSS	PU	1	0	0	0	1	0	1	-	8Ah	8Bh	45h
VSS	PU	VDD	PD	1	0	0	0	1	1	0	-	8Ch	8Dh	46h
VSS	PU	VDD	PU	1	0	0	0	1	1	1	-	8Eh	8Fh	47h
VDD	PD	VSS	PD	1	0	0	1	0	0	0	-	90h	91h	48h
VDD	PD	VSS	PU	1	0	0	1	0	0	1	-	92h	93h	49h
VDD	PD	VDD	PD	1	0	0	1	0	1	0	-	94h	95h	4Ah
VDD	PD	VDD	PU	1	0	0	1	0	1	1	-	96h	97h	4Bh
VDD	PU	VSS	PD	1	0	0	1	1	0	0	-	98h	99h	4Ch
VDD	PU	VSS	PU	1	0	0	1	1	0	1	-	9Ah	9Bh	4Dh
VDD	PU	VDD	PD	1	0	0	1	1	1	0	-	9Ch	9Dh	4Eh
VDD	PU	VDD	PU	1	0	0	1	1	1	1	-	9Eh	9Fh	4Fh

Pin Connectivity				Address of TPT29641								Address Byte Value		7-bit Hexadecimal Address Without R/$\overline{W}$
AD3	AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$	Write	Read	
VSS	PD	PD	VSS	1	0	1	0	0	0	0	-	A0h	A1h	50h
VSS	PD	PD	VDD	1	0	1	0	0	0	1	-	A2h	A3h	51h
VSS	PD	PU	VSS	1	0	1	0	0	1	0	-	A4h	A5h	52h
VSS	PD	PU	VDD	1	0	1	0	0	1	1	-	A6h	A7h	53h
VSS	PU	PD	VSS	1	0	1	0	1	0	0	-	A8h	A9h	54h
VSS	PU	PD	VDD	1	0	1	0	1	0	1	-	AAh	ABh	55h
VSS	PU	PU	VSS	1	0	1	0	1	1	0	-	ACh	ADh	56h
VSS	PU	PU	VDD	1	0	1	0	1	1	1	-	AEh	AFh	57h
VDD	PD	PD	VSS	1	0	1	1	0	0	0	-	B0h	B1h	58h
VDD	PD	PD	VDD	1	0	1	1	0	0	1	-	B2h	B3h	59h
VDD	PD	PU	VSS	1	0	1	1	0	1	0	-	B4h	B5h	5Ah
VDD	PD	PU	VDD	1	0	1	1	0	1	1	-	B6h	B7h	5Bh
VDD	PU	PD	VSS	1	0	1	1	1	0	0	-	B8h	B9h	5Ch
VDD	PU	PD	VDD	1	0	1	1	1	0	1	-	BAh	BBh	5Dh
VDD	PU	PU	VSS	1	0	1	1	1	1	0	-	BCh	BDh	5Eh
VDD	PU	PU	VDD	1	0	1	1	1	1	1	-	BEh	BFh	5Fh
VSS	PD	PD	PD	1	1	0	0	0	0	0	-	C0h	C1h	60h
VSS	PD	PD	PU	1	1	0	0	0	0	1	-	C2h	C3h	61h
VSS	PD	PU	PD	1	1	0	0	0	1	0	-	C4h	C5h	62h
VSS	PD	PU	PU	1	1	0	0	0	1	1	-	C6h	C7h	63h
VSS	PU	PD	PD	1	1	0	0	1	0	0	-	C8h	C9h	64h
VSS	PU	PD	PU	1	1	0	0	1	0	1	-	CAh	CBh	65h
VSS	PU	PU	PD	1	1	0	0	1	1	0	-	CCh	CDh	66h
VSS	PU	PU	PU	1	1	0	0	1	1	1	-	CEh	CFh	67h
VDD	PD	PD	PD	1	1	0	1	0	0	0	-	D0h	D1h	68h
VDD	PD	PD	PU	1	1	0	1	0	0	1	-	D2h	D3h	69h
VDD	PD	PU	PD	1	1	0	1	0	1	0	-	D4h	D5h	6Ah
VDD	PD	PU	PU	1	1	0	1	0	1	1	-	D6h	D7h	6Bh
VDD	PU	PD	PD	1	1	0	1	1	0	0	-	D8h	D9h	6Ch
VDD	PU	PD	PU	1	1	0	1	1	0	1	-	DAh	DBh	6Dh
VDD	PU	PU	PD	1	1	0	1	1	1	0	-	DCh	DDh	6Eh
VDD	PU	PU	PU	1	1	0	1	1	1	1	-	DEh	DFh	6Fh

(1) Do not use any other combination addresses to decode hardware addresses.

Command Code

Following the successful acknowledgment of the slave address, the bus master sends a byte to the TPT29641, which is stored in the control register. The three least significant bits (3 LSBs) of the command code serve as a pointer to designate the target register for access. When the auto-increment flag (AI=1) is set, these 3 bits are automatically incremented after each byte read/write operation, facilitating sequential access to multiple registers. Upon reaching the last allowed register (pointer value 111b), the pointer rolls over to 000b. Unused bits in the command code must be set to 0.

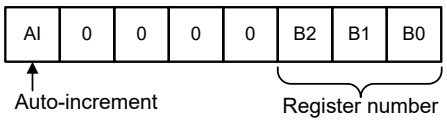


Figure 6. Command Code

Each master has 8 registers, as listed in Table 4 In addition to managing its own registers, each master can also read specific registers of another master.

Table 4. Command Code Register

B2	B1	B0	Register name	Type	Register Function
0	0	0	ID	R only	8-bit device ID
0	0	1	CONTR	R/W	control register
0	1	0	STATUS	R/W	status register
0	1	1	RT	R/W	reserve time
1	0	0	INT_STATUS	R/W	interrupt status register
1	0	1	INT_MSK	R/W	interrupt mask register
1	1	0	MB_LO	R/W	low 8 bits of the mail box
1	1	1	MB_HI	R/W	high 8 bits of the mail box

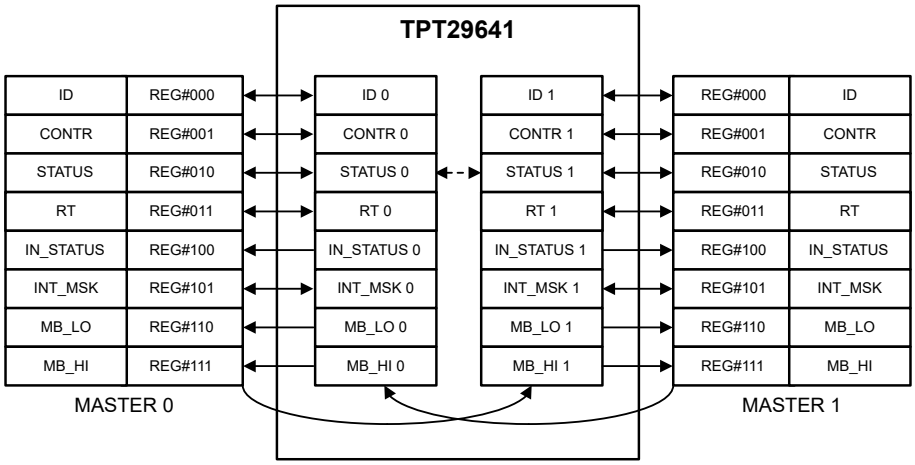


Figure 7. Internal Register Map

Power-on Reset

When power is supplied to the V_{DD} pin, the TPT29641 remains in a reset state due to an internal power-on reset until V_{DD} reaches the V_{PORR} threshold. At that moment, the reset is lifted, and the device's registers and I²C/SMBus state machine are initialized to their default settings. To reset the device again, V_{DD} must be decreased to below the V_{PORF} level.

$\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input is an active-LOW signal that helps recover from bus fault conditions. By pulling this signal LOW for at least tw(rst)L, the TPT29641 resets its register, I²C/SMBus state machine, and disconnects from the downstream.

Software Reset

Both granted and non-granted masters can trigger a software reset on the TPT29641 and all internal registers will be reset to their default states. If SWRET is enabled, the TPT29641 will send SCL LOW for more than 35 ms to the downstream bus before the reset occurs. During this period, the master should not access registers until the reset completes. If SWRET is disabled, the TPT29641 resets immediately without sending SCL LOW.

Voltage Translation

The pass gates of the switches are constructed so that the V_{DD} terminal can be used to limit the maximum high voltage. For the TPT29641 to act as a voltage translator, the $V_{o(sw)}$ voltage should be equal to or lower than the lowest bus voltage. $V_{o(sw)}$ is the pass gate voltage (V_{pass}) of the switches. This allows voltage level translation between 1.8-V, 2.3-V, 2.5-V, 3.3-V, and 3.6-V buses when the $V_{o(sw)}$ voltage is equal to or lower than the lowest bus voltage. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 3.6-V tolerant.

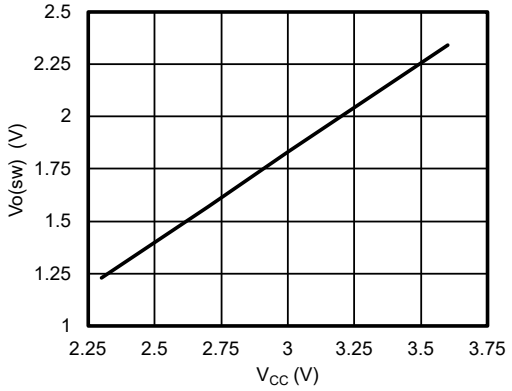


Figure 8. Pass Gate Voltage ($V_{O(SW)}$) vs. Supply Voltage (V_{CC})

Register Description

Register 0: ID Register ([B2:B0] = 000b)

This register stores the least significant 8 bits of the Device ID. A read operation on this register returns the fixed value 38h.

Table 5. ID - Device ID Register (Pointer Address 00h) Bit Description

Address	Register	Bit	Access	Description
00h	ID	7 to 0	R only	Hard-coded 38h for TPT29641

Register 1: Control Register ([B2:B0] = 001b)

The control registers described below are identical for both Master 0 and Master 1. However, two separate internal control registers exist physically, each dedicated to one master.

Table 6. CONTR - Control Register (Pointer Address 01h) Bit Description

Bit	Symbol	Access	Value	Description
7	PRIORITY	R/W		Master can set this register bit for setting the priority of the winner when two masters request the downstream bus at the same time. Table 7 shows how TPT29641 selects the winner when 2 masters set their own PRIORITY bit.
			0 *	Master can configure the priority bit for the case where two masters request the downstream bus at the same time. See Table 7 for information on how TPT29641 selects the winner.
6	SMBUS_DIS	R/W		When TPT29641 detects an SMBus time-out, if this bit is set, TPT29641 will disconnect the I²C-bus from the master to the downstream bus.
			0 *	Normal operation
			1	Connectivity between the master and the downstream bus will be disconnected upon detecting an SMBus time-out condition.
5	IDLE_TIMER_DIS	R/W		After RES_TIME expires, the I²C-bus idle for more than 150 ms, TPT29641 will disconnect the master from the downstream bus and take away its grant if this register bit is enabled. This IDLE_TIMER_DIS function also applies when there is a grant of a request with a zero value on RES_TIME.
			0 *	Normal operation.
			1	Enable 150 ms idle timer. After the reserve timer expires or if the reserve timer is disabled, if the downstream bus is idle for more than 100 ms, the connection between the master and the downstream bus will be disconnected.
4	SMBUS_SWRST	R/W		Non-granted or granted master sends a soft reset, if this bit is set, TPT29641 sets the clock LOW for 35 ms before reset of all register values to defaults

Bit	Symbol	Access	Value	Description
			0 *	Normal operation.
			1	Enable sending SMBus time-out to the downstream bus, after receiving a general call soft reset from the master.
3	BUS_INIT	R/W		Bus initialization for TPT29641 sends one clock out and checks the SDA signal. If SDA is HIGH, TPT29641 sends a STOP condition. The BUS_INIT function is completed. If SDA is LOW, TPT29641 sends the other clock out and checks SDA again. The TPT29641 will send out 9 clocks (maximum), and if SDA is still LOW, TPT29641 determines that the bus initialization has failed.
			0 *	Normal operation.
			1	Start initialization on the next bus connect function to the downstream bus.
2	BUS_CONNECT	R/W		Connectivity between master and downstream bus; the internal switch connects the I²C-bus from the master to the downstream bus only if LOCK_GRANT = 1.
			0 *	Do not connect the I²C-bus from the master to the downstream bus.
			1	Connect downstream bus; the internal switch is closed only if LOCK_GRANT = 1.
1	LOCK_GRANT	R only		This is a status read-only register bit. Lock grant status register bit indicates the ownership between the reading master and the downstream bus. If this register bit is 1, the reading master owns the downstream bus. If this register bit is zero, the reading master has not owned the downstream bus.
			0 *	This master does not have a lock on the downstream bus.
			1	This master has a lock on the downstream bus.
0	LOCK_REQ	R/W		Lock request register bit is for a master requesting the downstream bus when it does not have a lock on the downstream bus. When a master has a lock on the downstream bus, it can give up the ownership by writing zero to LOCK_REQ register bit. When LOCK_REQ becomes zero, LOCK_GRANT bit becomes zero, and the internal switch will be open
			0 *	Master is not requesting a lock on the downstream bus or giving up the lock if the master had a lock on the downstream bus.
			1	Master is requesting a lock on the downstream bus.

(1) POR = 00h.
(2) Legend: * default value

Table 7. How TPT29641 Selects the Winner

Master 0 Priority	Master 1 Priority	Last Master Granted	Result
0	0	none	Grant is given to Master 0
0	0	Master 0	Grant is given to Master 1
0	0	Master 1	Grant is given to Master 0
0	1	NA	Grant is given to Master 1
1	0	NA	Grant is given to Master 0
1	1	none	Grant is given to Master 1
1	1	Master 0	Grant is given to Master 1
1	1	Master 1	Grant is given to Master 0

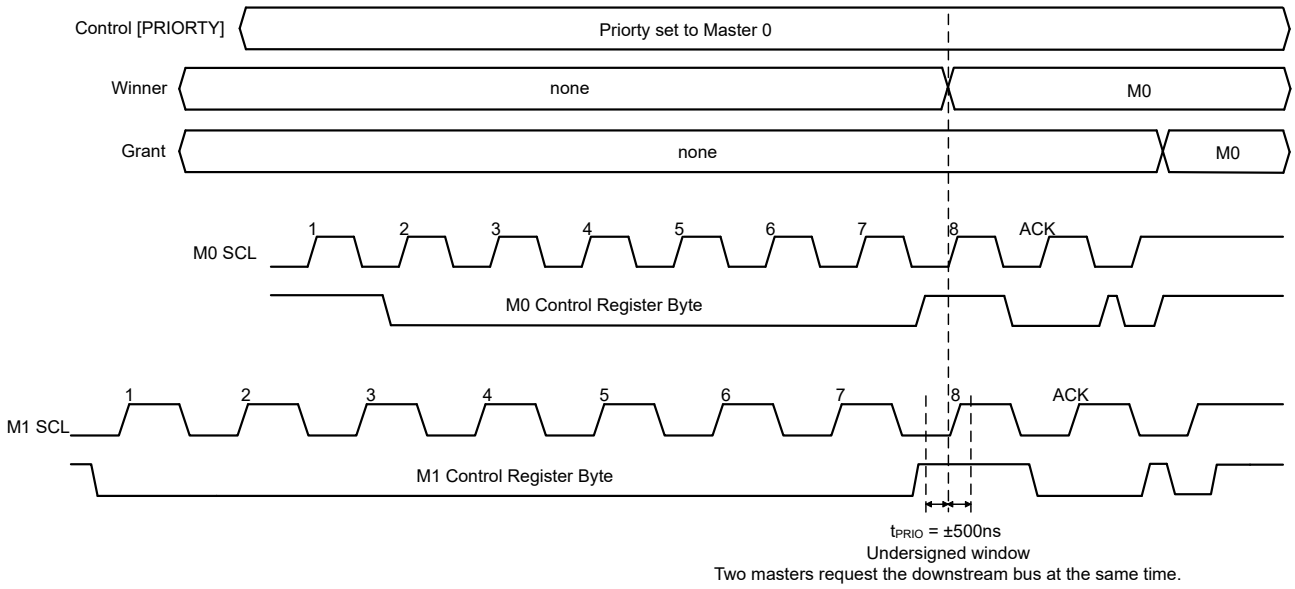


Figure 9. Two Masters Request the Downstream Bus at the Same Time

Register 2: Status Register ([B2:B0] = 010b)

Table 8. STATUS - Status Register (Pointer Address 02h) Bit Description

Bit	Symbol	Access	Value	Description
7	SDA_IO	R/W		SDA becomes I/O pin; the master can read or write to this register bit. If the master reads this bit, the value is the state of the downstream SDA pin. Zero value means SDA is LOW, and one means SDA pin is HIGH. When the master writes '0' to this register bit, the downstream SDA pin will assert LOW. If the master writes '1' to this register bit, the downstream SDA pin will be pulled HIGH.

Bit	Symbol	Access	Value	Description
				Remark: SDA becomes I/O pin only when BUS_CONNECT = 0 and LOCK_GRANT = 1.
			0 *	When read, it indicates the SDA pin of the downstream bus is LOW. When written, TPT29641 drives the SDA pin of the downstream bus LOW.
			1	When read, it indicates the SDA pin of the downstream bus is HIGH. When written, TPT29641 drives the SDA pin of the downstream bus HIGH.
6	SCL_IO	R/W		SCL becomes I/O pin; the master can read or write to this register bit. If the master reads this bit, the value is the state of the downstream SCL pin. Zero value means SCL is LOW, and one means SCL pin is HIGH. When the master writes '0' to this register bit, the downstream SCL pin will assert LOW. If the master writes '1' to this register bit, the downstream SCL pin will be pulled HIGH. Remark: SCL becomes I/O pin only when BUS_CONNECT = 0 and LOCK_GRANT = 1.
			0 *	When read, it shows the SCL pin of the downstream bus is LOW. When written, TPT29641 drives the SCL pin of the downstream bus LOW.
			1	When read, it shows the SCL pin of the downstream bus is HIGH. When written, TPT29641 drives the SCL pin of the downstream bus HIGH.
5	TEST_INT	W only		Test interrupt output pin; a master can send an interrupt to itself by writing '1' to this register bit. Writing '0' to this register bit has no effect. To clear this interrupt, the master must write '1' to TEST_INT_INT in the Interrupt Status register.
			0 *	Normal operation.
			1	Causes the TPT29641 $\overline{\text{INT}}$ pin to go LOW if not masked by TEST_INT_INT in the Interrupt Mask register. Allows this master to invoke its Interrupt Service Routine to handle housekeeping tasks.
4	MBOX_FULL	R only		This is a read-only status register bit. If this bit is '0', it indicates no data is available in the mail box. If it is '1', it indicates new data is available in the mail box.
			0 *	No data is available for this master.
			1	Mailbox contains data for this master from the other master.
3	MBOX_EMPTY	R only		This is a read-only status register bit. If this bit is '0', it indicates other master mailbox is full, and this master cannot send more data to the other master mailbox. If it is '1', it

Bit	Symbol	Access	Value	Description
				indicates other master is empty and this master can send data to the other master mailbox.
			0 *	Other master mailbox is full; wait until the other master reads data.
			1	Other master mailbox is empty. Other master has read previous data and it is permitted to write new data.
2	BUS_HUNG	R only		This is a read-only status register bit. If this register bit is '0', it indicates the bus is in normal condition. If this bit is '1', it indicates the bus is hung. The hung bus means the SDA signal is LOW and the SCL signal does not toggle for more than 700 ms or SCL is LOW for 700 ms.
			0 *	Normal operation.
			1	Downstream bus hung; when the SDA signal is LOW and the SCL signal does not toggle for more than 700 ms or SCL is LOW for 700 ms.
1	BUS_INIT_FAIL	R only		This is a read-only status register bit. If this register bit is '0', it indicates the bus initialization function has passed. The downstream bus is in idle mode (SCL and SDA are HIGH). If this register bit is '1', it indicates the bus initialization function has failed. The SDA signal could be stuck LOW.
			0 *	Normal operation.
			1	Bus initialization has failed. SDA still LOW, the downstream bus cannot recover.
0	OTHER_LOCK	R only		This is a status read-only register bit. Other master lock status indicates the ownership between the other master and the downstream bus. If this register bit is '1', the other master owns the downstream bus. If this register bit is '0', the other master does not own the downstream bus.
			0 *	The other master does not have a lock on the downstream bus.
			1	The other master has a lock on the downstream bus.

(1) POR = 00h.
(2) Legend: * default value

Register 3: Reserve Time Register ([B2:B0] = 011b)

Reserve time refers to the period (1.5 ms to 383 ms) during which a master maintains control of the downstream bus without interruption. When LOCK_GRANT is '1', writes to the RT register are permitted but do not take effect. If the master writes 00h to the RT register before requesting the downstream bus, it permanently retains bus ownership until clearing the LOCK_REQ bit to release control.

When IDLE_TIMER_DIS = 1 and Reserve Time are enabled, the master must wait an additional 150 ms after the Reserve Time expires before releasing control of the bus.

Table 9. RT - Reserve Time Register (Pointer Address 03h) Bit Description

Bit	Symbol	Access	Value	Description
7 to 0	RES_TIME[7:0]	R/W		Reserve timer. Changes during LOCK_GRANT = 1 will have no effect.
			00h *	Disable timer or reserve without time limited.
			01h	1.5 ms
			02h	3 ms
			03h	4.5 ms
			...	...
			FFh	383 ms

(1) POR = 00h.
(2) Legend: * default value

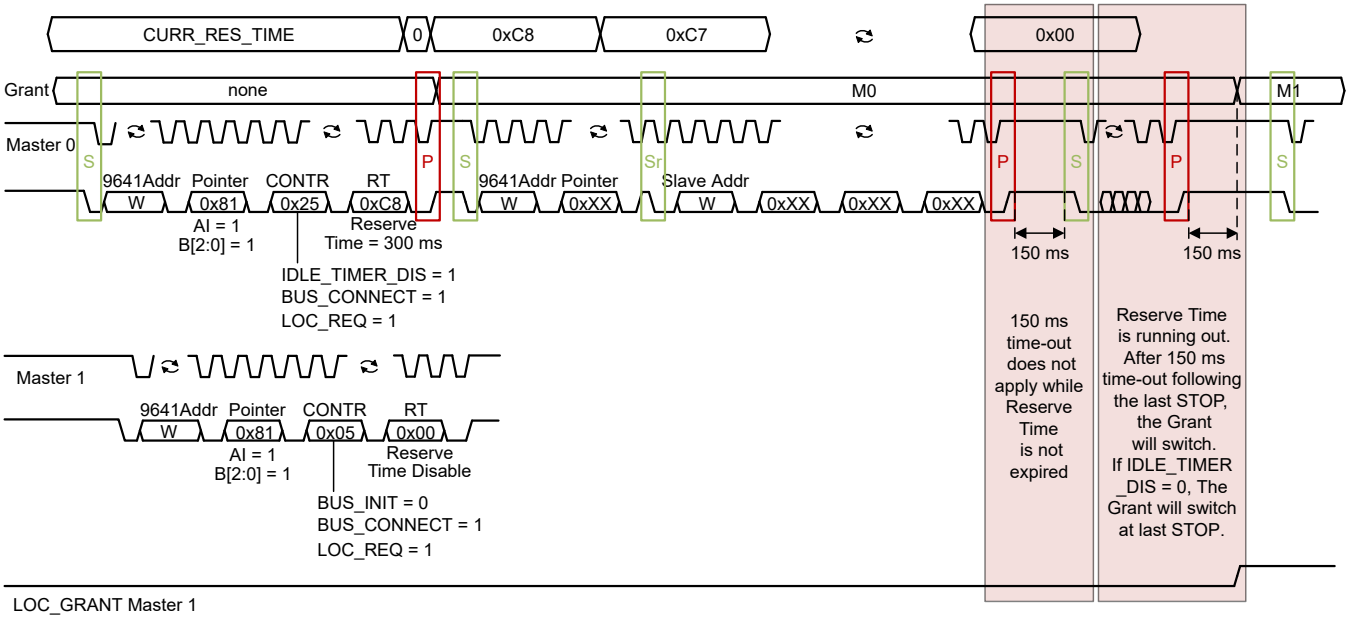


Figure 10. Request Downstream with Reserve Time and IDLE_TIMER_DIS=1

Register 4: Interrupt Status Register ([B2:B0] = 100b)

The TPT29641 supports seven interrupt types, with their status bits latched until cleared by writing‘1’ to the corresponding register.

Table 10. INT_STATUS - Interrupt Status Register (Pointer Address 04h) Bit Description

Bit	Symbol	Access	Value	Description
7	-			Reserved.

Bit	Symbol	Access	Value	Description
6	BUS_HUNG_INT	R only		Indicates to both masters that the SDA signal is LOW and the SCL signal does not toggle for more than 700 ms or the SCL is LOW for 700 ms.
			0	No interrupt generated; normal operation.
			1	Interrupt generated; downstream bus cannot recover; when the SDA signal is LOW and the SCL signal does not toggle for more than 700 ms or the SCL is LOW for 700 ms.
5	MBOX_FULL_INT	R/W		Indicates the mailbox has new mail.
			0	No interrupt generated; mailbox is not full.
			1	Interrupt generated; mailbox is full.
4	MBOX_EMPTY_INT	R/W		Indicates the sent mail is empty, other master has read the mail.
			0	No interrupt generated; sent mail is not empty.
			1	Interrupt generated; mailbox is empty.
3	TEST_INT_INT	R/W		Indicates this master has sent an interrupt to itself.
			0	No interrupt generated; master has not set the TEST_INT bit in the STATUS register.
			1	Interrupt generated; master activates its interrupt pin via the TEST_INT bit in the STATUS register.
2	LOCK_GRANT_INT	R/W		Indicates the master has a lock (ownership) on the downstream bus.
			0	No interrupt generated; this master does not have a lock on the downstream bus.
			1	Interrupt generated; this master has a lock on the downstream bus.
1	BUS_LOST_INT	R/W		Indicates the master has involuntarily lost the ownership of the downstream bus.
			0	No interrupt generated; this master is controlling the downstream bus.
			1	Interrupt generated; this master has involuntarily lost the control of the downstream bus.
0	INT_IN_INT	R/W		Indicates that there is an interrupt from the downstream bus to both the granted and non-granted masters.
			0	No interrupt on interrupt input pin $\overline{\text{INT\_IN}}$.
			1	Interrupt on interrupt input pin $\overline{\text{INT\_IN}}$.

(1) POR = 00h.

Register 5: Interrupt Mask Register ([B2:B0] = 101b)

Table 11. INT_STATUS - Interrupt Status Register (Pointer Address 04h) Bit Description

Bit	Symbol	Access	Value	Description
7	-			Reserved.
6	BUS_HUNG_MSK	R/W	0	Enable output interrupt when BUS_HUNG function is set.
			1	Disable output interrupt when BUS_HUNG function is set.
5	MBOX_FULL_MSK	R/W	0	Enable output interrupt when MBOX_FULL function is set.
			1	Disable output interrupt when MBOX_FULL function is set.
4	MBOX_EMPTY	R/W	0	Enable output interrupt when MBOX_EMPTY function is set.
			1	Disable output interrupt when MBOX_EMPTY function is set.
3	TEST_INT_MSK	R/W	0	Enable output interrupt when TEST_INT function is set.
			1	Disable output interrupt when TEST_INT function is set.
2	LOCK_GRANT_MSK	R/W	0	Enable output interrupt when LOCK_GRANT function is set.
			1	Disable output interrupt when LOCK_GRANT function is set.
1	BUS_LOST_MSK	R/W	0	Enable output interrupt when BUS_LOST function is set.
			1	Disable output interrupt when BUS_LOST function is set.
0	INT_IN_MSK	R/W	0	Enable output interrupt when $\overline{\text{INT\_IN}}$ function is set.
			1	Disable output interrupt when $\overline{\text{INT\_IN}}$ function is set.

(1) POR = 7Fh.

Registers 6 and 7: MB Registers ([B2:B0] = 110b and 111b)

Table 12. SMB - Shared Mail Box Registers (Pointer Addresses 06h, 07h) Bit Description

Address	Bit	Symbol	Access	Description
06h	7 to 0	MB_LO[7:0]	R/W	Low 8 bits of the mail box.
07h	7 to 0	MB_HI[7:0]	R/W	High 8 bits of the mail box.

Operating Cycle of the Downstream Bus

Request the Downstream Bus

To request bus control, a master must configure its Control register (CONTR, address 01h) and optionally set the Reserve Time register (RT, address 03h). By asserting the LOCK_REQ bit and programming the RT[7:0] value, the master can acquire uninterrupted bus ownership for the RES_TIME duration.

While Master 0 is occupying the downstream bus, Master 1 can assert a bus request by setting the LOCK_REQ bit in the Control Register (CONTR) and configuring the Reserve Time Register (RT). Control of the bus is transferred to Master 1 once the RES_TIME period of Master 0 expires and the downstream bus becomes idle.

If the Reserve Time is set to 0, the timer counter is disabled. In this state, the master indefinitely retains bus control until it gives up ownership.

Acquire the Downstream Bus

After writing to the LOCK_REQ bit, the master must confirm bus ownership through either:

- Polling the LOCK_GRANT bit in the Control register (CONTR);
- Waiting an interrupt signal ($\overline{\text{INTn}}$ pin) if the LOCK_GRANT_MSK bit is enabled in the INT_MSK register.

When LOCK_GRANT bit is one, this master acquires ownership of the downstream bus. After that, the master must set the BUS_CONNECT bit to 1 to establish communication with downstream slave devices.

Give up the Downstream Bus

The RES_TIME counter initiates a countdown after the LOCK_GRANT bit is set to 1. When RES_TIME reaches zero and the bus is idle (with SCL_SLAVE and SDA_SLAVE both HIGH following a STOP condition), the LOCK_GRANT bit of the master is cleared.

If a master requests the downstream bus with RES_TIME = 0, it must write 0 to the LOCK_REQ bit to manually give up its control.

Arbitration

Rules

1. If a master keeps its request active (LOCK_REQ = 1) after being granted, it will retain indefinite control of the bus.
   - If the idle timeout function is enabled, the bus disconnects only when both:
     — The reserve timer expires.
     — The bus remains idle for 150 ms.
2. If a master removes its request (LOCK_REQ = 0), its grant is immediately revoked.
   - If another master is requesting the bus (LOCK_REQ = 1), the grant is transferred to that device.
   - If no master is requesting the bus, the TPT29641 disconnects from all masters, and the bus enters the idle state.
3. If a master configures the reserve timer (RES_TIME) before being granted, the timer will automatically clear its request when it expires.
   - The timer supports a 1 ms to 383 ms window. When the timer expires, the master clears its request and follows Step 2.
   - If the bus remains idle for over 150 ms while the reserve timer has not expired, the grant of the master is maintained.
   - If the master actively clears its request while the reserve timer has not expired, the grant of the master is immediately revoked.
4. When two masters attempt to request the grant nearly simultaneously, arbitration proceeds as follows:

- The first master that sets its request bit (LOCK_REQ=1) in the control register is granted priority. It is independent of the START signal timing and the clock frequencies of masters. Even if a master is performing a burst write with an address rollover, it will be granted bus control when its request bit in the control register is set first.
- The grant of winning master becomes effective only after its current transaction is terminated with a STOP condition. A STOP condition must be issued before accessing downstream slaves. Re-START conditions are prohibited during bus requests.
- If both masters set LOCK_REQ at the same time(close enough that the logic cannot resolve request timing), the grant is assigned based on the Priority bit in the control register. For details, refer to Table 6.

5. A write operation to the control register for a REQUEST will always be acknowledged with an ACK.
   - The master must poll the control register or utilize interrupt mechanisms to determine whether the bus grant has been issued.

Disconnect Events

The disconnection of the master device is triggered by the following events, provided the conditions for grant removal and downstream bus disconnection (as defined in the preceding sections) are satisfied:

- Reserve timer expires after STOP condition (ideal scenario, the cleanest disconnection method).
- Bus idle for over 150 ms (non-ideal scenario).
- Writing '0' to the LOCK_REQ bit (active request release).

State machines

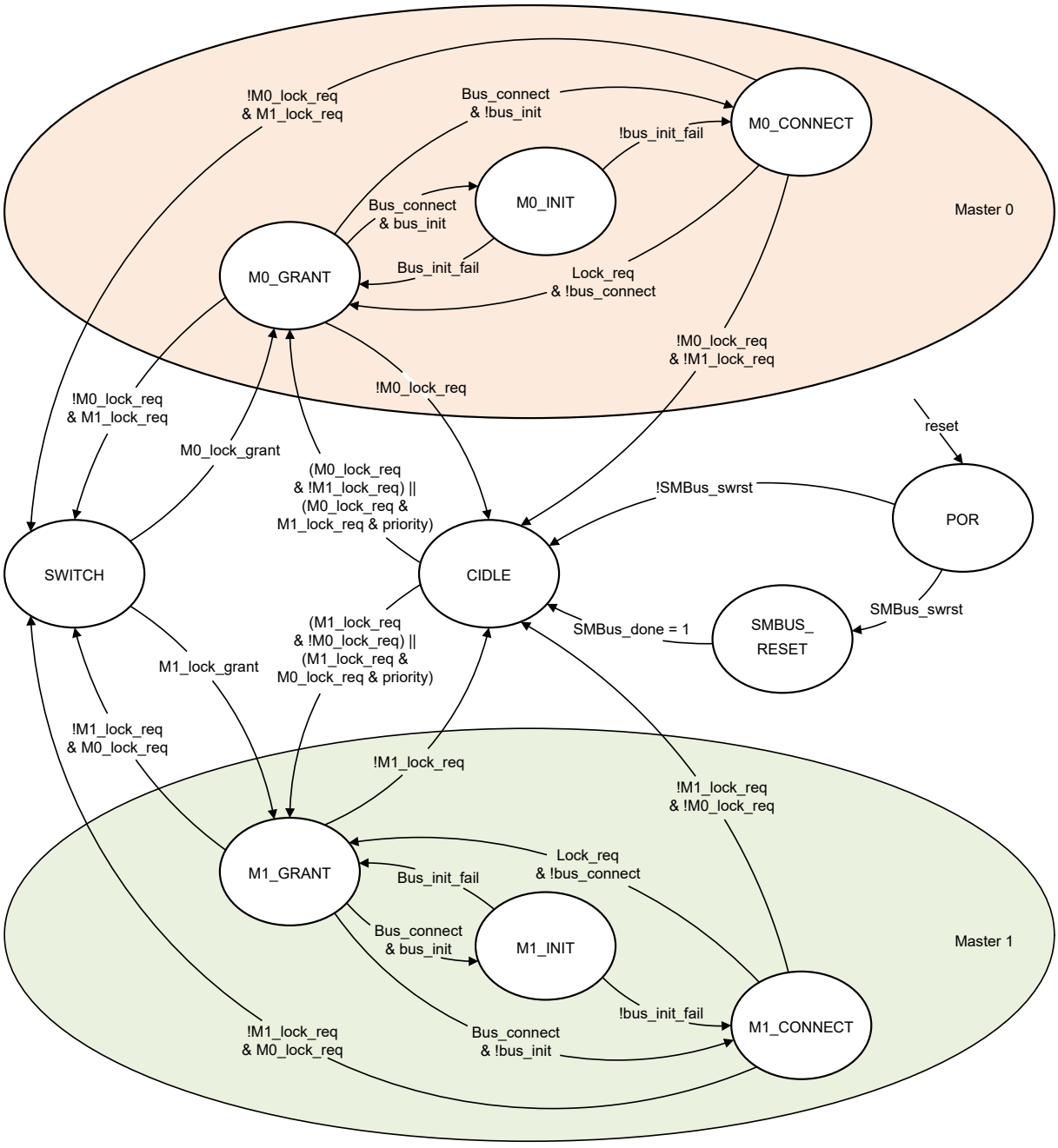


Figure 11. State Machine of Downstream Bus Ownership

Request Grant Examples

Master 0 initiates a START condition first, but Master 1 (operating at a higher clock frequency) sets the request bit (LOCK_REQ = 1) in the control register earlier, so Master 1wins the arbitration, as shown in Figure 12.

The arbitration result (LOCK_GRANT = 1) is applied only after the winning master issues a STOP condition. If the winning master continues writing to subsequent registers using auto-incrementing addresses, its bus control is delayed until the STOP condition is issued, and it is still deemed the arbitration winner.

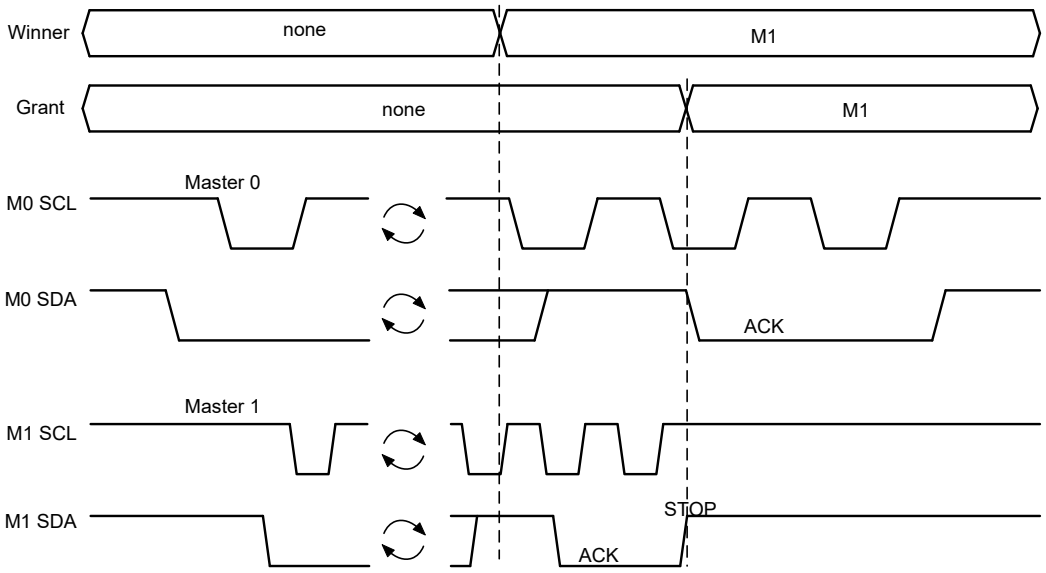


Figure 12. Request Grant Example

If both masters set LOCK_REQ at the same time(close enough that the logic cannot resolve request timing), the winner is determined by the PRIORITY bits in the control register, as shown in Figure 9.

Auto-increment

Auto-increment

Writing to each register requires the transmission of 3 bytes: the slave address, command byte, and data byte. By setting the AI bit (bit 8 of the command byte) to '1', the master can continuously write or read data with the slave auto-incrementing the register address. Upon reaching the last allowed register (pointer value 111b), the pointer rolls over to 000b.

For example, when writing 8 data bytes with the command byte 0x84, Data Byte 1 is written to register 0x4, Data Byte 2 is written to register 0x5, Data Byte 3 is written to register 0x6, Data Byte 4 is written to register 0x7, Data Byte 5 is written to register 0x0 (address rollover), Data Byte 6 is written to register 0x1, Data Byte 7 is written to register 0x2, and Data Byte 8 is written to register 0x3. For writes to read-only registers, their values remain unchanged. The read operation follows a Similar flow.

The master terminates the auto-increment write operation by sending a STOP bit after the final ACK from the slave. To continue reading data from subsequent registers, the master sends an ACK after each byte. To end the auto-increment read operation, the master sends a NACK followed by a STOP bit after the final byte.

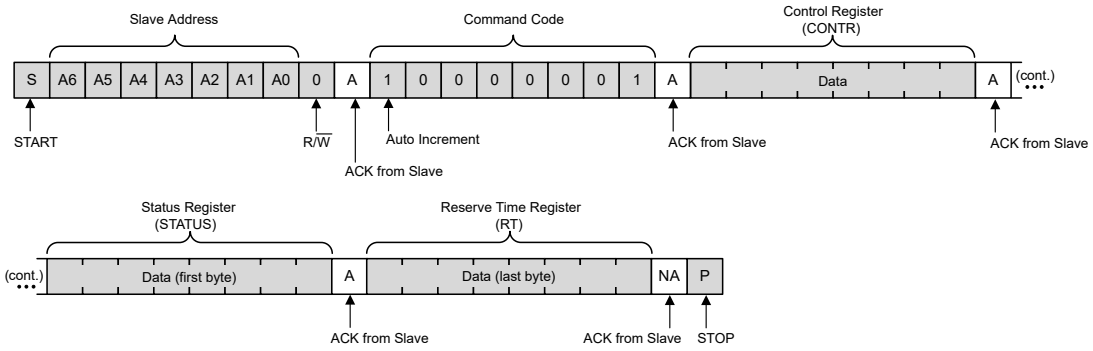


Figure 13. Write Registers Using the Auto-Increment (AI) Bit

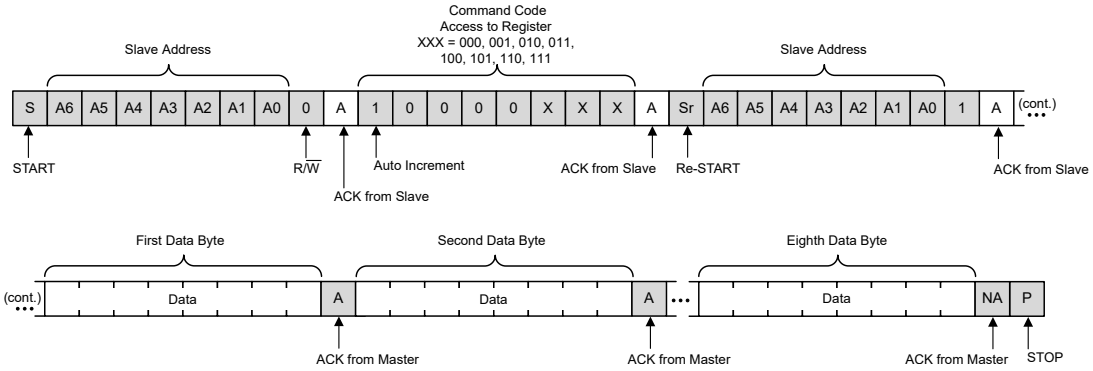


Figure 14. Read Registers Using the Auto-Increment (AI) Bit

Table 13. Read/Write the Registers Using Auto-Increment

Command Code	First Data Byte	Second Data Byte	Third Data Byte	Fourth Data Byte	Fifth Data Byte	Sixth Data Byte	Seventh Data Byte	Eighth Data Byte
10000000	ID	CONTR	STATUS	RT	INT_ STATUS	INT_MASK	MB_LO	MB_HI
10000001	CONTR	STATUS	RT	INT_ STATUS	INT_MASK	MB_LO	MB_HI	ID
10000010	STATUS	RT	INT_ STATUS	INT_MASK	MB_LO	MB_HI	ID	CONTR
10000011	RT	INT_ STATUS	INT_MASK	MB_LO	MB_HI	ID	CONTR	STATUS
10000100	INT_ STATUS	INT_MASK	MB_LO	MB_HI	ID	CONTR	STATUS	RT
10000101	INT_MASK	MB_LO	MB_HI	ID	CONTR	STATUS	RT	INT_ STATUS
10000110	MB_LO	MB_HI	ID	CONTR	STATUS	RT	INT_ STATUS	INT_MASK
10000111	MB_HI	ID	CONTR	STATUS	RT	INT_ STATUS	INT_MASK	MB_LO

General Call Software Reset

The Software Reset Call allows all devices on the I²C bus to be reset to their power-up state values via a specific I²C command sequence. This operation requires that the I²C bus is functional and no device is causing the bus to hang. The software reset procedure is as follows:

1. The master issues a START condition.
2. The master transmits the reserved General Call address '0000 000' with the R/$\overline{W}$ bit set to '0'.
3. The device acknowledges (ACK) only if the R/$\overline{W}$ bit is '0'. If the R/$\overline{W}$ bit is '1', no acknowledgment is returned.
4. The master sends one data byte with the value 06h. If the byte is 06h, the device responds with an ACK. If the byte is not 06h or if more than one byte is sent, the device returns a NACK and aborts the software reset operation.
5. The master issues a STOP condition, triggering the device to reset to its default state (power-up values). If the master sends a Re-START instead, the reset is not executed.

If the device returns a NACK at any stage, the master must interpret this as a 'Software Reset Abort'.

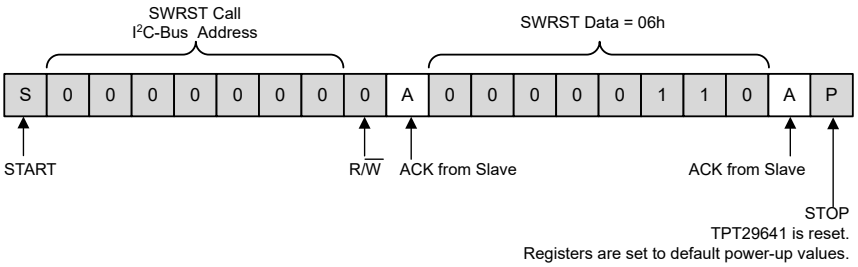


Figure 15. Software Reset Sequence

Device ID (TPT29641 ID field)

The Device ID field is a 3-byte (24-bit) read-only field containing the following information:

- First 12 bits: Manufacturer identifier (uniquely assigned per manufacturer).
- Next 9 bits: Part identification (defined by the manufacturer).
- Last 3 bits: Die revision (assigned by the manufacturer).

Table 14. TPT29641 ID field

Byte 3								Byte 2								Byte 1							
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0
Bits [23:11]								Bits [10:3]								Bits [2:0]							
Manufacturer ID								Part ID								Revision							

The process for reading the device ID field is as follows:

1. The master issues a START condition.
2. The master transmits the reserved Device ID address '1111 100' with the R/$\overline{W}$ bit set to '0'.
3. The master sends the slave address of the target device to be identified. The LSB of the address is a "Don't care" value, but only the target slave responds with an ACK.
4. The master issues a Re-START command. Using a STOP followed by a START will reset the slave's state machine, causing the Device ID read to fail.

5. The master retransmits the reserved Device ID address '1111 100' with the R/$\overline{W}$ bit set to '1'.
6. Read the 3-Byte Device ID.
7. The master ends the read sequence by sending a NACK after the final byte, followed by a STOP command. If the master continues to send ACK after the third byte, the TPT29641 cycles back to the first byte and repeats the Device ID sequence until a NACK is detected. The reading of the Device ID can also be stopped after any byte by sending a NACK command.

Shared Mailbox

The Shared Mailbox consists of two 8-bit bidirectional mailboxes for communication between two masters. Each master has the MB_HI register and MB_LO register, as shown in Figure 7. There are two status flags to indicate the mailbox state.

- MBOX_FULL: Indicates that there is unread data in the local mailbox received from the other master.
- MBOX_EMPTY: Indicates that the mailbox of the other master is empty and ready to receive new data.

Mailbox Data Write Procedure

1. The master must check the MBOX_EMPTY status bit before writing:
   - MBOX_EMPTY = 0: The mailbox contains unread data. Writing is prohibited to avoid data loss/corruption.
   - MBOX_EMPTY = 1: The mailbox is ready to accept new data.
2. The master must write the full 16-bit data, starting with the MB_LO (low-byte) register followed by the MB_HI (high-byte) register.
   - Invalid Operation: If written in reverse order (MB_HI first, MB_LO second), the MBOX_FULL bit of the receiving master will not be set to 1.
3. After successful writing:
   - The MBOX_EMPTY bit of the sending master is cleared to '0', indicating the mailbox is occupied.
   - The MBOX_FULL bit of the receiving master is set to '1', signaling new data is available for reading.

Mailbox Data Read Procedure

1. When the master's MBOX_FULL bit is set to '1', it indicates that data has been written by the other master and is ready for reading.
2. The master can read the MB_LO and MB_HI registers in any order. The MBOX_FULL status bit is cleared to '0' only after both registers have been read.
3. After successful reading:
   - The MBOX_EMPTY bit of the sending master is set to '1', indicating its mailbox is ready to accept new data.
   - The MBOX_FULL bit of the receiving master is cleared to '0', signifying no new data is ready for reading.

Note: When a master writes the mailbox registers, the data is sent to the mailbox of the other master. When a master reads the mailbox registers, it accesses only its own mailbox and cannot read back data it has written itself.

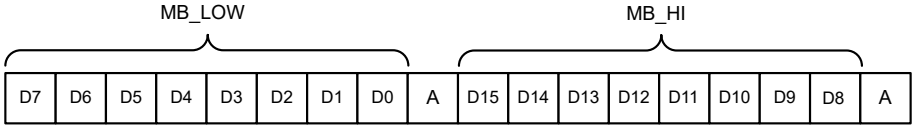


Figure 16. Shared Mailbox Byte Arrangement

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

A typical application is shown in Figure 17.

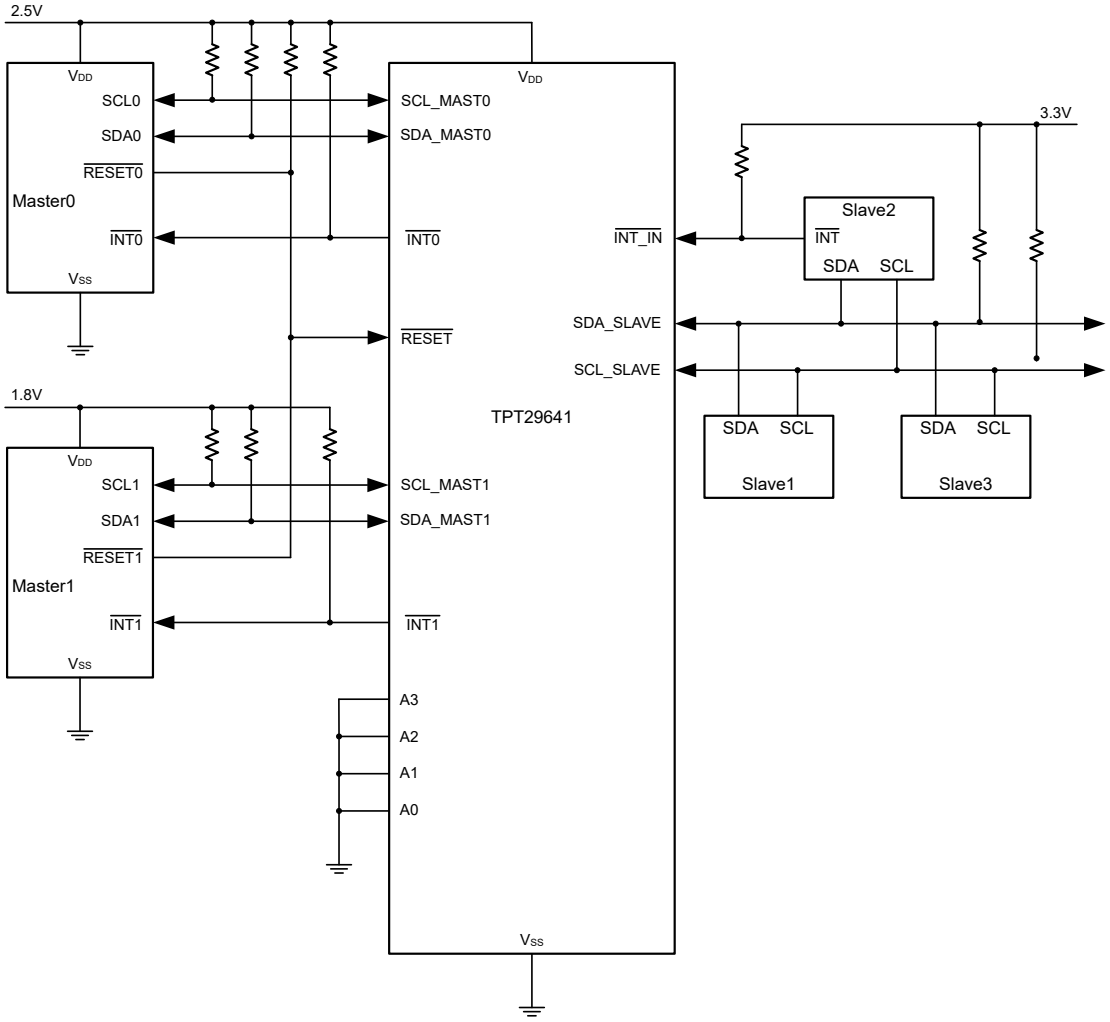


Figure 17. Typical Application Circuit

Arbitration Application

The TPT29641 is a 2-to-1 I²C bus master arbiter designed for dual master devices sharing the same downstream slave devices. The arbitration process requires no pre-configuration or software intervention, being entirely automated by hardware. Any master can request control of the downstream bus at any time, and the TPT29641 will automatically switch control upon meeting conditions. Operations between masters do not interfere with each other, ensuring ongoing

transmissions are neither interrupted nor overwritten by the other master. The TPT29641 switches master control permissions only when the downstream bus is idle, preventing data corruption. If the downstream bus hangs, the TPT29641 supports multiple recovery methods, such as smart bus initialization, SMBus timeout, and remote toggling of SCL and SDA.

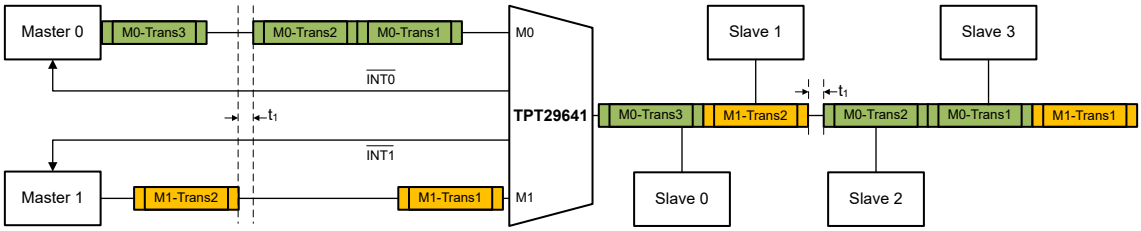


Figure 18. Arbitration Application

Bus Initialization/Recovery Application

When downstream I²C slave devices without a hardware reset pin experience a bus hang for over 700 ms, the TPT29641 can automatically isolate it from the master, preventing fault propagation to the entire bus. After isolation, the TPT9641 resumes normal access to other slave devices. Before reconnecting the downstream bus, the master can command the TPT29641 to reset the downstream bus by sending nine SCL clock pulses and STOP condition.

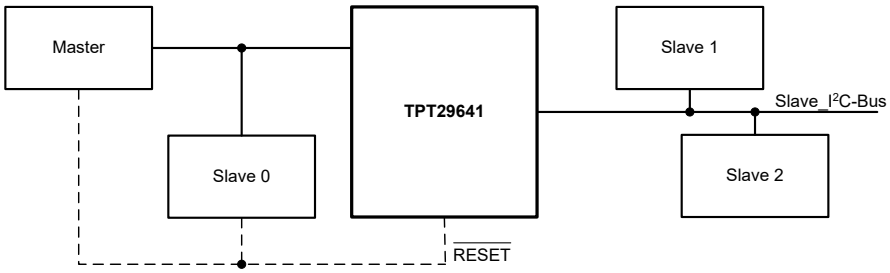
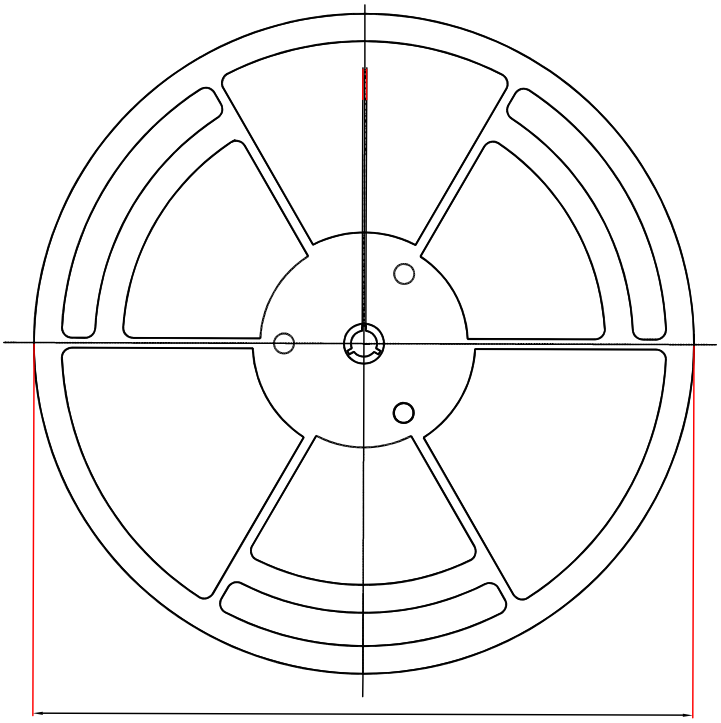
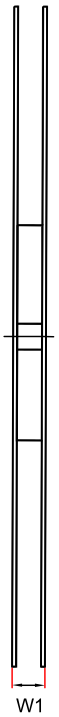
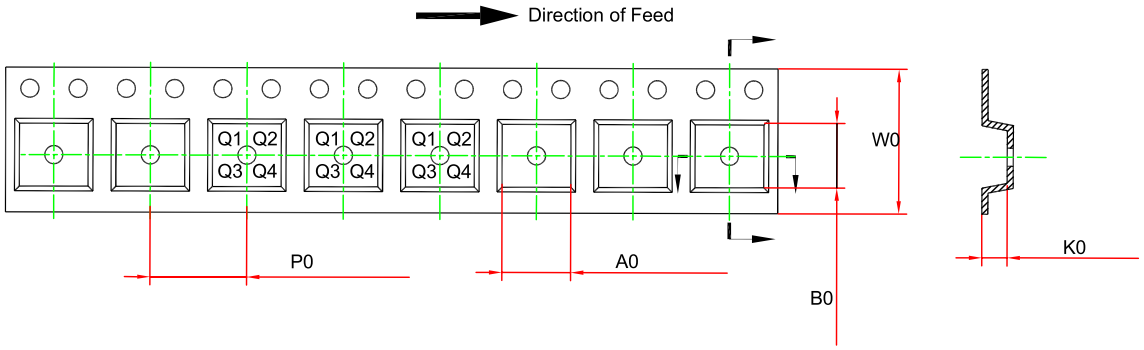


Figure 19. Bus Initialization/Recovery Application

Tape and Reel Information





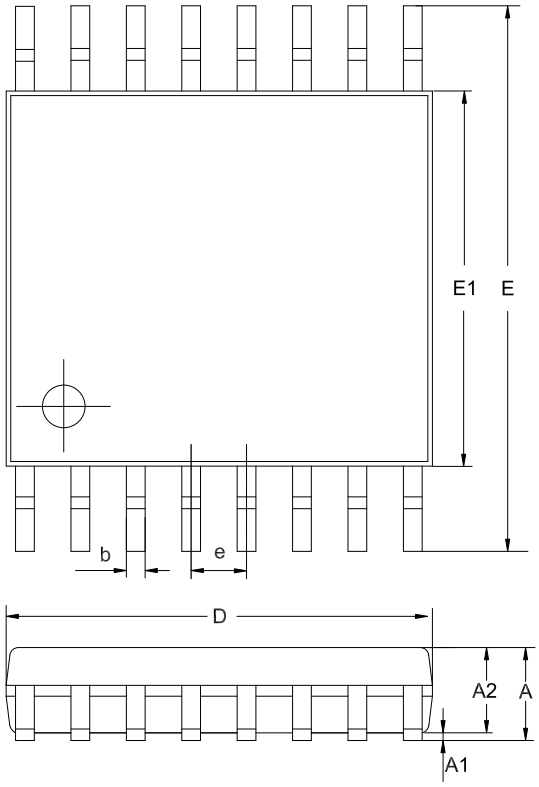


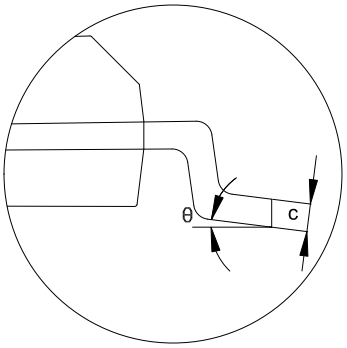
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT29641-QFNR	QFN3X3-16	330	17.6	3.3	3.3	1.1	8	12	Q1
TPT29641-TS3R	TSSOP-16	330	17.6	6.8	5.5	1.5	8	12	Q1

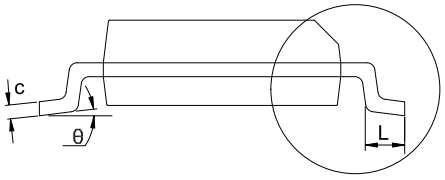
Package Outline Dimensions

TSSOP16

Package Outline Dimensions TS3(TSSOP-16-A)







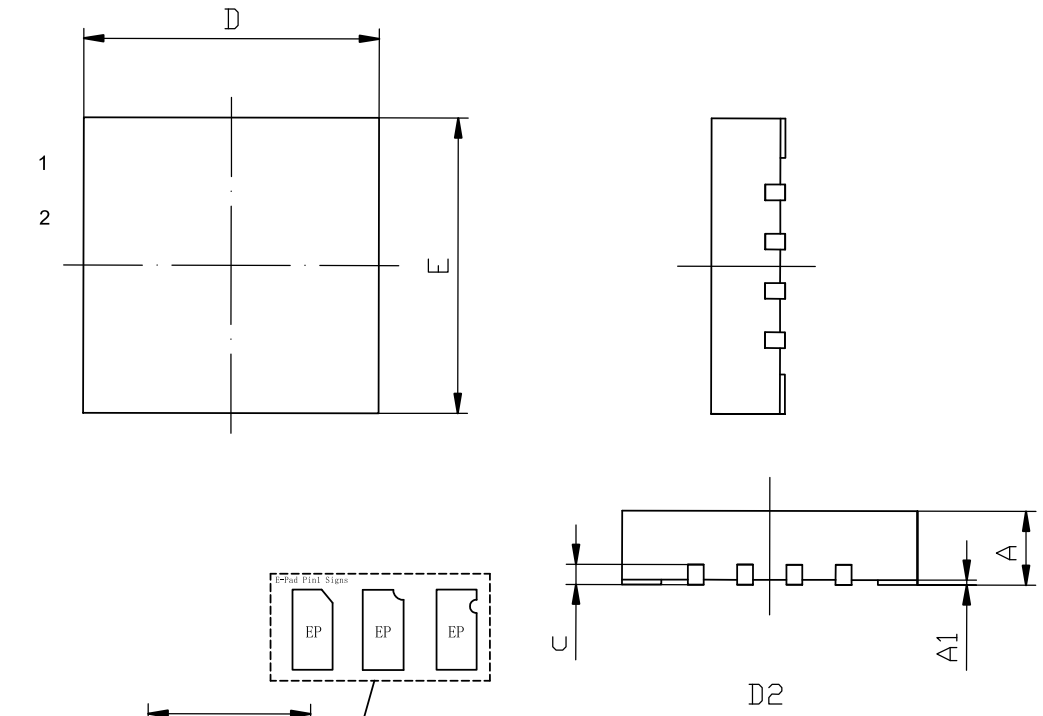
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

QFN3X3-16

Package Outline Dimensions QFN(QFN3X3-16-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
b1	0.160 REF		0.006 REF	
c	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D2	1.550	1.750	0.061	0.069
E	2.900	3.100	0.114	0.122
E2	1.550	1.750	0.061	0.069
e	0.500 BSC		0.020 BSC	
L	0.250	0.450	0.010	0.018
h	0.200	0.300	0.008	0.012

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order number	Operating Temperature Range	Package	Marking	MSL	Transport Media, Quantity	Eco Plan
TPT29641-TS3R	−40 to 85°C	TSSOP16	T29641	MSL3	Tape and Reel, 3000	Green
TPT29641-QFNR	−40 to 85°C	QFN3X3-16	T29641	MSL3	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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