Dual Channel Bidirectional I²C Bus Level Shift and Repeater

Features

- Dual Channel Level Shift and Repeater for SDA/SCL Lines in I²C Applications and SMBus Compatible
- Support Multi-mode: Standard-mode (SM), Fast-mode (FM), and Fast-mode Plus (FM+)
- Open-Drain I²C Input/Output
- Latching Free Operation
- Allows Voltage-Level Translation between
  - V_{REF1} Range: 0.85 V to 5.5 V
  - V_{REF2} Range: 2.25 V to 5.5 V
- 5 V Tolerant I²C-bus and Enable Pins
- High-impedance SCL1, SDA1, SCL2, and SDA2 Pins for EN = LOW
- Support Low-level Output Current up to 30 mA
- ESD Protection:
  - 7000-V Human-Body Model
  - 1500-V Charged-Device Model

Applications

- I²C, SMBus, PMBus, MDIO, UART, Low-Speed SDIO, GPIO, and Other Two-Signal Interfaces
- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Description

The TPT29617X-S device is a dual channel I²C level shift and repeater, functions with an enable (EN) input and can work within the V_{REF1} range from 0.85 V to 5.5 V and the V_{REF2} range from 2.25 V to 5.5 V.

The SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, which allows bidirectional data flow between ports. If EN is low, the translator switch is off, and a high-impedance state exists between ports to isolate both sides.

Dual channel, bidirectional buffer isolates capacitance and allows 540 pF on either side of the device at 1 MHz and up to 4000 pF at lower speeds.

The TPT29617X-S is available in the MSOP8 package and is characterized from −40°C to +125°C.

Functional Block Diagram

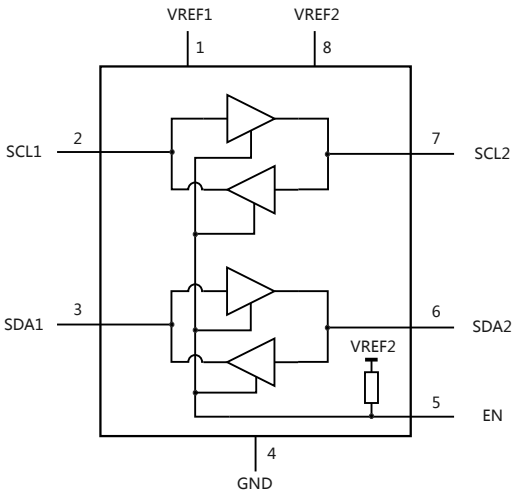


Table of Contents

Revision History

Date	Revision	Notes
2024-06-18	Rev.A.0	Released version

Pin Configuration and Functions

TPT29617X-VS1R-S
MSOP8 Package
Top View

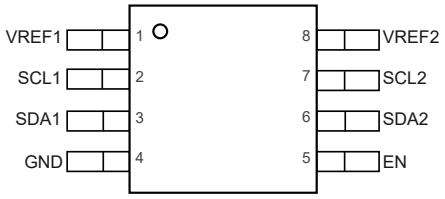


Table 1. Pin Functions: TPT29617X-S

Pin		I/O	Description
No.	Name		
1	VREF1	I	Side-1 supply voltage (0.85 V to 5.5 V)
2	SCL1	I/O	I²C SCL line, side-1. Connect to VREF1 through a pull-up resistor.
3	SDA1	I/O	I²C SDA line, side-1. Connect to VREF1 through a pull-up resistor.
4	GND	I	Supply ground
5	EN	I	Active-high repeater enable input, internal pull high to VREF2
6	SDA2	I/O	I²C SDA line, side-2. Connect to VREF2 through a pull-up resistor.
7	SCL2	I/O	I²C SCL line, side-2. Connect to VREF2 through a pull-up resistor.
8	VREF2	I	Side-2 and device supply voltage (2.25 V to 5.5 V)

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{REF1}	DC Reference Voltage Range	−0.5	7	V
V_{REF2}	DC Reference bias Voltage Range	−0.5	7	V
V_I	Input Voltage Range	−0.5	7	V
$V_{I/O}$	Input/output Voltage Range	−0.5	7	V
I_{IK}	Input Clamp Current, $V_I < 0$		−50	mA
I_{OK}	Output Clamp Current, $V_{I/O} < 0$		−50	mA
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
$V_{I/O}$	Input/output Voltage, SCL1, SDA1, SCL2, SDA2	0	5.5	V
V_{REF1}	Reference Voltage	0.85	5.5	V
V_{REF2}	Reference Voltage	2.25	5.5	V
I_{input}	Input Clamp Current	0	50	mA
I_{output}	Output Clamp Current	0	50	mA
T_A	Operating Ambient Temperature	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP8	180	72	°C/W

Electrical Characteristics

All test conditions: V_{REF1} = 0.85 V to 5.5 V, V_{REF2} = 2.25 V to 5.5 V, GND = 0 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter			Conditions		Min	Typ	Max	Unit
Supply Voltage and Current								
V_{IK}	Input Clamp Voltage		I_I = −18 mA, V_{CC} = 2.25 V to 5.5 V		−1.2		−0.3	V
V_{OL}	Low-level Output Voltage	SDA1, SCL1	I_{OL} = 13 mA, V_{REF1} = 0.85 V to 5.5 V			0.1	0.2	V
		SDA2, SCL2	I_{OL} =150 µA or 13 mA, V_{ILA} = 0 V, V_{REF2} = 2.25 V to 5.5 V			0.5	0.62	
V_{IH}	High-level Input Voltage	SDA1, SCL1	V_{REF1} = 0.85 V to 5.5 V		0.7 x V_{REF1}		5.5	V
		SDA2, SCL2	V_{REF2} = 2.25 V to 5.5 V		0.7 x V_{REF2}		5.5	
		EN	V_{REF2} = 2.25 V to 5.5 V		0.72 x V_{REF2}		5.5	
V_{IL}	Low-level Input Voltage	SDA1, SCL1	V_{REF1} = 0.85 V to 5.5 V				0.3 x V_{REF1}	V
		SDA2, SCL2	V_{REF2} = 2.25 V to 5.5 V				0.4	
		EN	V_{REF2} = 2.25 V to 5.5 V				0.3 x V_{REF2}	
V_{OL}−V_{IL}	Difference between Low-level Output and Low-level Input Voltage		V_{OL} at I_{OL} = 1 mA;			90	140	mV
I_{CC1}	Quiescent Supply Current for V_{REF1}		Both channels low, SDA1 = SCL1 = GND and SDA2 = SCL2 = open, or SDA1 = SCL1 = open and SDA2 = SCL2 = GND	V_{REF1} = 0.85 V		1.5	5	µA
				V_{REF1} = 5.5 V		10	20	
I_{CC2}	Quiescent Supply Current		Output Low Level	V_{REF2} = 2.25 V to 5.5 V		9	15	mA
			Output High Level			1.2	5	
I_I	Input Leakage Current	SDA2, SCL2	V_I = V_{REF2}	V_{REFx} = 2.25 V to 5.5 V	–1		+1	µA
			V_I = 0.2 V, EN = 0		–1		+1	
		SDA1, SCL1	V_I = V_{REF1}		–1		+1	
			V_I = 0.2 V		–1		+1	
		EN	V_I = V_{REF2}		–1		+1	
			V_I = 0.2 V		–18	–7		
C_I	Input Capacitance (1)	SCL1, SCL2	V_I = 3 V or 0 V, V_{CC} = 3.3 V or 0 V			7		pF
		EN	V_I = 3 V or 0 V, V_{CC} = 3.3 V			5		
C_{IO}	Input/output Capacitance (1)	SDA1, SDA2	V_I = 3 V or 0 V, V_{CC} = 3.3 V			10		pF

(1) Test data based on bench tests and design simulation; NOT test in production.

AC Timing Requirements

All test conditions: V_{REF1} = 0.85 V to 5.5 V, V_{REF2} = 2.25 V to 5.5 V, GND = 0 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter			From (input)	To (output)	Conditions	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay		SDA2, SCL2	SDA1, SCL1			80	150	ns
			SDA1, SCL1	SDA2, SCL2	V_{REF2} = 2.25 to 5.5 V		85	150	ns
t_{PHL}	Propagation Delay		SDA2, SCL2	SDA1, SCL1			55	100	ns
			SDA1, SCL1	SDA2, SCL2			90	150	ns
t_{TLH}	Transition Time	2 side	30% Level	70% Level			90	150	ns
		1 side					75	100	ns
t_{THL}	Transition Time	2 side	70% Level	30% Level			10	30	ns
		1 side					10	30	
t_{en}	Setup Time, EN high before Start condition							100	ns
t_{dis}	Disable Time							100	ns

Typical Performance Characteristics

All test conditions: V_{REF1} = 0.9 V, V_{REF2} = 2.25 V, unless otherwise noted.

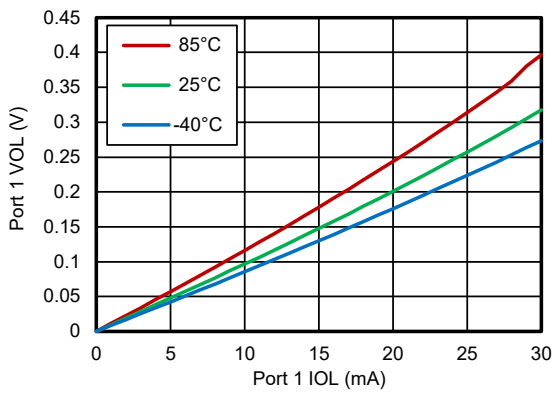


Figure 1. Port 1 VOL vs. IOL

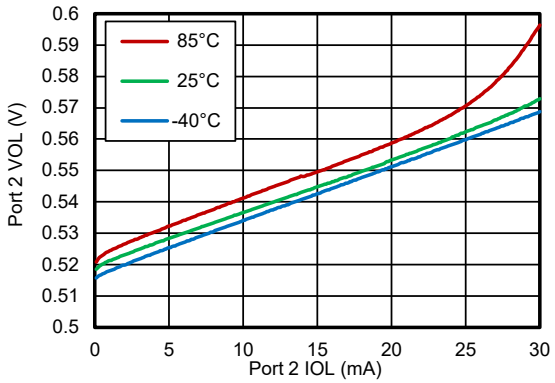
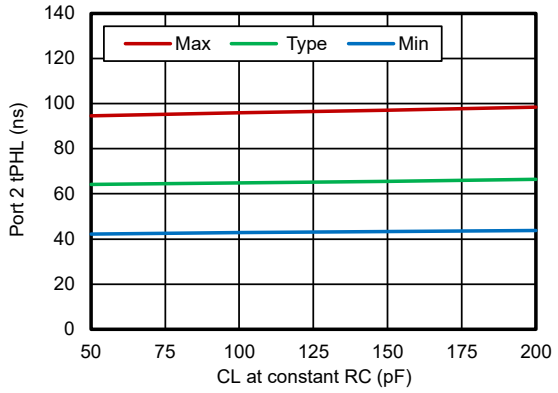


Figure 2. Port 2 VOL vs. IOL



VREF1 = 0.95 V, VREF2 = 2.5 V, RC = 67.5 ns

Figure 3. Port 2 tPHL vs. CL

Parameter Measurement Waveforms

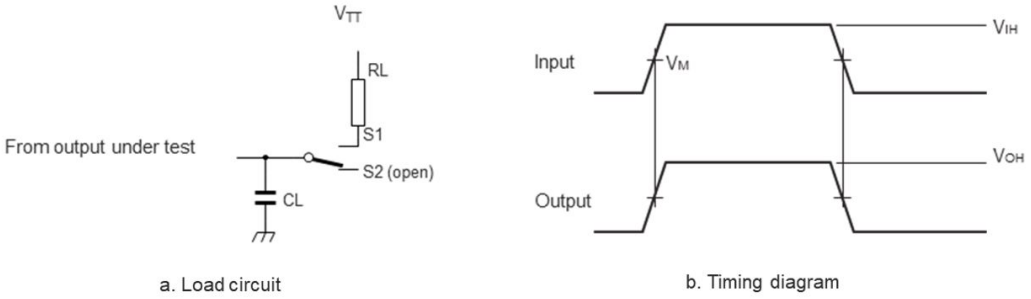


Figure 4. Load Circuit for Outputs

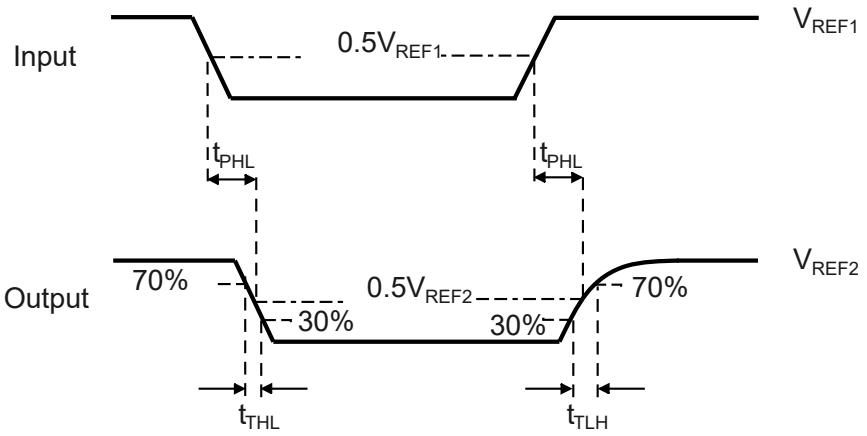


Figure 5. Propagation Delay and Transition Times, side1 to side2

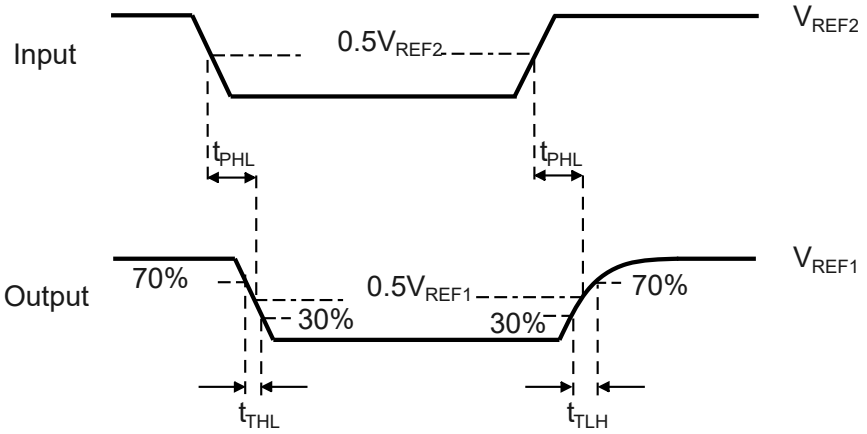


Figure 6. Propagation Delay and Transition Times, side2 to side1

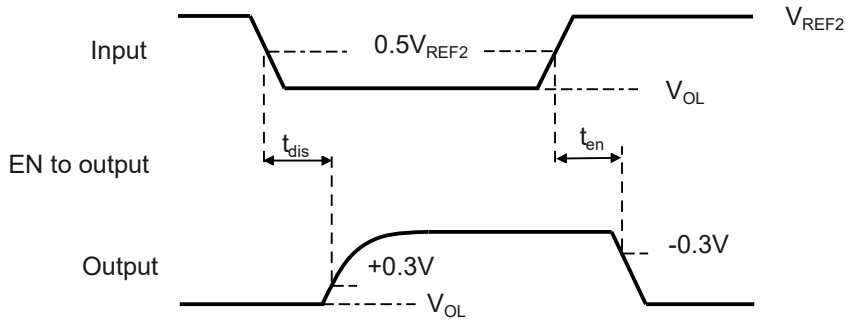


Figure 7. Enable and Disable Times

Detailed Description

Overview

The TPT29617X-S is a dual channel level shift and repeater for SDA/SCL Lines in I²C Applications and is SMBus Compatible, which supports I²C bus or SMBus translation down to V_{REF1} as 0.85 V with normal system performance. The TPT29617X-S builds in two bidirectional open-drain buffers specifically designed to support up/down-translation between the low voltage (down to 0.85 V) and a 2.5 V, 3.3 V or 5 V I²C bus or SMBus. All inputs and I/Os are tolerant to 5.5 V level.

The TPT29617X-S includes a power-up circuit that keeps the output drivers turned off until V_{REF2} is above 2.25 V and after the internal reference circuits have settled ~400 µs, and the V_{REF1} is above 0.85 V. V_{REF2} and V_{REF1} can be applied in any sequence at power-up. After power-up and with the enable (EN) HIGH, a LOW level on port-1 (< 0.3*VREF1) turns the corresponding port-2 driver (SDA or SCL) on and drives port-2 down to ~0.55 V. When port-1 rises above 0.3*V_{REF1}, the port-2 pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port-2 falls first and goes below 0.4 V, the port-1 driver is turned on and port-1 pulls down to ~0 V. The port-1 pull-down is not enabled unless the port-2 voltage goes below 0.4 V. If the port-2 low voltage goes below 0.4 V, the port-2 pull-down driver is enabled and port-2 is only able to rise to 0.55 V until port-1 rises above 0.3*V_{REF1}, then port-2 continues to rise and is pulled up by the external pull-up resistor. The V_{REF1} is only used to provide the 0.35*V_{REF1} reference to the port-1 input comparators and is for the power good detect circuit.

Functional Block Diagram

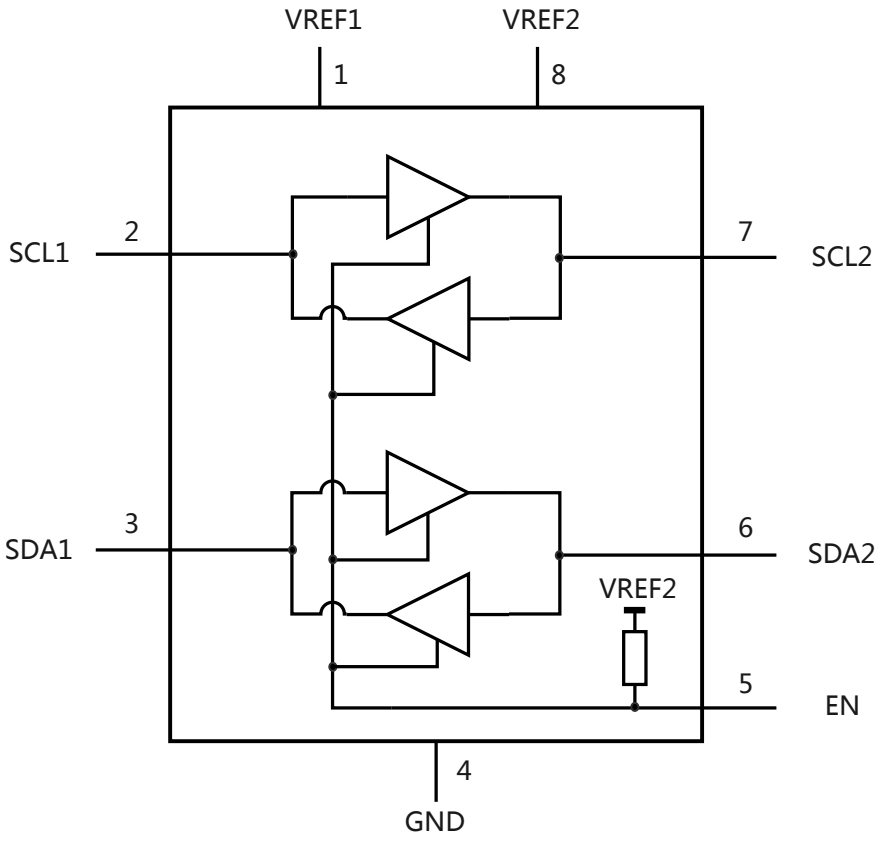


Figure 8. Functional Block Diagram

Feature Description

Enable (EN)

The EN pin is active HIGH with thresholds referenced to V_{REF2} and an internal pull-up to V_{REF2} that maintains the device active unless the user selects to disable the TPT29617X-S to isolate a badly behaved slave on power-up until the system power-up reset. It should never change states during an I²C-bus operation because disabling during a bus operation hangs the bus and enabling part way through a bus cycle confuses the I²C-bus parts being enabled. The enable does not switch the internal reference circuits, so the ~400 µs delay can only been seen when V_{REF2} comes up.

The EN pin only changes states when the global bus and the repeater port are in an idle state to prevent system failures.

Table 2. Device Function Table

Input EN (1)	Translator Function
H	SCL1 = SCL2, SDA1 = SDA2
L	Disconnect

(1) The SCL switch conducts if EN is ≥ 1 V higher than SCL1 or SCL2. The same is true of SDA.
(2) EN = Floating, or the GPIO goes Hi-z which controls the EN from the I²C master, and the TPT29617X-S status refers to EN = H.

Latching Free Operation

The output on the port 2 internal buffer is set at the pull-down LOW as 0.55 V, while the input threshold of the internal buffer is set at about 90 mV lower (around 0.45 V). When port 2 I/O is driven LOW internally, the LOW is not recognized as a Low by the input. This prevents latching conditions from occurring. The output pull-down on port 1 drives a hard Low and the input level is set at 0.35VCC (port 1) to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.85 V.

I²C-bus Systems

As the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I²C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part is designed to work with Standard mode, Fast-mode, and Fast-mode Plus I²C-bus devices in addition to SMBus devices. Standard mode and Fast-mode I²C-bus devices only specify a 3-mA output drive; this limits the termination current to 3 mA in a generic I2C-bus system where Standard-mode devices, Fast-mode devices, and multiple masters are possible. When only Fast-mode Plus devices are used with 20 mA at 5 V drive strength, then lower-value pull-up resistors can be used. The side-2 RC should not be less than 67.5 ns because shorter RCs increase the turnaround bounce when the side-2 transitions from being externally driven to pulled down by its offset buffer.

Please see the Application Information , the pull-up resistors value, which contains typical, star network, and series network circuits.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT29617X-S is a dual channel level shift and repeater for SDA/SCL Lines in I²C Applications and is SMBus Compatible, which supports I²C-bus or SMBus translation down to V_{REF1} as 0.85 V with normal system performance.

- I²C, SMBus, PMBus, MDIO, UART, Low-Speed SDIO, GPIO, and Other Two-Signal Interfaces
- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer handsets
- Industrial Automation

Typical Application

A typical application is shown in Figure 9. In this example, the system master is running on a 1.8-V I²C bus while the slave is connected to a 3.3-V bus. Both buses run at 1000 kHz. Master devices can be placed on either bus.

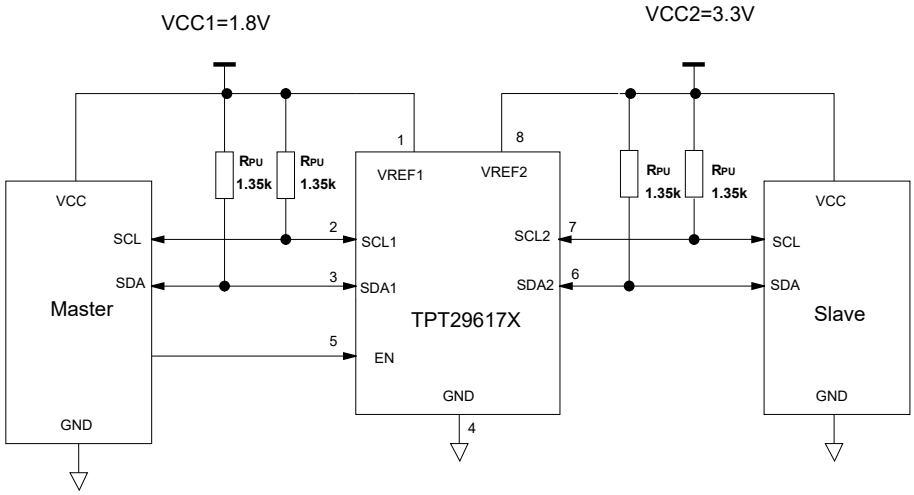


Figure 9. Typical Application Circuit

The TPT29617X-S is 5 V tolerant, so it does not require any additional circuitry to translate between 0.85 V to 5.5 V bus voltages and 2.25 V to 5.5 V bus voltages.

When port-1 of the TPT29617X-S is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below 0.3*V_{REF1} and causes the internal driver on port-2 to turn on, causing port-2 to pull down to about 0.5 V. When port-2 of the TPT29617X-S falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port-1 to turn on and pull the port-1 pin down to ground. To illustrate what can be seen in a typical application, refer to Figure 10 and Figure 11. If the bus master in Figure 9 were to write to the slave through the TPT29617X-S, waveforms shown in

Figure 10 is observed on port-1. This looks like a normal I²C-bus transmission except that the HIGH level may be as low as 0.85 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

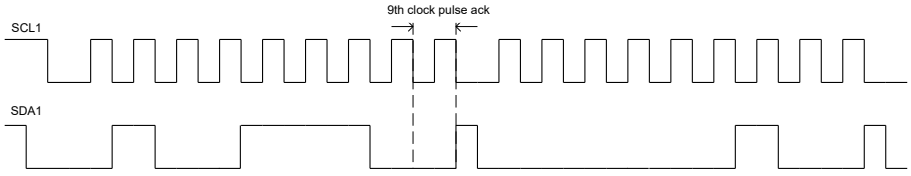


Figure 10. PORT-1 (0.85 V ~ 5.5 V) Waveform

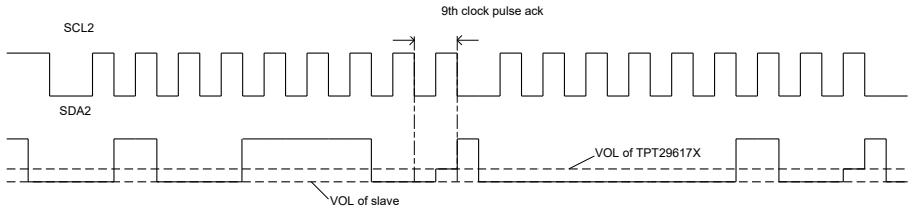


Figure 11. PORT-2 (2.25 V ~ 5.5 V) Waveform

Since A port is 5 V tolerant, the V_{REF1} can be lowered to support the device spectrum while still supporting 5 V signals on port-1.

On the port-2 side of the TPT29617X-S, the clock and data lines have a positive offset from the ground equal to the V_{OL} of the TPT29617X-S. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device which is very close to ground in this example. At the end of the acknowledgment, the level rises only to the Low level set by the driver in port-2.

The TPT29617X-S for a short delay while the port-1 side rises above $0.3*V_{REF1}$ then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the TPT29617X-S (V_{IL}) be at or below 0.4 V to be recognized by the TPT29617X-S and then transmitted to the port-1 side.

Multiple TPT29617X-S port-1 sides can be connected in a star configuration (Figure 12), allowing all nodes to communicate with each other.

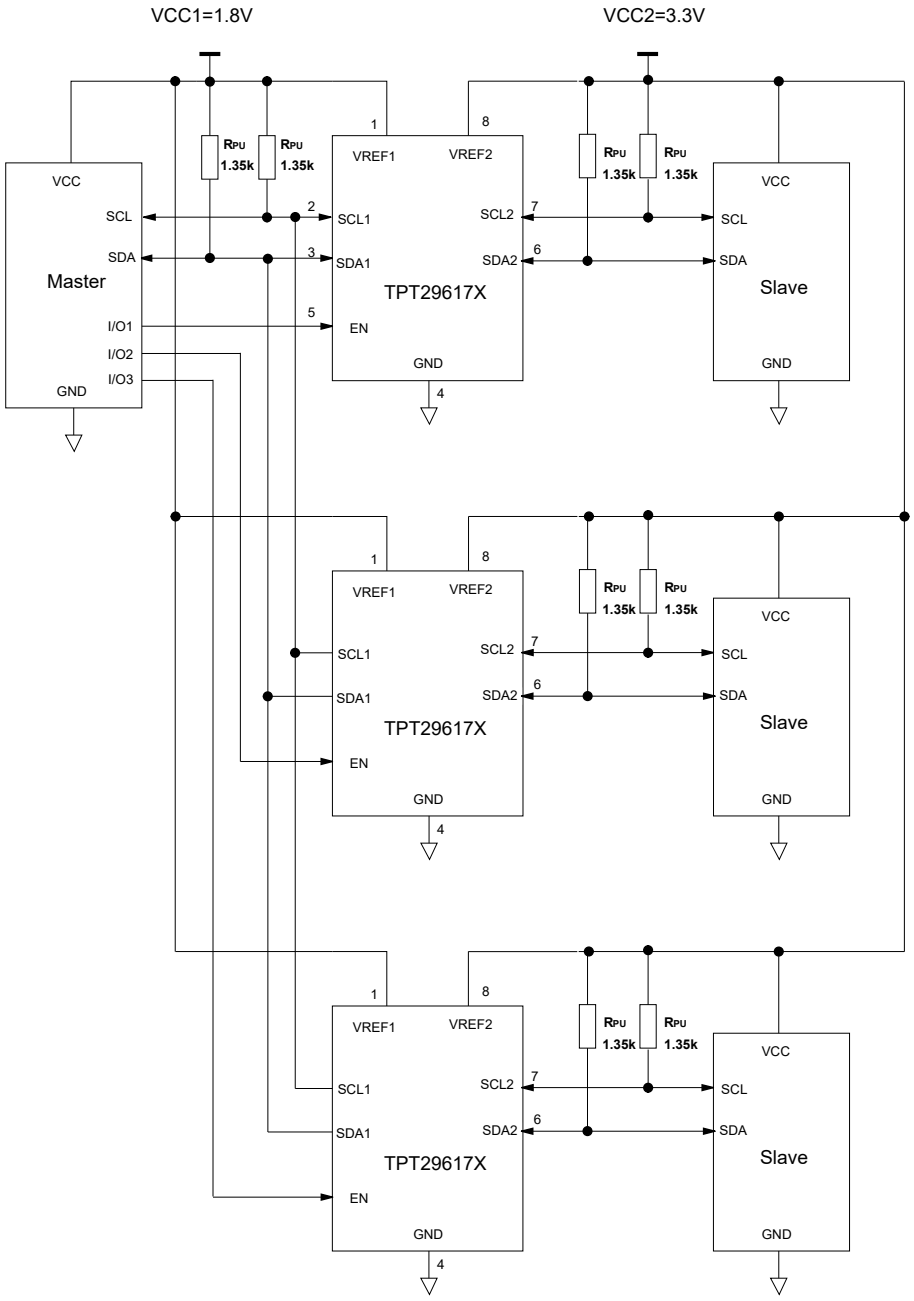


Figure 12. Typical Application Circuit, Star Network

Multiple TPT29617X-S can be connected in series (Figure 13) as long as port-1 is connected to port-2. I²C-bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

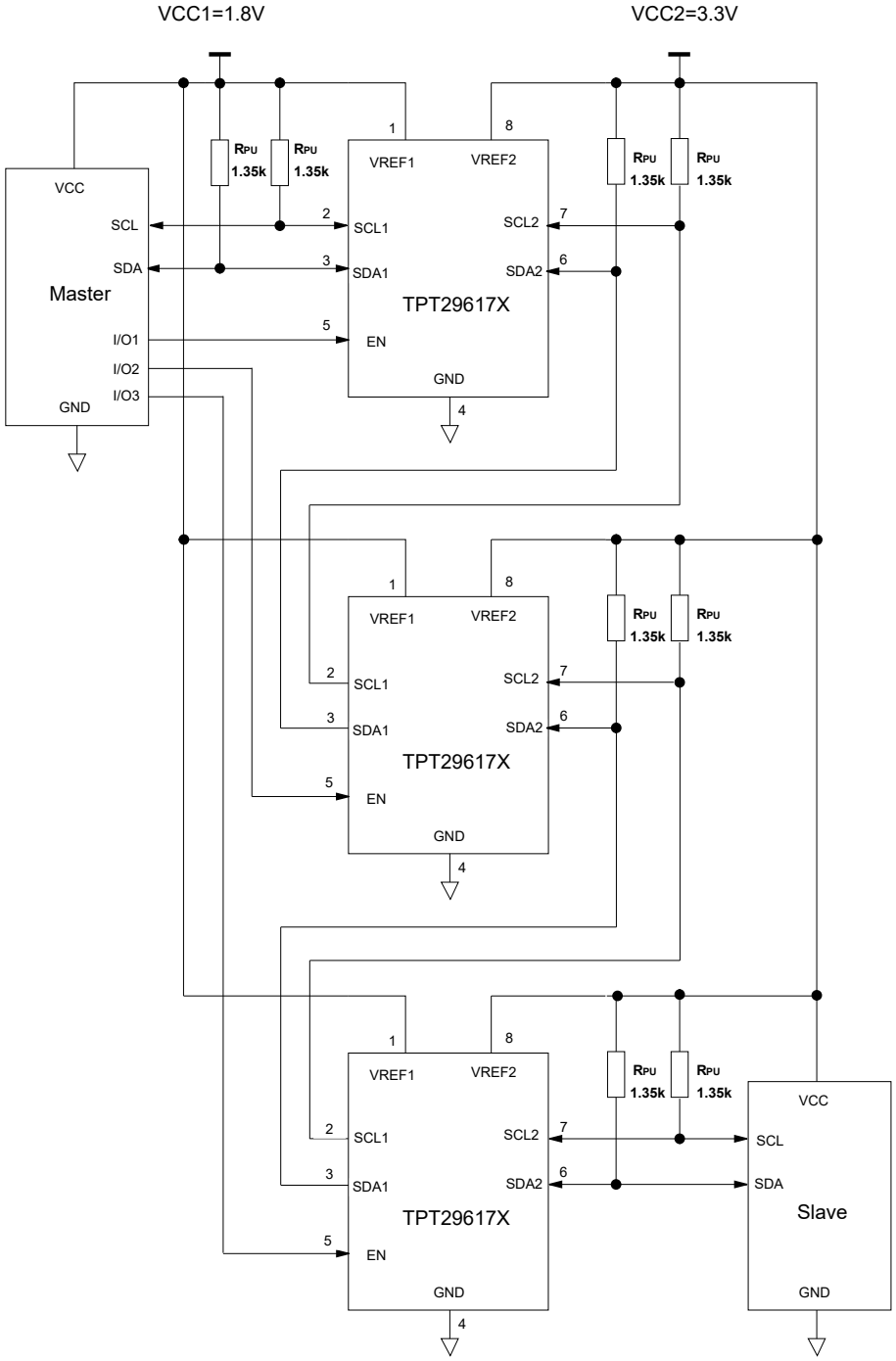


Figure 13. Typical Application Circuit, Series Network

Decoupling capacitors are not shown for simplicity, but they are required. It is especially important that the decoupling for the TPT29617X-S VREF2 be close to the VREF2 pin.

Layout

Layout Example

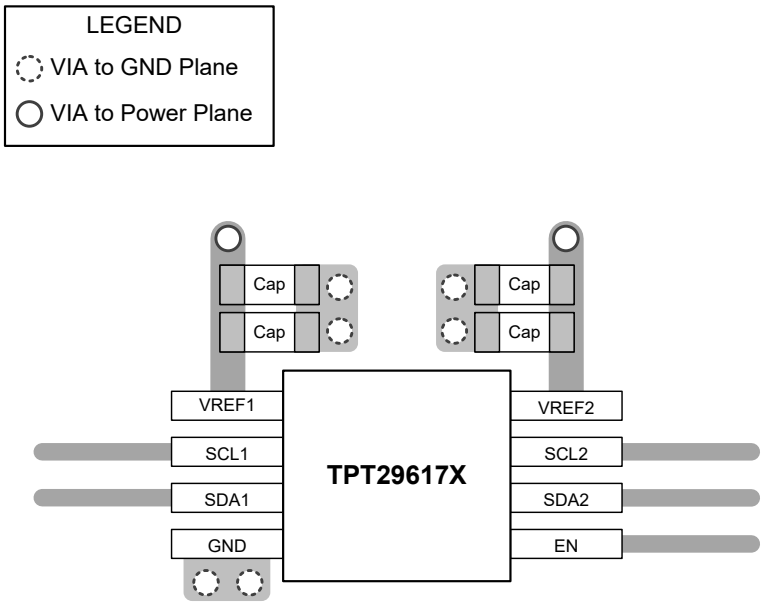
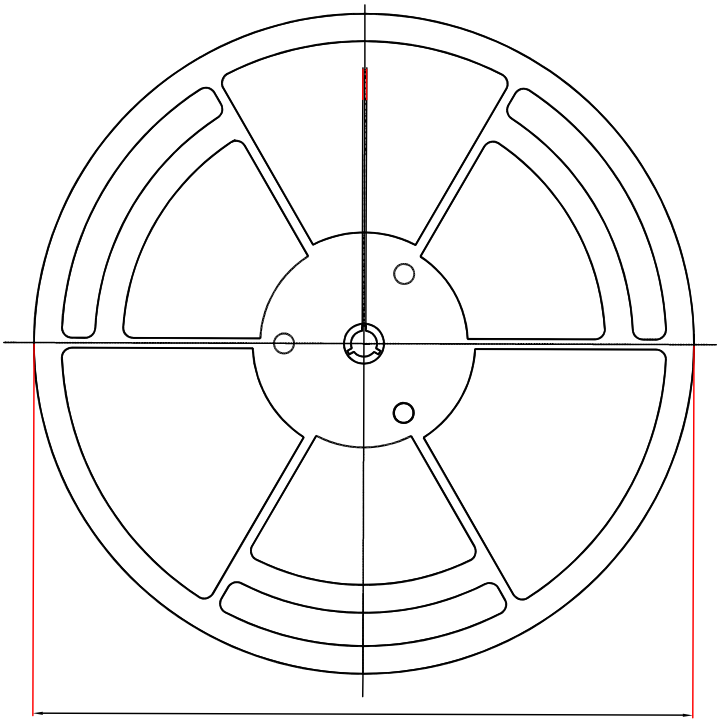
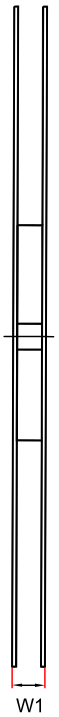
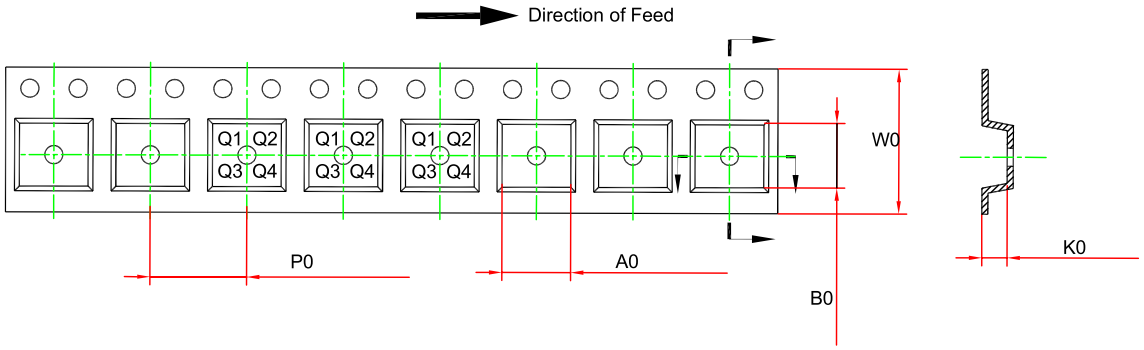


Figure 14. TPT29617X-S Layout Example

Tape and Reel Information





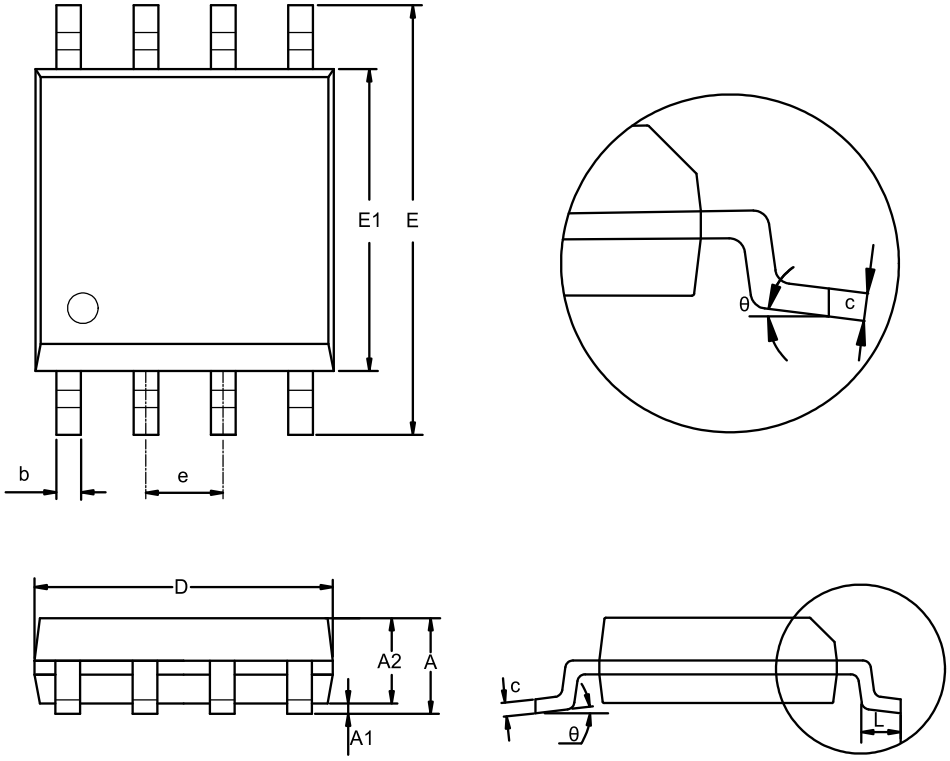


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPT29617X-VS1R-S	MSOP8	330	5.3	1.3	12	17.6	3.4	8	Q1

Package Outline Dimensions

MSOP8

Package Outline Dimensions VS1(MSOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29617X-VS1R-S	−40 to 125°C	MSOP8	9617X	MSL3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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