Dual Bidirectional I3C/I²C-bus and SPI Voltage-level Translator

Features

- Provides Voltage Level Translation for I3C, I²C-bus, SMBus and SPI Devices
- I3C Compliant with Data Dates up to 12.5 MHz
- Wide Supply Voltage Range:
  - V_{CCA} Range: 0.72 V to 1.98 V
  - V_{CCB} Range: 0.72 V to 1.98 V; $V_{CCA} \le V_{CCB}$
- I_{OFF} Supports Partial Power-down Mode
- Inputs Tolerate Overvoltages up to 1.98 V
- OE Input is Referenced to V_{CCA} with 1.98-V Overvoltage Tolerance
- High-impedance Outputs when OE = LOW or V_{CC} = 0 V

Applications

- I²C, I3C, SMBus, PMBus, SPI, and Other Two-Signal Interfaces
- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets

Description

The TPT29606 is a 2-bit, I3C/I²C-bus, and SPI voltage-level translator. It features automatic direction sensing and is suitable for traditional I²C-bus and SMBus applications, as well as 12.5-MHz I3C-bus applications and higher speed SPI applications.

The supply voltage range for V_{CCA} and V_{CCB} is 0.72 V to 1.98 V, with the requirement that V_{CCA} must be less than V_{CCB}. The OE input pin is referenced to V_{CCA}. The OE pin can withstand a voltage up to 1.98 V. Its control signal can be sourced from either V_{CCA} or V_{CCB} power domains. When the OE signal is at a low level, the device enters a high-impedance state.

The TPT29606 is available in DFN1.4X1-8 and SOT23-8 packages, and is characterized from −40°C to +125°C.

Typical Application Circuit

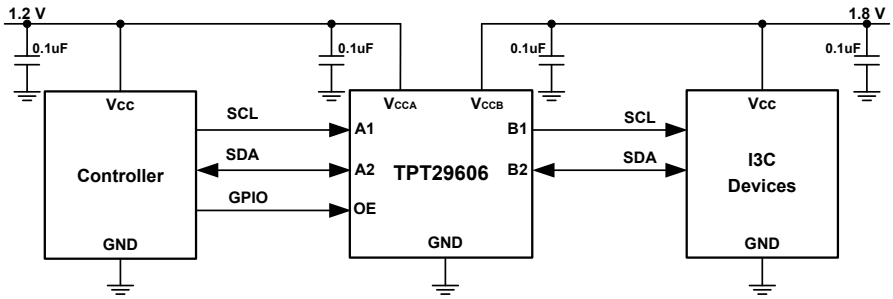


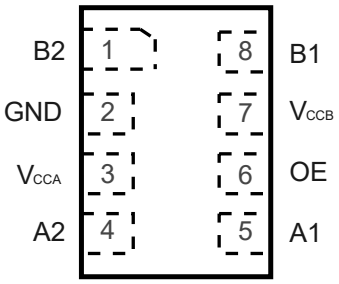
Table of Contents

Revision History

Date	Revision	Notes
2025-06-16	Rev.A.0	Released version

Pin Configuration and Functions

TPT29606-DFSRR
DFN1.4X1-8
Top View



TPT29606-T8TR
SOT23-8
Top View

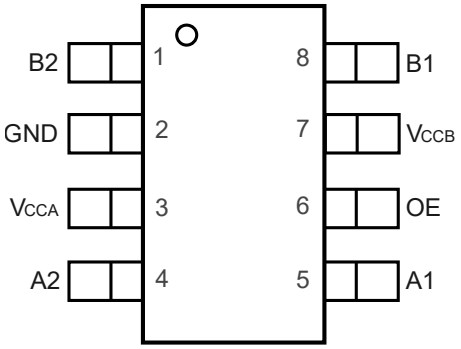


Table 1. Pin Functions: TPT29606

Pin		I/O	Description
No.	Name		
1	B2	I/O	B2 port input or output (Referenced to V_{CCB})
2	GND	-	Supply ground
3	V_{CCA}	-	A-port supply
4	A2	I/O	A2 port input or output (Referenced to V_{CCA})
5	A1	I/O	A1 port input or output (Referenced to V_{CCA})
6	OE	I	Output enable (Referenced to V_{CCA}, active HIGH; signal can be from V_{CCA} or V_{CCB} domain)
7	V_{CCB}	-	B-port supply
8	B1	I/O	B1 port input or output (Referenced to V_{CCB})

Table 2. Functional Table

Supply voltage		Input (1)	Input/output
V_{CCA}	V_{CCB}	OE (2)	
0.72 V to 1.98 V	0.72 V to 1.98 V	L	disconnected
0.72 V to 1.98 V	0.72 V to 1.98 V	H	A1 = B1; A2 = B2
GND (3)	GND (3)	X	disconnected

(1) H = HIGH voltage level; L = LOW voltage level; X = don't care
(2) V_{IL} and V_{IH} are referenced to V_{CCA}. OE can tolerate an overvoltage of 1.8 V.
(3) When either V_{CCA} or V_{CCB} is at GND level, the device goes into Power-down mode.

Specifications

Absolute Maximum Ratings (1)

Parameter		Conditions	Min	Max	Unit
V_{CCA}	Supply Voltage A	$V_{CCA} \le V_{CCB}$	−0.5	2.5	V
V_{CCB}	Supply Voltage B	$V_{CCA} \le V_{CCB}$	−0.5	2.5	V
V_I	Input Voltage (2)	A port, B port, and OE	−0.5	2.5	V
V_O	Output Voltage (2)	Active mode	−0.5	V_{CCO} + 0.25 (3)(4)	V
		Power-down or 3-state mode	−0.5	2.5	V
I_{IK}	Input Clamp Current	V_I < 0 V	−50		mA
I_{OK}	Output Clamp Current	V_O < 0 V	−50		mA
I_O	Output Current	V_O = 0 V to V_{CCO} (3)	−50	50	mA
I_{CC}	Supply Current	I_{CCA} or I_{CCB}		100	mA
I_{GND}	Ground Current		−100		mA
T_{stg}	Storage Temperature		−65	150	°C
P_{tot}	Total Power Dissipation	T_{amb} = −40°C to +125°C		125	mW

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) V_{CCO} is the supply voltage associated with the output.
(4) V_{CCO} + 0.25 V should not exceed 2.5 V.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions (1)

Parameter		Conditions	Min	Max	Unit
V_{CCA}	Supply Voltage A	$V_{CCA} \le V_{CCB}$	0.72	1.98	V
V_{CCB}	Supply Voltage B	$V_{CCA} \le V_{CCB}$	0.72	1.98	V
V_I	Input Voltage	A port, B port, and OE	0	1.98	V
V_O	Output Voltage	A port	0	1.98	V
		B port	0	1.98	V
T_{amb}	Ambient Temperature		−40	125	°C

Parameter		Conditions	Min	Max	Unit
T_J	Junction Temperature		−40	125	°C
$\Delta t/\Delta V$	Input Transition Rise and Fall Rate	V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V		5.3	ns/V

(1) The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
DFN1.4X1-8	288	147	°C/W
SOT23-8	195	124	°C/W

Static Characteristics

All test conditions: V_{CCA} = 0.72 V to 1.98 V, V_{CCB} = 0.72 V to 1.98 V, T_A = −40°C to +85°C. Typical specifications are at T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level Input Voltage	A port or B port	V_{CCA} = 0.72 V to 0.9 V; V_{CCB} = 0.72 V to 0.9 V;	V_{CCI} − 0.2			V
		A port or B port	V_{CCA} = 0.9 V to 1.98 V; V_{CCB} = 0.9 V to 1.98 V;	V_{CCI} − 0.4			V
		OE input		0.65× V_{CCA}			V
V_{IL}	LOW-level Input Voltage	A port or B port				0.3× V_{CCA}	V
		OE input				0.3× V_{CCA}	V
V_{OH}	HIGH-level Output Voltage	A port	I_O = −20 μA	V_{CCO} − 0.4			V
		B port	I_O = −20 μA	V_{CCO} − 0.4			V
V_{OL}	LOW-level Output Voltage	A port	I_O = −20 μA			0.3	V
		B port	I_O = −20 μA			0.3	V
I_I	Input Leakage Current	OE input	V_I = 0 V to 1.98 V	−2		2	μA
I_{OZ}	OFF-state Output Current	A or B port	V_O = 0 V to 1.98 V	−2		2	μA
I_{OFF}	Power-off Leakage Current	A port; V_O = 0 V to 1.98 V	V_{CCA} = 0 V; V_{CCB} = 0 V to 1.98 V	−7		7	μA
		B port; V_O = 0 V to 1.98 V	V_{CCB} = 0 V; V_{CCA} = 0 V to 1.98 V	−7		7	μA
I_{CCA}	Supply Current	V_I = 0 V or V_{CCI}; I_O = 0 A	OE = LOW		0.8	7	μA
			OE = HIGH		0.8	7	μA
			V_{CCA} = 1.98 V; V_{CCB} = 0 V;		0.9	9	μA
			V_{CCA} = 0 V; V_{CCB} = 1.98 V;	−2	−0.02		μA
I_{CCB}	Supply Current	V_I = 0 V or V_{CCI}; I_O = 0 A	OE = LOW		0.8	8	μA
			OE = HIGH		0.8	11	μA
			V_{CCA} = 1.98 V; V_{CCB} = 0 V;	−2	-0.02		μA
			V_{CCA} = 0 V; V_{CCB} = 1.98 V;		0.9	9	μA
I_{CCA} + I_{CCB}	Supply Current	V_I = 0 V or V_{CCI}; I_O = 0 A	OE = LOW		1.6	16	μA

Static Characteristics

All test conditions: V_{CCA} = 0.72 V to 1.98 V, V_{CCB} = 0.72 V to 1.98 V, T_A = −40°C to +125°C. Typical specifications are at T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level Input Voltage	A port or B port	V_{CCA} = 0.72 V to 0.9 V; V_{CCB} = 0.72 V to 0.9 V;	V_{CCI} − 0.2			V
		A port or B port	V_{CCA} = 0.9 V to 1.98 V; V_{CCB} = 0.9 V to 1.98 V;	V_{CCI} − 0.4			V
		OE input		0.65× V_{CCA}			V
V_{IL}	LOW-level Input Voltage	A port or B port				0.3× V_{CCA}	V
		OE input				0.3× V_{CCA}	V
V_{OH}	HIGH-level Output Voltage	A port	I_O = −20 μA	V_{CCO} − 0.4			V
		B port	I_O = −20 μA	V_{CCO} − 0.4			V
V_{OL}	LOW-level Output Voltage	A port	I_O = −20 μA			0.3	V
		B port	I_O = −20 μA			0.3	V
I_I	Input Leakage Current	OE input	V_I = 0 V to 1.98 V	−6		6	μA
I_{OZ}	OFF-state Output Current	A or B port	V_O = 0 V to 1.98 V	−10		10	μA
I_{OFF}	Power-off Leakage Current	A port; V_O = 0 V to 1.98 V	V_{CCA} = 0 V; V_{CCB} = 0 V to 1.98 V	−37		37	μA
		B port; V_O = 0 V to 1.98 V	V_{CCB} = 0 V; V_{CCA} = 0 V to 1.98 V	−37		37	μA
I_{CCA}	Supply Current	V_I = 0 V or V_{CCI}; I_O = 0 A	OE = LOW		0.8	32	μA
			OE = HIGH		0.8	28	μA
			V_{CCA} = 1.98 V; V_{CCB} = 0 V;		0.9	40	μA
			V_{CCA} = 0 V; V_{CCB} = 1.98 V;	−15	−0.02		μA
I_{CCB}	Supply Current	V_I = 0 V or V_{CCI}; I_O = 0 A	OE = LOW		0.8	29	μA
			OE = HIGH		0.8	36	μA
			V_{CCA} = 1.98 V; V_{CCB} = 0 V;	−15	-0.02		μA
			V_{CCA} = 0 V; V_{CCB} = 1.98 V;		0.9	40	μA
I_{CCA} + I_{CCB}	Supply Current	V_I = 0 V or V_{CCI}; I_O = 0 A	OE = LOW		1.6	65	μA

Dynamic Characteristics (1)

All test conditions: V_{CCA} = 0.8 V, T_A = −40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{pd} (2)	Propagation Delay	A to B; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	2.1	5.6	7.7	ns
		B to A; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	1.2	10.6	19.9	ns
		A to B; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	1.7	3.9	5.3	ns
		B to A; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	0.5	9.6	17.2	ns
t_{en}	Enable Time	OE to A, B; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;			250	ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;			250	ns
t_{dis}	Disable Time	OE to A; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;			350	ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;			350	ns
		OE to B; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;			350	ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;			350	ns
t_t	Transition Time	A port; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	2.1	8.5	17.5	ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	1.5	9.0	15.4	ns
		B port; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	1.1	4.0	5.8	ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	0.7	1.5	2.1	ns
$t_{sk(o)}$	Output Skew Time	delta between channels (3)	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	0.0	0.2	0.4	ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	0.0	0.2	0.4	ns
t_W	Pulse Width	data inputs	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	37			ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	37			ns
f_{data}	Data Rate		V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	0.064		26	Mbps
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	0.064		26	Mbps

(1) Parameters are provided by the lab bench test and design simulation.

(2) t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}.

(3) $t_{sk(o)}$ means skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

Dynamic Characteristics (continued) (1)

All test conditions: V_{CCA} = 1.2 V, T_A = −40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{pd} (2)	Propagation Delay	A to B; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	1.5	4.5	6.1	ns
		B to A; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	1.1	3.9	5.3	ns
		A to B; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	1.0	2.5	3.5	ns
		B to A; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	0.6	2.8	3.9	ns
t_{pdc}	Propagation Delay	A to B; C_L = 80 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	2.5	4.9	7	ns
		B to A; C_L = 30 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	0.9	3.4	5	ns
t_{en}	Enable Time	OE to A, B; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;			250	ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;			250	ns
t_{dis}	Disable Time	OE to A; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;			350	ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;			350	ns
		OE to B; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;			350	ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;			350	ns
t_t	Transition Time	A port; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	0.8	2.6	3.5	ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	0.6	1.5	2.5	ns
		B port; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	1.1	3.6	5.1	ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	0.6	1.3	2.2	ns
t_{tc}	Transition Time	A port; C_L = 30 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	1.0	2.2	3.6	ns
		B port; C_L = 80 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	2.5	4.3	6.3	ns
$t_{sk(o)}$	Output Skew Time	delta between channels (3)	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	0.0	0.1	0.2	ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	0.0	0.1	0.3	ns
t_W	Pulse Width	data inputs	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	15.0			ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	13.5			ns
f_{data}	Data Rate		V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	0.064		52	Mbps
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	0.064		52	Mbps

(1) Parameters are provided by the lab bench test and design simulation.
(2) t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}.
(3) Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

Dynamic Characteristics (continued) (1)

All test conditions: V_{CCA} = 1.8 V, T_A = −40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{pd} (2)	Propagation Delay	A to B; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;	1.0	2.5	3.4	ns
		B to A; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;	0.7	2.3	3.0	ns
t_{en}	Enable Time	OE to A, B; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;			250	ns
t_{dis}	Disable Time	OE to A; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;			350	ns
		OE to B; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;			350	ns
t_t	Transition Time	A port; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;	0.5	1.2	1.7	ns
		B port; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.2 V;	0.7	1.7	2.5	ns
$t_{sk(o)}$	Output Skew Time	delta between channels (3)	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;	0.0	0.1	0.2	ns
t_W	Pulse Width	data inputs	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;	13.5			ns
f_{data}	Data Rate		V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;	0.064		52	Mbps

(1) Parameters are provided by the lab bench test and design simulation.

(2) t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}.

(3) Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

Dynamic Characteristics (continued) (1)

All test conditions: V_{CCA} = 0.8 V, T_A = −40°C to +125°C, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{pd} (2)	Propagation Delay	A to B; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	2.1	5.6	7.7	ns
		B to A; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	1.2	10.6	19.9	ns
		A to B; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	1.7	3.9	5.3	ns
		B to A; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	0.5	9.6	17.2	ns
t_{en}	Enable Time	OE to A, B; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;			250	ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;			250	ns
t_{dis}	Disable Time	OE to A; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;			350	ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;			350	ns
		OE to B; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;			350	ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;			350	ns
t_t	Transition Time	A port; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	2.1	8.5	17.5	ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	1.5	9.0	15.4	ns
		B port; C_L = 15 pF	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	1.1	4.0	5.8	ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	0.7	1.5	2.1	ns
$t_{sk(o)}$	Output Skew Time	delta between channels (3)	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	0.0	0.2	0.4	ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	0.0	0.2	0.4	ns
t_W	Pulse Width	data inputs	V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	37			ns
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	37			ns
f_{data}	Data Rate		V_{CCA} = 0.8 V; V_{CCB} = 1.2 V;	0.064		26	Mbps
			V_{CCA} = 0.8 V; V_{CCB} = 1.8 V;	0.064		26	Mbps

(1) Parameters are provided by the lab bench test and design simulation.

(2) t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}.

(3) Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

Dynamic Characteristics (continued) (1)

All test conditions: V_{CCA} = 1.2 V, T_A = −40°C to +125°C, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{pd} (2)	Propagation Delay	A to B; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	1.5	4.5	6.2	ns
		B to A; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	1.1	3.9	5.4	ns
		A to B; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	1.0	2.5	3.6	ns
		B to A; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	0.6	2.8	4.0	ns
t_{pdc}	Propagation Delay	A to B; C_L = 80 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	2.5	4.9	7.4	ns
		B to A; C_L = 30 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	0.9	3.4	5.3	ns
t_{en}	Enable Time	OE to A, B; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;			250	ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;			250	ns
t_{dis}	Disable Time	OE to A; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;			350	ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;			350	ns
		OE to B; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;			350	ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;			350	ns
t_t	Transition Time	A port; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	0.8	2.6	3.5	ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	0.6	1.5	2.6	ns
		B port; C_L = 15 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	1.1	3.6	5.1	ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	0.6	1.3	2.3	ns
t_{tc}	Transition Time	A port; C_L = 30 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	1.0	2.2	3.8	ns
		B port; C_L = 80 pF	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	2.5	4.3	6.9	ns
$t_{sk(o)}$	Output Skew Time	delta between channels (3)	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	0.0	0.1	0.2	ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	0.0	0.1	0.3	ns
t_W	Pulse Width	data inputs	V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	15.0			ns
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	13.5			ns
f_{data}	Data Rate		V_{CCA} = 1.2 V; V_{CCB} = 1.2 V;	0.064		52	Mbps
			V_{CCA} = 1.2 V; V_{CCB} = 1.8 V;	0.064		52	Mbps

(1) Parameters are provided by the lab bench test and design simulation.
(2) t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}.
(3) Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

Dynamic Characteristics (continued) (1)

All test conditions: V_{CCA} = 1.8 V, T_A = −40°C to +125°C, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{pd} (2)	Propagation Delay	A to B; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;	1.0	2.5	3.5	ns
		B to A; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;	0.7	2.3	3.1	ns
t_{en}	Enable Time	OE to A, B; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;			250	ns
t_{dis}	Disable Time	OE to A; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;			350	ns
		OE to B; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;			350	ns
t_t	Transition Time	A port; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;	0.5	1.2	1.7	ns
		B port; C_L = 15 pF	V_{CCA} = 1.8 V; V_{CCB} = 1.2 V;	0.7	1.7	2.6	ns
$t_{sk(o)}$	Output Skew Time	delta between channels (3)	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;	0.0	0.1	0.2	ns
t_W	Pulse Width	data inputs	V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;	13.5			ns
f_{data}	Data Rate		V_{CCA} = 1.8 V; V_{CCB} = 1.8 V;	0.064		52	Mbps

(1) Parameters are provided by the lab bench test and design simulation.
(2) t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}.
(3) Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

Test Circuit and Waveforms

The test circuit for measuring data rate, pulse width, propagation delay, output rise time, and fall time is shown in Figure 1.

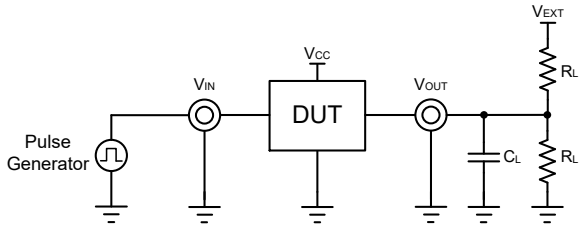


Figure 1. Test Circuits

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 26 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
(2) R_L is the load resistance; C_L is the load capacitance, including jig and probe capacitance; V_{EXT} is the external voltage for measuring switching times.
(3) For measuring data rate, pulse width, propagation delay, and output rise and fall measurements, R_L = 1 MΩ; for measuring enable and disable times, R_L = 50 kΩ.

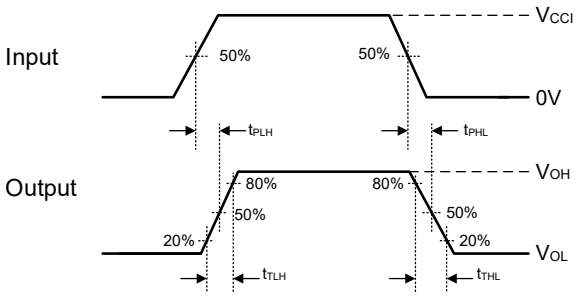


Figure 2. Propagation Delay Times

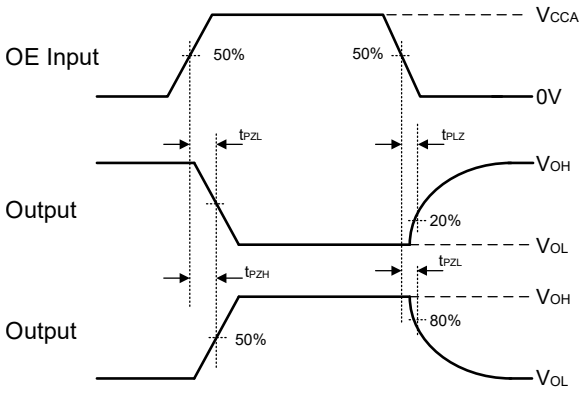


Figure 3. Enable and Disable Times

(1) t_{pd} is the same as t_{PLH} and t_{PHL}; t_t is the same as t_{THL} and t_{TLH}.
(2) t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.
(3) For measuring t_{PZL} and t_{PLZ}, V_{EXT} = 2 × V_{CCO}.
(4) V_{CCI} is the supply voltage associated with the input port.
(5) V_{CCO} is the supply voltage associated with the output port.
(6) V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Detailed Description

Overview

The TPT29606 is a 2-bit, I3C/I²C-bus and SPI voltage-level translator. It features automatic direction sensing and is suitable for traditional I²C-bus and SMBus applications, as well as 12.5 MHz I3C-bus applications and higher speed SPI applications.

The supply voltage range for V_{CCA} and V_{CCB} is 0.72 V to 1.98 V, with the requirement that V_{CCA} must be less than V_{CCB}. The OE input pin is referenced to V_{CCA}. The OE pin can withstand a voltage up to 1.98 V. Its control signal can be sourced from either V_{CCA} or V_{CCB} power domains. When the OE signal is at a low level, the device enters a high-impedance state.

Functional Block Diagram

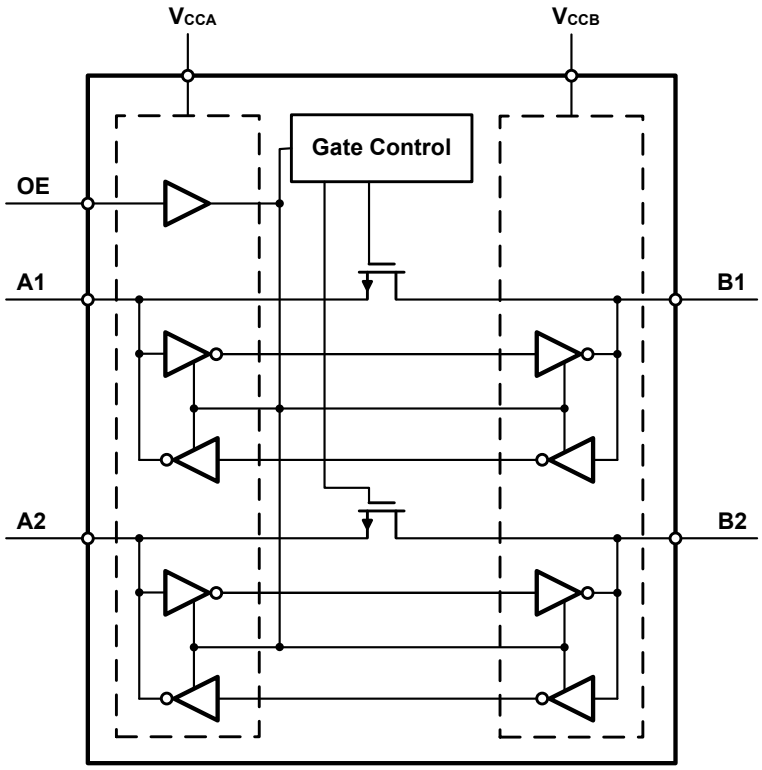


Figure 4. Functional Block Diagram

Feature Description

Architecture

The TPT29606 architecture employs an N-channel pass-gate transistor for level translation, integrated with internal pull-up resistors and edge-rate acceleration circuitry. During low-level cycles, the N-channel pass-gate transistor is turned on, while during high-level cycles, it is turned off and the port voltage is pulled up to V_{CC} through an internal 10 kΩ resistor. The pull-up resistor is enabled only when both V_{CCA} and V_{CCB} are powered on, OE is high, and the bus is high. The edge-rate acceleration circuitry is implemented as a one-shot circuit. It speeds up the output slew rate, enabling high-speed communication. The TPT29606 achieves bidirectional signal transmission between Port A and Port B without requiring a direction-control signal. It is compatible with both open-drain and push-pull operations.

Power-up and Power-down

During operation of the TPT29606, V_{CCA} must be lower than V_{CCB}. The device has no power-up sequencing requirement. Either supply can be powered on first without damaging the device. When either V_{CCA} or V_{CCB} is disconnected, the chip disables all output ports and enters power-down mode.

Enable and Disable

The OE pin is used to enable or disable the device. When OE is driven low, the device enters a high-impedance state. The V_{IH} and V_{IL} thresholds of OE are referenced to V_{CCA}. The OE pin can withstand a voltage up to 1.98 V. Its control signal can be sourced from either V_{CCA} or V_{CCB} power domains. OE must not be left floating in any condition and must be kept low during power-up or power-down.

Input Driver Requirements

The continuous DC current sinking and sourcing capabilities of the TPT29606 are determined by the external system-level design, depending on the type of connected drivers (open-drain or push-pull). The high-bandwidth IO circuitry enables a fast change between input and output. It has a modest sourcing capability of hundreds of microamperes, as determined by the pull-up resistor. The signal fall time depends on the slew rate, output impedance, and capacitive load of the line.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

The TPT29606 achieves bidirectional level translation between devices or systems operating at different supply voltages. It is suitable for I3C, I²C, and SPI applications. Typical application circuits are shown in Figure 5, Figure 6, and Figure 7.

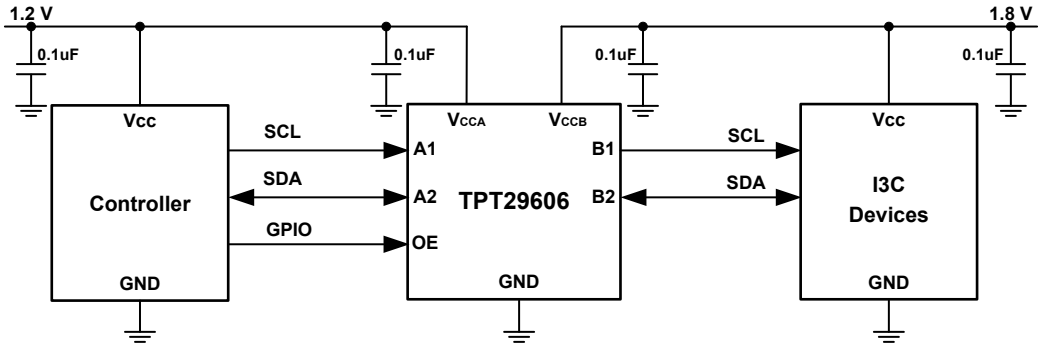


Figure 5. I3C Typical Application Circuit

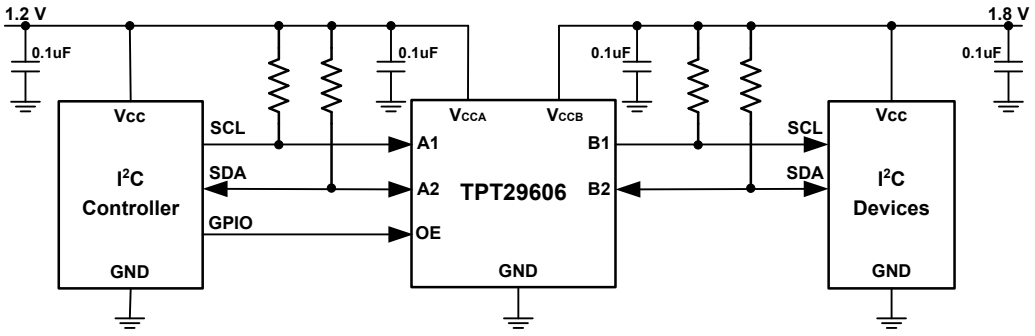


Figure 6. I²C Typical Application Circuit

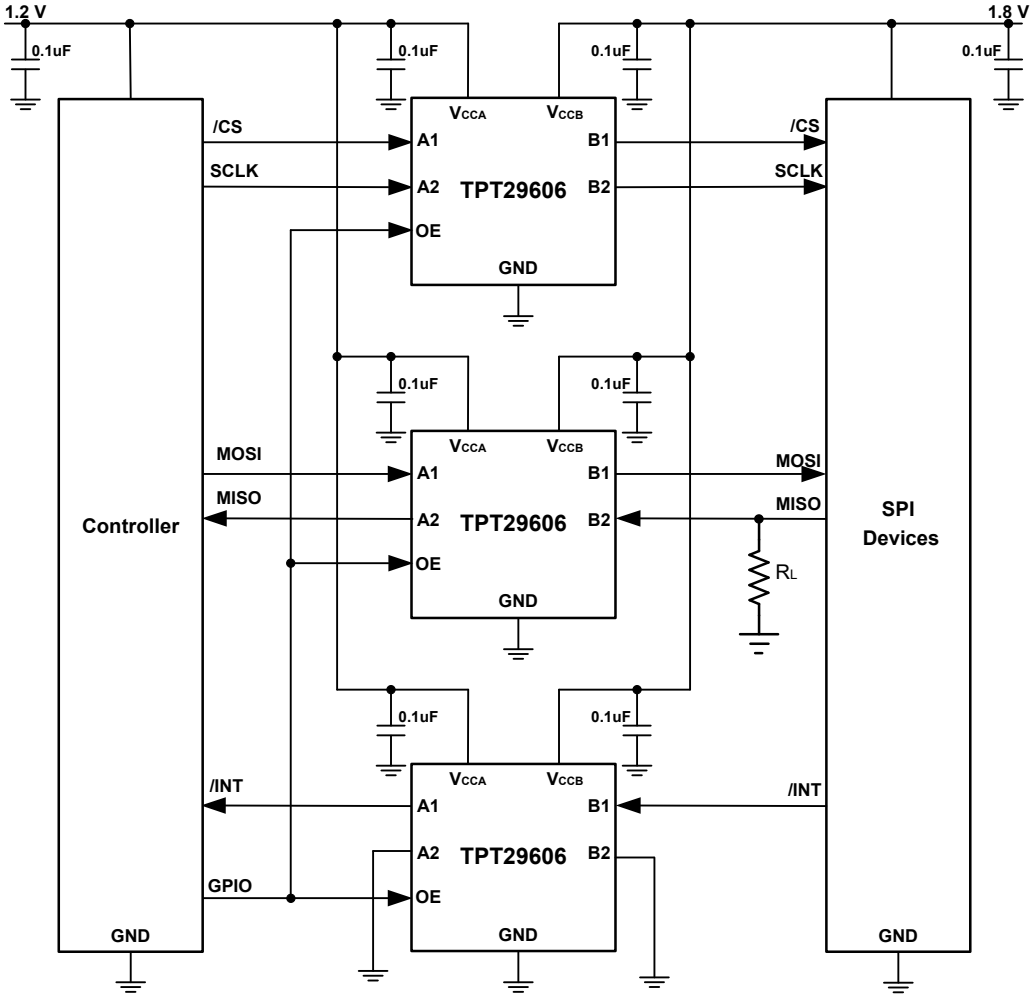


Figure 7. SPI Typical Application Circuit

Layout

Layout Example

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they have to turn corners. Figure 8 shows progressively better techniques for rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

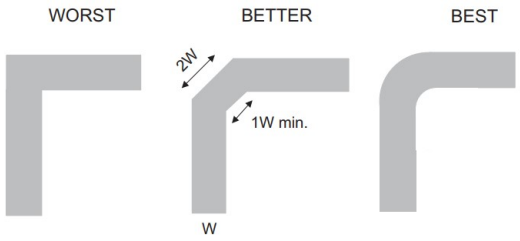


Figure 8. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 9 illustrates an example of a PCB layout with the TPT29606. Some key considerations are:

- Decouple the V_{CC} pin with a 0.1-μF capacitor, and place as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{CC} supply.
- Keep the trace length as short as possible to avoid excessive loading.
- PCB signal trace lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 8 ns, ensuring that any reflection encounters low impedance at the source driver.

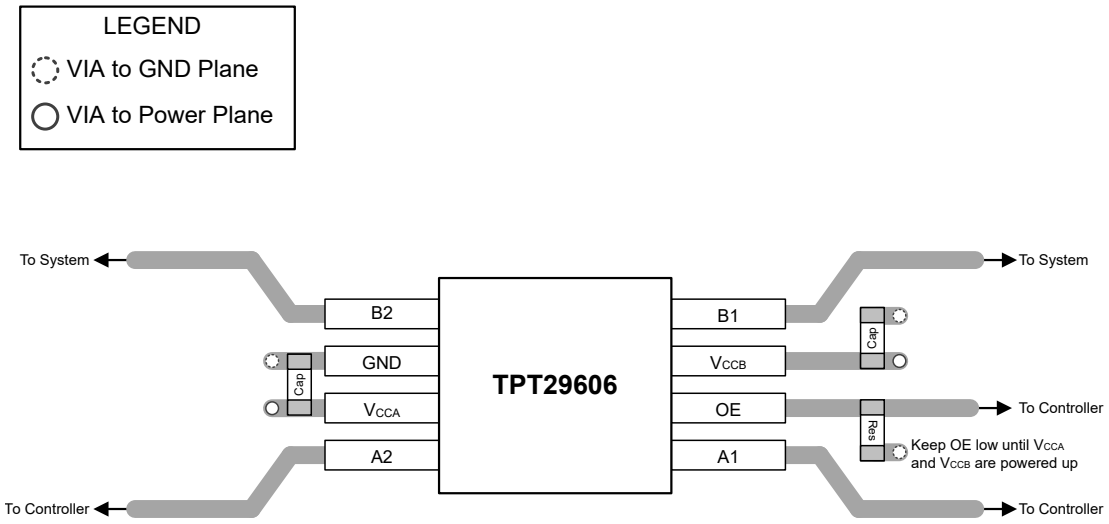
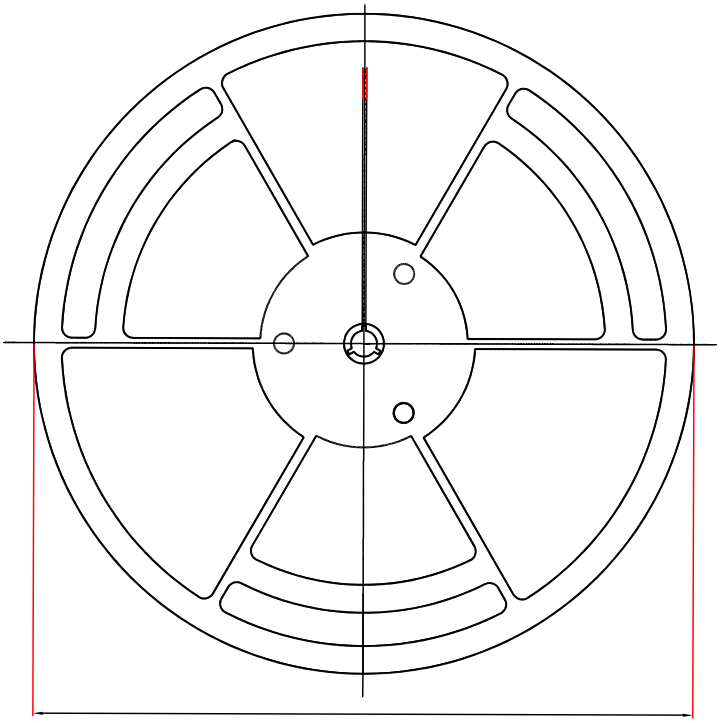
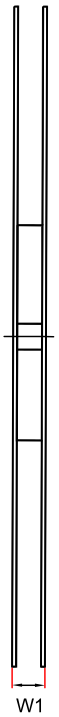
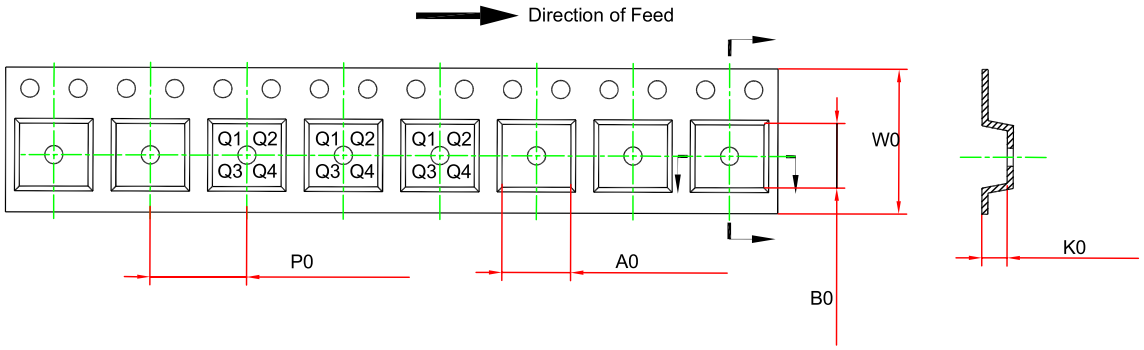


Figure 9. TPT29606 Layout Example

Tape and Reel Information





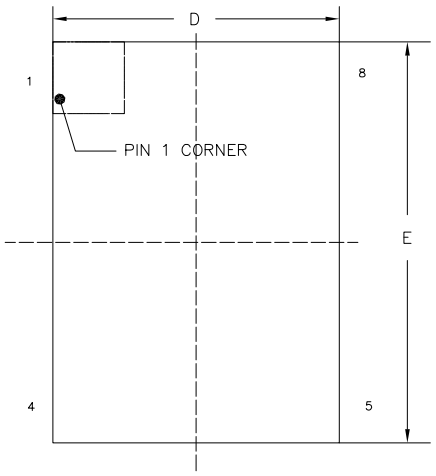


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT29606-DFSRR	DFN1.4X1-8	180	13.1	1.15	1.6	0.5	4	8	Q1
TPT29606-T8TR	SOT23-8	178	13.1	3.3	3.2	1.4	4	8	Q3

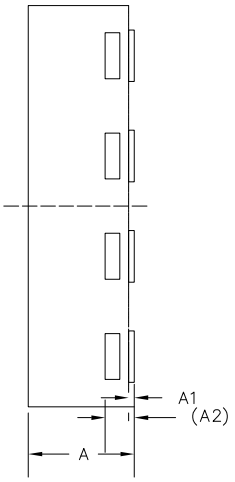
Package Outline Dimensions

DFN1.4X1-8

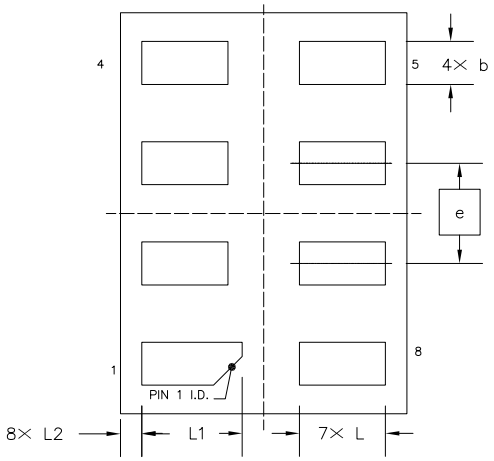
Package Outline Dimensions DFSR(DFN1.4X1-8-B)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

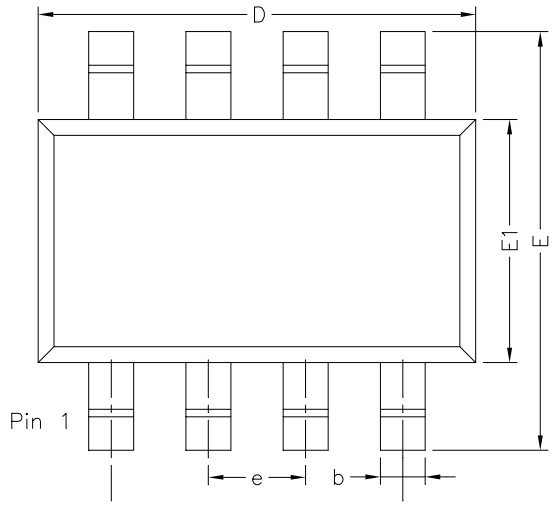
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

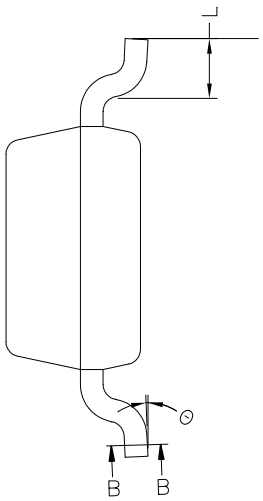
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.320	0.400	0.013	0.016
A1	0.000	0.050	0.000	0.002
A2	0.102 REF		0.004 REF	
b	0.100	0.200	0.004	0.008
D	1.000 BSC		0.039 BSC	
E	1.400 BSC		0.055 BSC	
e	0.350 BSC		0.014 BSC	
L	0.250	0.350	0.010	0.014
L1	0.300	0.400	0.011	0.016
L2	0.075 REF		0.003 REF	

SOT23-8

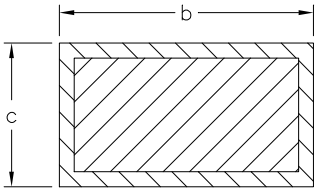
Package Outline Dimensions T8T(SOT23-8-B)



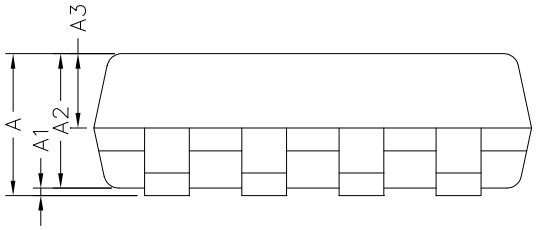
TOP VIEW



SIDE VIEW



SECTION B–B



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	---	1.100	---	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	1.000	0.031	0.034
A3	0.400	0.600	0.016	0.024
b	0.260	0.380	0.010	0.015
c	0.140	0.200	0.006	0.008
D	2.850	2.980	0.112	0.117
E	2.650	2.950	0.104	0.116
E1	1.550	1.680	0.061	0.066
e	0.650 BSC		0.026 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29606-DFSRR	−40 °C to +125 °C	DFN1.4X1-8	606	MSL3	Tape and Reel,4000	Green
TPT29606-T8TR	−40 °C to +125 °C	SOT23-8	606	MSL3	Tape and Reel,3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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