

Features

- Bidirectional Translator of 1:8 I²C Switch
- Active-Low Reset Input
- Three Address Terminals, Allowing up to 8 Devices on the I²C Bus
- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- Allows Voltage-Level Translation among 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- Support Standard Mode and Fast Mode I²C Devices, 0 to 400-kHz Clock Frequency
- Low R_{on} Switches
- Supports Hot Insertion
- Latch-Up Performance Reaches 600 mA per JESD 78
- ESD Protection Exceeds JESD 22
 - 7.0-kV Human-Body Model
 - 1.5-kV Charged-Device Model

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products with I²C Slave Address Conflicts (e.g., Multiple, Identical Temp Sensors)

Description

The TPT29548L-S is a 1:8 bidirectional translating I²C switch. The SCL/SDA upstream pair fans out to eight downstream channels. Any single SC_n/SD_n channel or combination of channels can be selected, determined by the programmable control register.

If one of the downstream I²C buses is stuck in a low state, then an active-low reset ($\overline{\text{RESET}}$) input helps the TPT29548L-S to recover. Pulling $\overline{\text{RESET}}$ low resets the I²C state machine and causes all the channels to be deselected, as the internal power-on reset function.

The pass gates of the switches are constructed so that the VCC terminal can be used to limit the maximum high voltage, which is passed by the TPT29548L-S and operates from 1.6 V to 5.5 V. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5-V tolerant.

The TPT29548L-S is available in TSSOP24 and QFN4X4-24 packages, and is characterized from -40°C to +125°C.

Typical Application Circuit

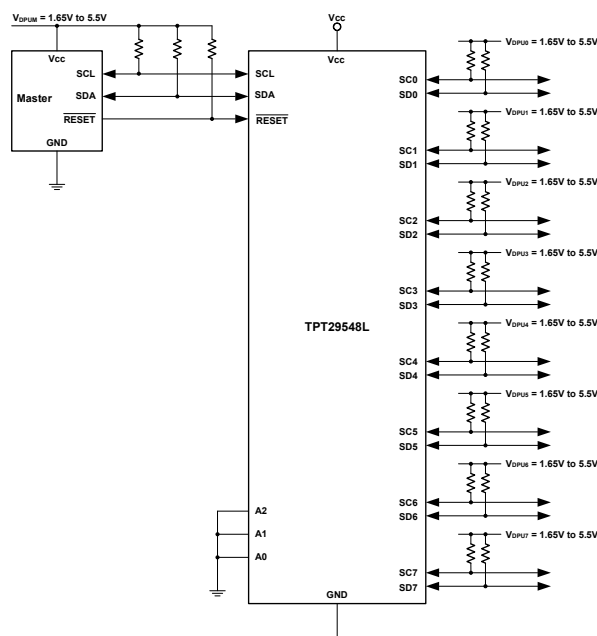


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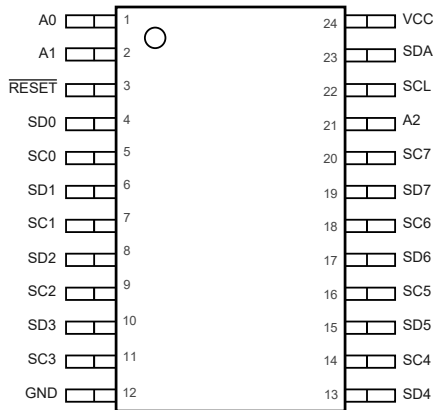
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Revision History

Date	Revision	Notes
2025-07-07	Rev.A.0	Released version

Pin Configuration and Functions

TPT29548L-S
TSSOP24



TPT29548L-S
QFN4×4-24

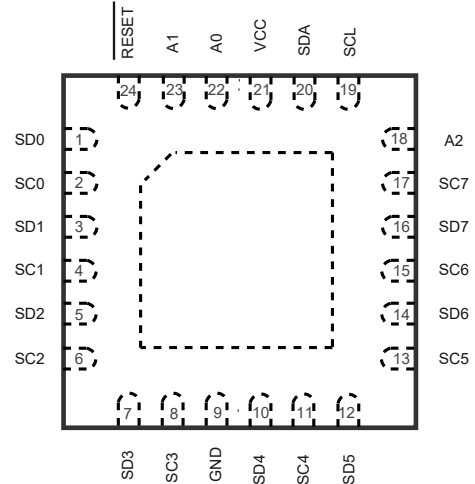


Table 1. Pin Functions

Pin No.		Name	I/O	Description
TSSOP24	QFN4×4-24			
1	22	A0	I	Address input 0. Connect directly to VCC or ground.
2	23	A1	I	Address input 1. Connect directly to VCC or ground.
3	24	RESET	I	Reset input, active LOW. Connect to VCC or pull up the power of the master side through a pull-up resistor, if not used.
4	1	SD0	I/O	Data 0. Connect to the power of the slave channel 0 through a pull-up resistor.
5	2	SC0	I/O	Clock 0. Connect to the power of the slave channel 0 through a pull-up resistor.
6	3	SD1	I/O	Data 1. Connect to the power of the slave channel 1 through a pull-up resistor.
7	4	SC1	I/O	Clock 1. Connect to the power of the slave channel 1 through a pull-up resistor.
8	5	SD2	I/O	Data 2. Connect to the power of the slave channel 2 through a pull-up resistor.
9	6	SC2	I/O	Clock 2. Connect to the power of the slave channel 2 through a pull-up resistor.
10	7	SD3	I/O	Data 3. Connect to the power of the slave channel 3 through a pull-up resistor.
11	8	SC3	I/O	Clock 3. Connect to the power of the slave channel 3 through a pull-up resistor.
12	9	GND	GND	Ground.

1.8-V 8-channel I²C Switch with Reset

Pin No.		Name	I/O	Description
TSSOP24	QFN4×4-24			
13	10	SD4	I/O	Data 4. Connect to the power of the slave channel 4 through a pull-up resistor.
14	11	SC4	I/O	Clock 4. Connect to the power of the slave channel 4 through a pull-up resistor.
15	12	SD5	I/O	Data 5. Connect to the power of the slave channel 5 through a pull-up resistor.
16	13	SC5	I/O	Clock 5. Connect to the power of the slave channel 5 through a pull-up resistor.
17	14	SD6	I/O	Data 6. Connect to the power of the slave channel 6 through a pull-up resistor.
18	15	SC6	I/O	Clock 6. Connect to the power of the slave channel 6 through a pull-up resistor.
19	16	SD7	I/O	Data 7. Connect to the power of the slave channel 7 through a pull-up resistor.
20	17	SC7	I/O	Clock 7. Connect to the power of the slave channel 7 through a pull-up resistor.
21	18	A2	I	Address input 2. Connect directly to VCC or ground.
22	19	SCL	I/O	Clock bus. Connect to VCC through a pull-up resistor.
23	20	SDA	I/O	Data bus. Connect to VCC through a pull-up resistor.
24	21	VCC	Supply	Supply voltage.
	25	Thermal Pad		For the QFN package, the exposed thermal pad must be connected to ground.

Specifications

Absolute Maximum Ratings ⁽¹⁾

Parameter		Min	Max	Unit
V _{CC}	Supply Voltage	-0.5	7	V
V _I	Input Voltage	-0.5	7	V
I _{IK}	Input Clamp Current, V _I < 0	-20	20	mA
I _{OK}	Output Clamp Current, V _O < 0	-25	25	mA
I _{CC}	Continuous Current Through GND	-100	100	mA
T _J	Maximum Junction Temperature		130	°C
T _A	Operating Temperature Range	-45	125	°C
T _{STG}	Storage Temperature Range	-60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter			Min	Max	Unit
V _{CC}	Supply Voltage		1.65	5.5	V
V _{IH}	High-Level Input Voltage	SCL, SDA	0.7 × V _{CC}	5.5	V
		A2~A0, $\overline{\text{RESET}}$	0.7 × V _{CC}	5.5	V
V _{IL}	Low-Level Input Voltage	SCL, SDA	-0.5	0.3 × V _{CC}	V
		A2~A0, $\overline{\text{RESET}}$	-0.5	0.3 × V _{CC}	V
T _A	Operating Temperature Range		-40	125	°C

Thermal Information

Package Type	θ _{JA}	θ _{JC}	Unit
TSSOP24	75	25	°C/W
QFN24	65	28	°C/W

1.8-V 8-channel I²C Switch with Reset
Electrical Characteristics - DC Parameters

All test conditions: $V_{CC} = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^{\circ}\text{C to }+125^{\circ}\text{C}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I _{DD}	Supply Current in Operating Mode	No load; V _I = V _{CC} or GND; f _{SCL} = 100 kHz		0.7	2	μA
		No load; V _I = V _{CC} or GND; f _{SCL} = 400 kHz		2.6	5	μA
I _{stb}	Standby Current	No load; V _I = V _{CC} or GND		0.2	1	μA
V _{POR}	Power-on Reset Voltage, V _{CC} Rising	No load; V _I = V _{CC} or GND		1.25	1.5	V
	Power-on Reset Voltage, V _{CC} Falling		0.8	1.15		V
Input SCL; Input/Output SDA						
V _{IL}	Low-Level Input Voltage				0.3×V _{CC}	V
V _{IH}	High-Level Input Voltage		0.7×V _{CC}			V
I _{OL}	Low-Level Output Current, SDA	V _{OL} = 0.4 V	3	8		mA
		V _{OL} = 0.6 V	6	9		mA
I _L	Leakage Current	V _I = V _{CC} or GND	−1		1	μA
C _i	Input Capacitance ⁽¹⁾	V _I = GND		15		pF
C _{io}	Input/Output Capacitance ⁽¹⁾	V _I = GND		15		pF
Select Inputs A0 to A2, RESET						
V _{IL}	Low-Level Input Voltage				0.3×V _{CC}	V
V _{IH}	High-Level Input Voltage		0.7×V _{CC}			V
I _{LI}	Input Leakage Current	V _I = V _{CC} or GND	−1		1	μA
C _i	Input Capacitance ⁽¹⁾	V _I = GND		3		pF
Pass Gate						
R _{on}	On-State Resistance	V _O = 0.4 V; I _O = 10 mA	10	34	70	Ω
V _{O(SW)}	Switch Output Voltage	V _{I(SW)} = V _{CC} = 1.8 V; I _{O(SW)} = −100 μA ⁽¹⁾		1.1		V
		V _{I(SW)} = V _{CC} = 1.65 V to 1.95 V; I _{O(SW)} = −100 μA	0.7		1.25	V

(1) Parameters are provided by the lab bench test and design simulation.

1.8-V 8-channel I²C Switch with Reset

All test conditions: $V_{CC} = 2.3\text{ V to }2.7\text{ V}$, $T_A = -40^{\circ}\text{C to }+125^{\circ}\text{C}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I _{DD}	Supply Current in Operating Mode ⁽¹⁾	No load; V _I = V _{CC} or GND; f _{SCL} = 100 kHz		1.3	5	μA
		No load; V _I = V _{CC} or GND; f _{SCL} = 400 kHz		4.3	10	μA
I _{stb}	Standby Current ⁽¹⁾	No load; V _I = V _{CC} or GND		0.3	1	μA
V _{POR}	Power-on Reset Voltage, V _{CC} Rising	No load; V _I = V _{CC} or GND		1.25	1.5	V
	Power-on Reset Voltage, V _{CC} Falling		0.8	1.15		V
Input SCL; Input/Output SDA						
V _{IL}	Low-Level Input Voltage				0.3×V _{CC}	V
V _{IH}	High-Level Input Voltage		0.7×V _{CC}			V
I _{OL}	Low-Level Output Current, SDA	V _{OL} = 0.4 V	6	14		mA
		V _{OL} = 0.6 V	10	19		mA
I _L	Leakage Current ⁽¹⁾	V _I = V _{CC} or GND	−1		1	μA
C _i	Input Capacitance ⁽¹⁾	V _I = GND		15		pF
C _{io}	Input/Output Capacitance ⁽¹⁾	V _I = GND		15		pF
Select Inputs A0 to A2, $\overline{\text{RESET}}$						
V _{IL}	Low-Level Input Voltage				0.3×V _{CC}	V
V _{IH}	High-Level Input Voltage		0.7×V _{CC}			V
I _{LI}	Input Leakage Current ⁽¹⁾	V _I = V _{CC} or GND	−1		1	μA
C _i	Input Capacitance ⁽¹⁾	V _I = GND		3		pF
Pass Gate						
R _{on}	On-State Resistance	V _O = 0.4 V; I _O = 10 mA	7	15	45	Ω
V _{O(SW)}	Switch Output Voltage	V _{I(SW)} = V _{CC} = 2.5 V; I _{O(SW)} = −100 μA ⁽¹⁾		1.5		V
		V _{I(SW)} = V _{CC} = 2.3 V to 2.7 V; I _{O(SW)} = −100 μA	1.1		2.0	V

(1) Parameters are provided by the lab bench test and design simulation.

1.8-V 8-channel I²C Switch with Reset

All test conditions: $V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $T_A = -40^{\circ}\text{C to }+125^{\circ}\text{C}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I _{DD}	Supply Current in Operating Mode ⁽¹⁾	No load; V _I = V _{CC} or GND; f _{SCL} = 100 kHz		2.2	8	μA
		No load; V _I = V _{CC} or GND; f _{SCL} = 400 kHz		7.3	16	μA
I _{stb}	Standby Current ⁽¹⁾	No load; V _I = V _{CC} or GND		0.5	2	μA
V _{POR}	Power-on Reset Voltage, V _{CC} Rising	No load; V _I = V _{CC} or GND		1.25	1.5	V
	Power-on Reset Voltage, V _{CC} Falling		0.8	1.15		V
Input SCL; Input/Output SDA						
V _{IL}	Low-Level Input Voltage				0.3×V _{CC}	V
V _{IH}	High-Level Input Voltage		0.7×V _{CC}			V
I _{OL}	Low-Level Output Current, SDA	V _{OL} = 0.4 V	6	20		mA
		V _{OL} = 0.6 V	10	27		mA
I _L	Leakage Current ⁽¹⁾	V _I = V _{CC} or GND	−1		1	μA
C _i	Input Capacitance ⁽¹⁾	V _I = GND		15		pF
C _{io}	Input/Output Capacitance ⁽¹⁾	V _I = GND		15		pF
Select Inputs A0 to A2, RESET						
V _{IL}	Low-Level Input Voltage				0.3×V _{CC}	V
V _{IH}	High-Level Input Voltage		0.7×V _{CC}			V
I _{LI}	Input Leakage Current ⁽¹⁾	V _I = V _{CC} or GND	−1		1	μA
C _i	Input Capacitance ⁽¹⁾	V _I = GND		3		pF
Pass Gate						
R _{on}	On-State Resistance	V _O = 0.4 V; I _O = 15 mA	5	12	30	Ω
V _{O(SW)}	Switch Output Voltage	V _{I(SW)} = V _{CC} = 3.3 V; I _{O(SW)} = −100 μA ⁽¹⁾		1.9		V
		V _{I(SW)} = V _{CC} = 3.0 V to 3.6 V; I _{O(SW)} = −100 μA	1.6		2.8	V

(1) Parameters are provided by the lab bench test and design simulation.

1.8-V 8-channel I²C Switch with Reset

All test conditions: $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^{\circ}\text{C to }+125^{\circ}\text{C}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I _{DD}	Supply Current in Operating Mode	No load; V _I = V _{CC} or GND; f _{SCL} = 100 kHz		5.2	15	μA
		No load; V _I = V _{CC} or GND; f _{SCL} = 400 kHz		17.2	30	μA
I _{stb}	Standby Current	No load; V _I = V _{CC} or GND		0.8	2	μA
V _{POR}	Power-on Reset Voltage, V _{CC} Rising	No load; V _I = V _{CC} or GND		1.25	1.5	V
	Power-on Reset Voltage, V _{CC} Falling		0.8	1.15		V
Input SCL; Input/Output SDA						
V _{IL}	Low-Level Input Voltage				0.3×V _{CC}	V
V _{IH}	High-Level Input Voltage		0.7×V _{CC}			V
I _{OL}	Low-Level Output Current, SDA	V _{OL} = 0.4 V	6	27		mA
		V _{OL} = 0.6 V	10	39		mA
I _L	Leakage Current	V _I = V _{CC} or GND	−1		1	μA
C _i	Input Capacitance ⁽¹⁾	V _I = GND		15		pF
C _{io}	Input/Output Capacitance ⁽¹⁾	V _I = GND		15		pF
Select Inputs A0 to A2, $\overline{\text{RESET}}$						
V _{IL}	Low-Level Input Voltage				0.3×V _{CC}	V
V _{IH}	High-Level Input Voltage		0.7×V _{CC}			V
I _{LI}	Input Leakage Current	V _I = V _{CC} or GND	−1		1	μA
C _i	Input Capacitance ⁽¹⁾	V _I = GND		3		pF
Pass Gate						
R _{on}	On-State Resistance	V _O = 0.4 V; I _O = 15 mA	4	10	20	Ω
V _{O(SW)}	Switch Output Voltage	V _{I(SW)} = V _{CC} = 5 V; I _{O(SW)} = −100 μA ⁽¹⁾		3.6		V
		V _{I(SW)} = V _{CC} = 4.5 V to 5.5 V; I _{O(SW)} = −100 μA	2.6		4.5	V

(1) Parameters are provided by the lab bench test and design simulation.

Electrical Characteristics - AC Parameters

I²C Interface Timing Requirements

All test conditions: within recommended operating free-air temperature range, unless otherwise noted.

Symbol	Description	Condition	I ² C Normal Mode		I ² C Fast Mode		Unit
			Min	Max	Min	Max	
f _{scl}	I ² C Clock Frequency		0	100	0	400	kHz
t _{sch}	I ² C Clock High Time		4		0.6		μs
t _{scl}	I ² C Clock Low Time		4.7		1.3		μs
t _{sp}	I ² C Spike Time			50		50	ns
t _{sdS}	I ² C Serial-Data Setup Time		250		100		ns
t _{sdh}	I ² C Serial-Data Hold Time		0		0		ns
t _{icr}	I ² C Input Rise Time			1000	20	300	ns
t _{icf}	I ² C Input Fall Time ⁽¹⁾			300	20 + 0.1C _b ⁽²⁾	300	ns
t _{ocf}	I ² C Output Fall Time ⁽¹⁾	10-pF to 400-pF bus		300	20 + 0.1C _b ⁽²⁾	300	ns
t _{buf}	I ² C Bus Free Time Between Stop and Start		4.7		1.3		μs
t _{sts}	I ² C Start or Repeated Start Condition Setup		4.7		0.6		μs
t _{sth}	I ² C Start or Repeated Start Condition Hold		4		0.6		μs
t _{sps}	I ² C Stop Condition Setup		4		0.6		μs
t _{vd(data)}	Valid Data Time	SCL low to SDA output valid		3.5		0.9	μs
t _{vd(ack)}	Valid Data Time of ACK Condition	ACK signal from SCL low to SDA (out) low		3.5		0.9	μs
t _{PD}	Propagation Delay ⁽³⁾	from SDA to SDx, or SCL to SCx		0.3		0.3	ns
C _b	I ² C Bus Capacitive Load ⁽²⁾			400		400	pF

(1) All the parameters in the above table are requested by I²C standard, not tested in production.

(2) C_b is the total capacitance of one bus line in pF.

(3) The propagation delay is calculated from the 20-Ω typical R_{on} and the 15-pF load capacitance.

Switching Characteristics

All test conditions: within recommended operating free-air temperature range, $C_L \leq 100$ pF, unless otherwise noted.

Symbol	Description	Condition	Min	Max	Unit
RESET Timing Requirements					
$t_{W(rst) L}$	Low-Level Reset Time	$V_{CC} = 1.65$ V to 5.5 V	6		ns
t_{rst}	Reset Time	SDA clear		500	ns
$t_{REC; STA}$	Recovery Time to Start Condition		0		ns

Parameter Measurement Waveforms

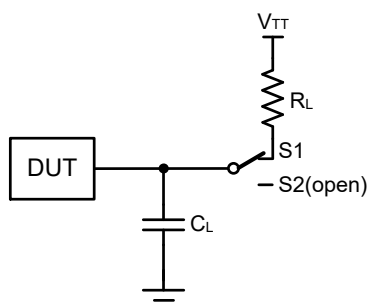


Figure 1. Load Circuit for Outputs

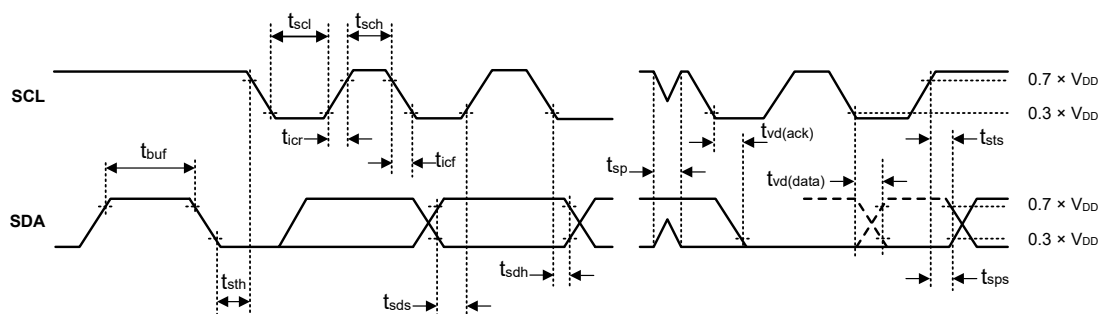


Figure 2. Definition of Timing on the I²C-bus

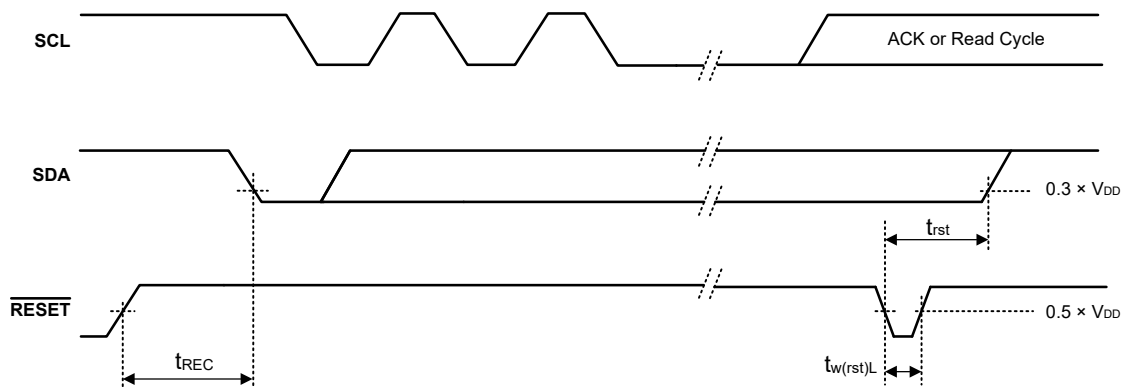


Figure 3. Definition of RESET Timing

Detailed Description

Overview

The TPT29548L-S is a 1:8 bidirectional translating I²C switch. The SCL/SDA upstream pair fans out to eight downstream channels. Any single SCn/SDn channel or combination of channels can be selected, determined by the programmable control register.

If one of the downstream I²C buses is stuck in a low state, then an active-low reset ($\overline{\text{RESET}}$) input helps the TPT29548L-S to recover. Pulling $\overline{\text{RESET}}$ low resets the I²C state machine and causes all the channels to be deselected, as the internal power-on reset function.

The pass gates of the switches are constructed so that the VCC terminal can be used to limit the maximum high voltage, which is passed by the TPT29548L-S and operates from 1.65 V to 5.5 V. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5-V tolerant.

Functional Block Diagram

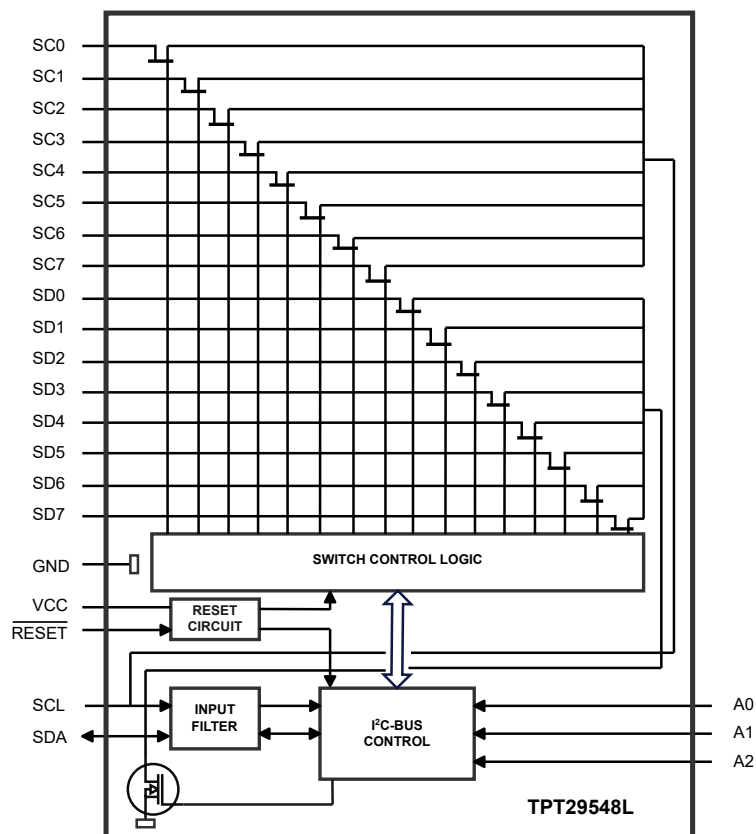


Figure 4. Functional Block Diagram

Feature Description

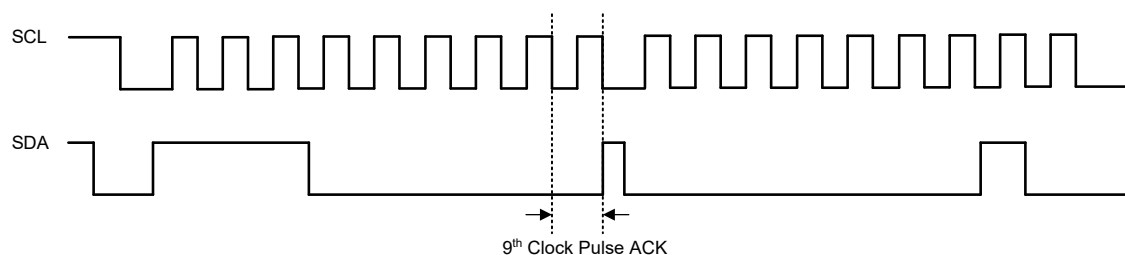


Figure 5. I²C Bus Waveform

Device Address

Following a START condition, the bus master must output the address to which the slave has access. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins, and they must be pulled HIGH or LOW. The address of the TPT29548L-S is shown below.

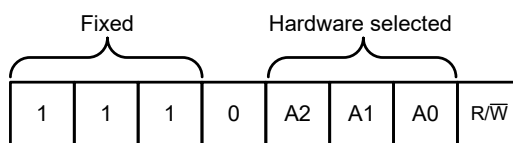


Figure 6. Slave Device Address

Control Register

Following the successful acknowledgment of the slave address, the bus master sends a byte to the TPT29548L-S, which is stored in the control register. If multiple bytes are received by the TPT29548L-S, it saves the last byte received. This register can be written and read via the I²C bus.

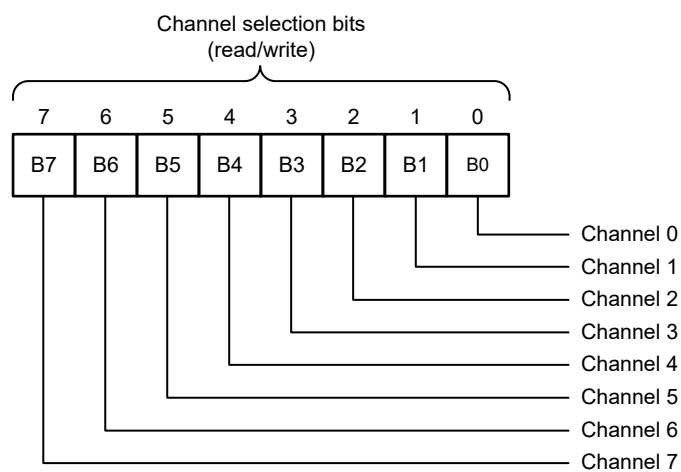


Figure 7. Control Register

Control Register Definition

One or several SCx/SDx downstream pairs, or channels, are selected by the contents of the control register. This register is written after the TPT29548L-S has been addressed. The control byte is used to determine which channel is to be selected. When a channel is selected, the channel becomes active after a STOP condition has been placed on the I²C bus. This ensures that all SCx/SDx lines are in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 2. Control Register: Write-Channel Selection; Read-Channel Status

B7	B6	B5	B4	B3	B2	B1	B0	Command
x	x	x	x	x	x	x	0	Channel 0 disable
x	x	x	x	x	x	x	1	Channel 0 enable
x	x	x	x	x	x	0	x	Channel 1 disable
x	x	x	x	x	x	1	x	Channel 1 enable
x	x	x	x	x	0	x	x	Channel 2 disable
x	x	x	x	x	1	x	x	Channel 2 enable
x	x	x	x	0	x	x	x	Channel 3 disable
x	x	x	x	1	x	x	x	Channel 3 enable
x	x	x	0	x	x	x	x	Channel 4 disable
x	x	x	1	x	x	x	x	Channel 4 enable
x	x	0	x	x	x	x	x	Channel 5 disable
x	x	1	x	x	x	x	x	Channel 5 enable
x	0	x	x	x	x	x	x	Channel 6 disable
x	1	x	x	x	x	x	x	Channel 6 enable
0	x	x	x	x	x	x	x	Channel 7 disable
1	x	x	x	x	x	x	x	Channel 7 enable

(1) Multiple channels can be enabled at the same time. Example: B7 = 0, B6 = 1, B5 = 0, B4 = 0, B3 = 1, B2 = 1, B1 = 0, B0 = 0, which means that channels 7, 5, 4, 1, and 0 are disabled and channels 6, 3, and 2 are enabled. Care should be taken not to exceed the maximum bus capacitance. The default condition is all zeroes.

Bus Transactions

The TPT29548L-S has only one register, which can be written by sending data directly after the target address, without the need to send a register address.

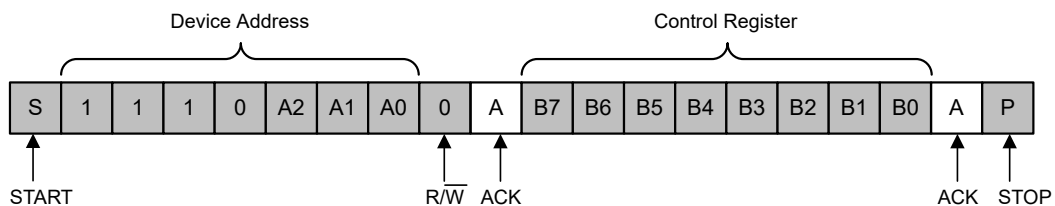
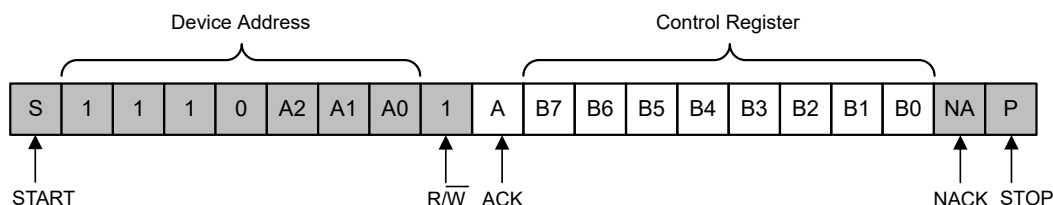


Figure 8. Write Control Register


Figure 9. Read Control Register

RESET Input

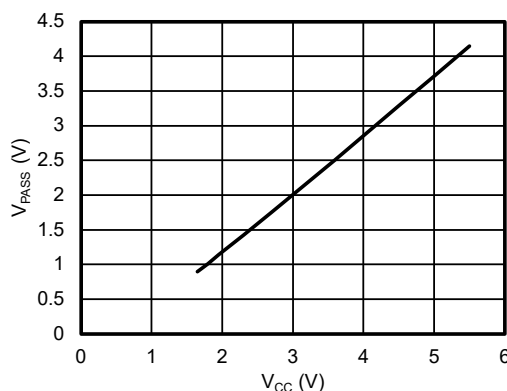
The $\overline{\text{RESET}}$ input is an active-low signal that helps recover from bus fault conditions. By pulling this signal LOW for at least $t_{w(\text{rst})L}$, the TPT29548L-S resets its register, I²C-bus state machine, and deselects all channels. The $\overline{\text{RESET}}$ input must be connected to the V_{CC} via a pull-up resistor.

Power-on Reset

When power is supplied to the V_{CC} pin, the TPT29548L-S remains in a reset state due to an internal power-on reset until V_{CC} reaches the V_{PORR} threshold. At that moment, the reset is lifted, and the registers of the device and I²C state machine are initialized to their default settings (all zeros), resulting in all channels being deselected. To reset the device again, V_{CC} must be decreased to below the V_{PORF} level.

Voltage Translation

For the TPT29548L-S to act as a voltage translator, the $V_{O(\text{sw})}$ voltage should be equal to or lower than the lowest bus voltage. $V_{O(\text{sw})}$ is the pass gate voltage (V_{pass}) of the switches. The pass gates of the switches are constructed so that the V_{CC} terminal can be used to limit the maximum high voltage, which is passed by the TPT29548L-S and operating from 1.65 V to 5.5 V. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5-V tolerant.


Figure 10. Pass Gate Voltage (V_{pass}) vs. Supply Voltage (V_{CC})

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT29548L-S can connect one I²C master device and eight target devices, and it can resolve address conflicts for the downstream channels.

Typical Application

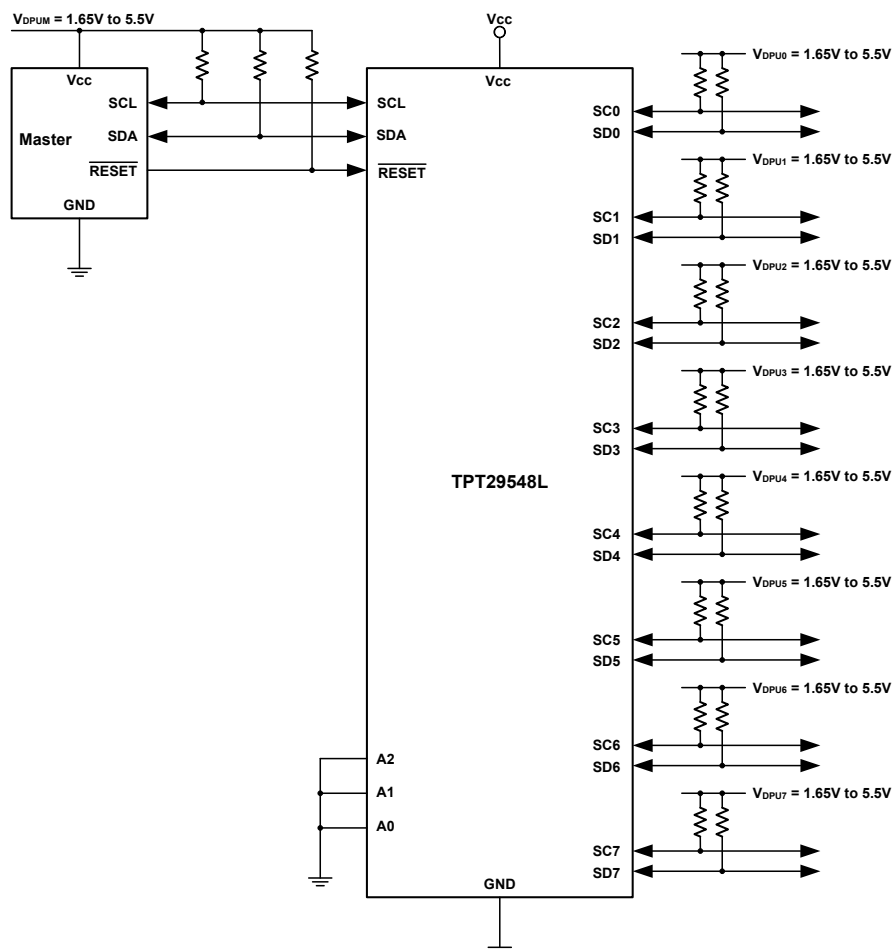


Figure 11. Typical Application Circuit

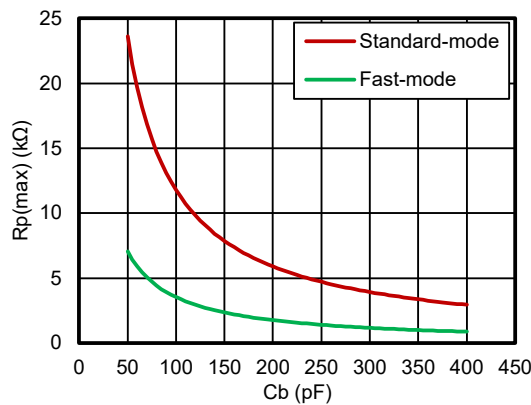
1.8-V 8-channel I²C Switch with Reset
Pull-Up Resistance

The minimum pull-up resistance is a function of V_{DPUX} , $V_{OL(max)}$, and I_{OL} .

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of t_r and C_b .

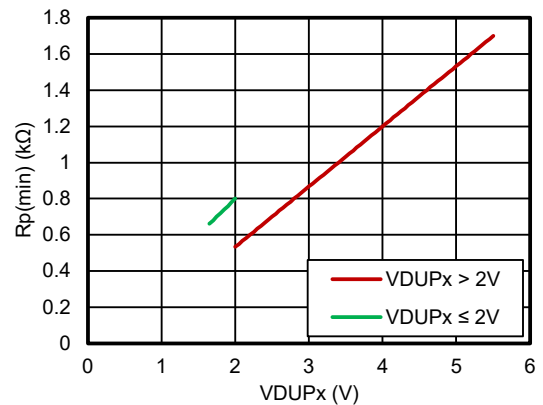
$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$



Standard-mode ($f_{scl} = 100$ kHz, $t_r = 1$ μs)

Fast-mode ($f_{scl} = 400$ kHz, $t_r = 300$ ns)

Figure 12. Maximum Pull-Up Resistance ($R_{p(max)}$) vs. Bus Capacitance (C_b)



$V_{OL} = 0.4$ V, $I_{OL} = 3$ mA when $V_{DPUX} > 2$ V

$V_{OL} = 0.2 \times V_{DPUX}$, $I_{OL} = 2$ mA when $V_{DPUX} \leq 2$ V

Figure 13. Maximum Pull-Up Resistance ($R_{p(max)}$) vs. Bus Capacitance (C_b)

Layout

Layout Example

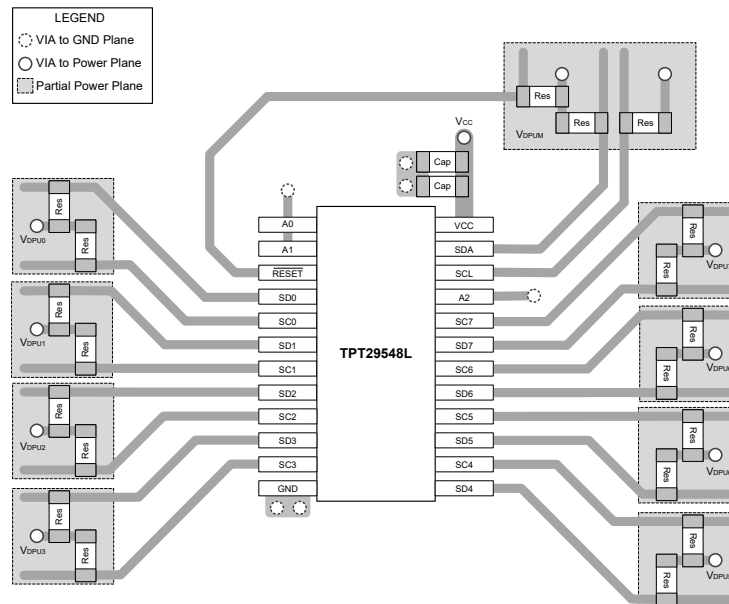
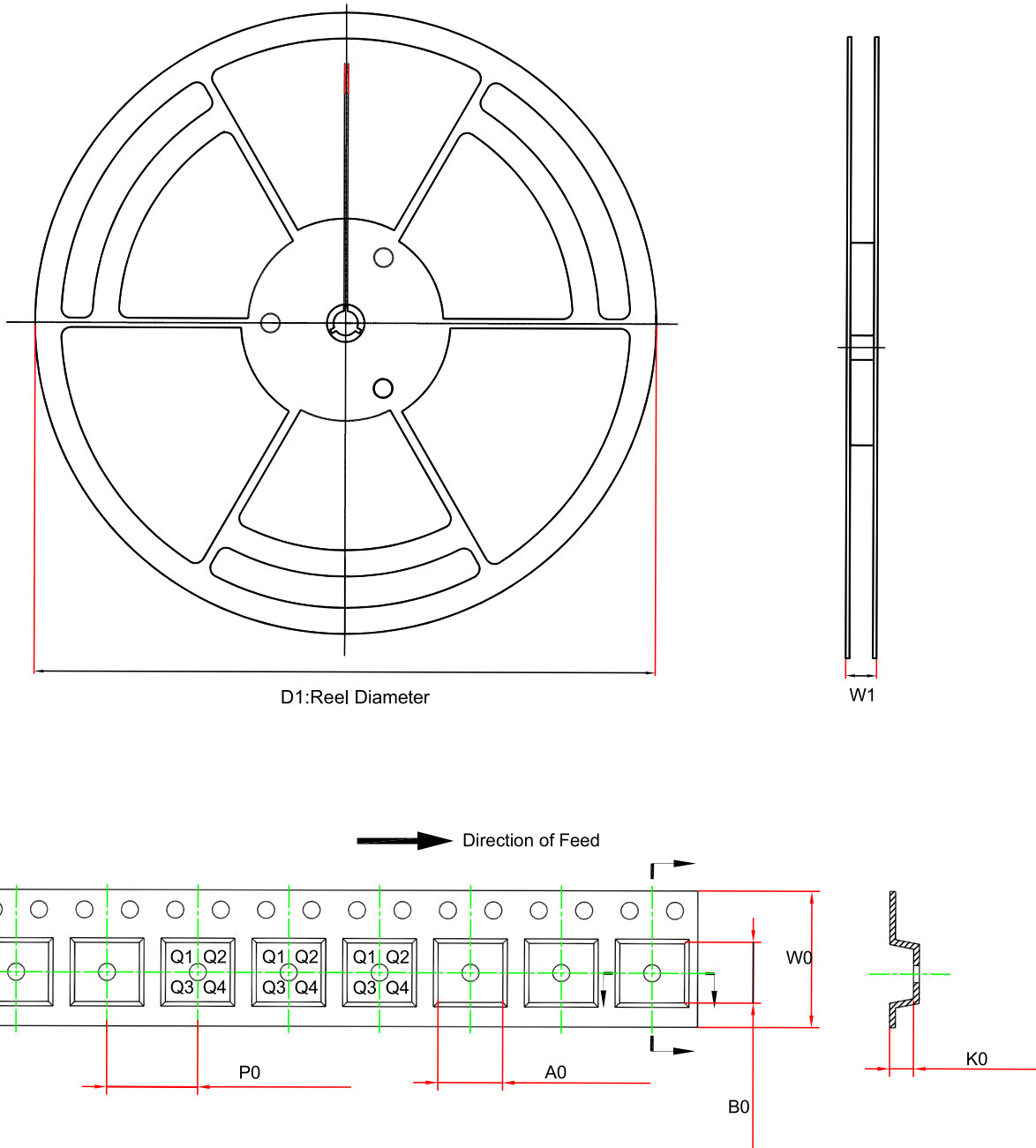


Figure 14. TPT29548L-S Layout Example

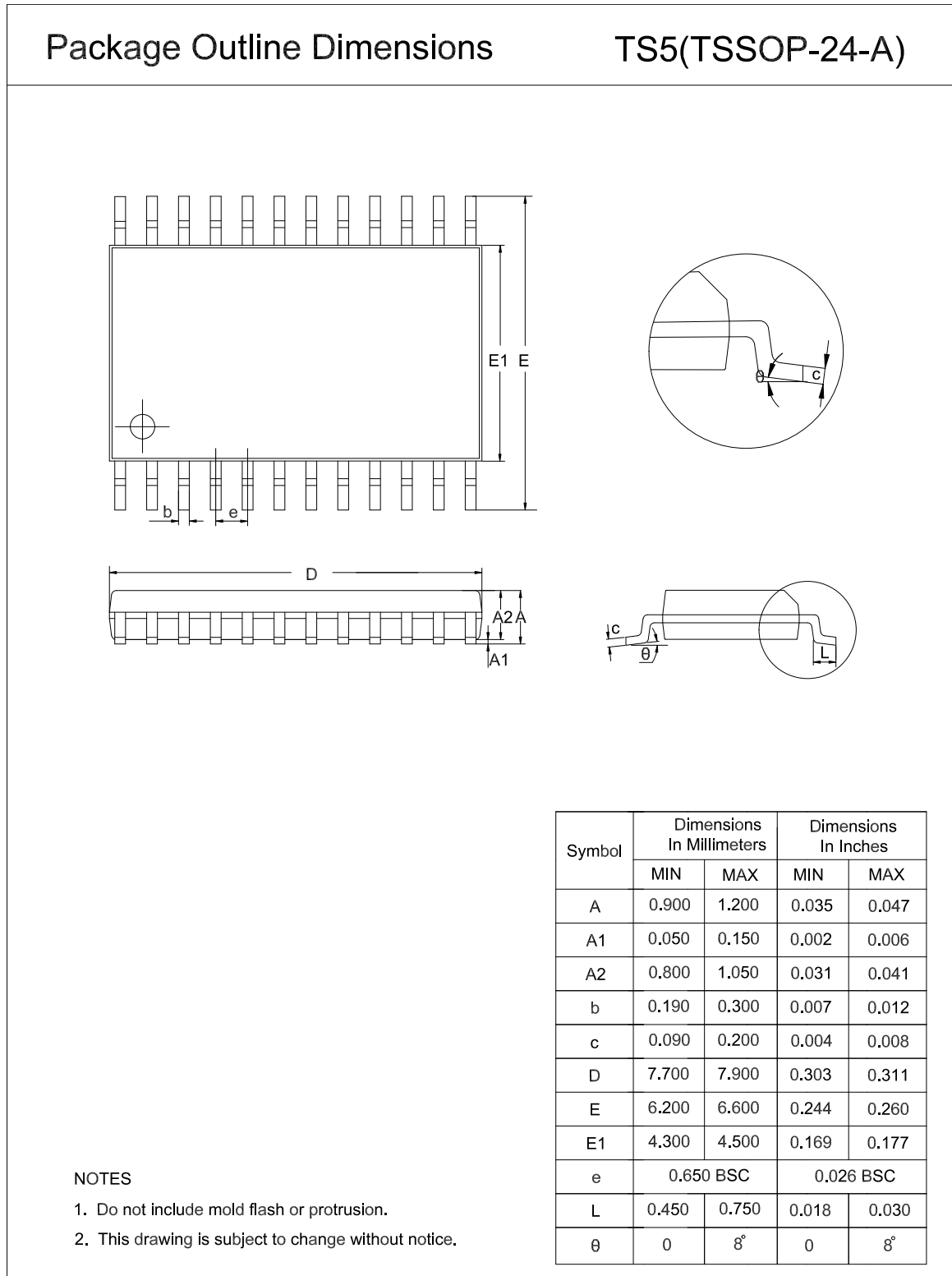
Tape and Reel Information

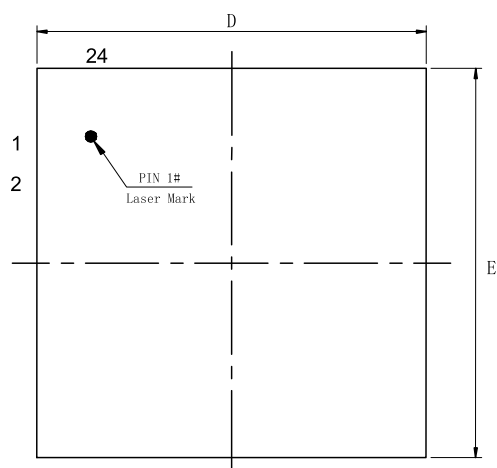
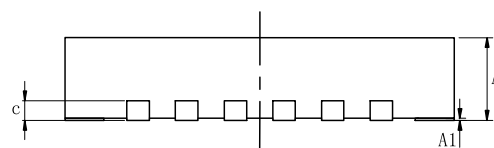
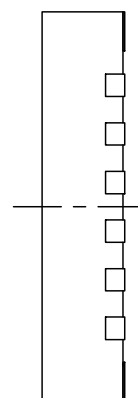
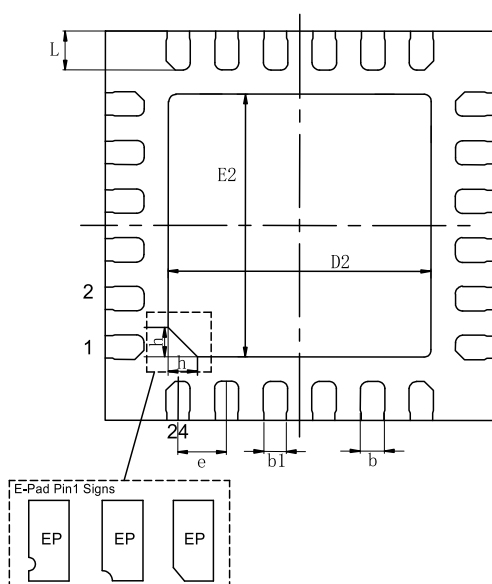


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT29548L-TS5R-S	TSSOP24	330	21.6	6.8	8.3	1.6	8	16	Q1
TPT29548L-FE2R-S	QFN4X4-24	330	17.6	4.3	4.3	1.1	8	12	Q2

Package Outline Dimensions

TSSOP24



QFN4X4-24
Package Outline Dimensions
FE2(QFN4X4-24-G)

TOP VIEW

SIDE VIEW

BOTTOM VIEW
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
b1	0.160 REF		0.006 REF	
c	0.180	0.250	0.007	0.010
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
e	0.500 BSC		0.020 BSC	
L	0.350	0.450	0.014	0.018
D2	2.150	2.350	0.085	0.093
E2	2.150	2.350	0.085	0.093
h	0.300	0.400	0.008	0.016

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29548L-TS5R-S	-40 to 125°C	TSSOP24	29548L	MSL3	Tape and Reel,4000	Green
TPT29548L-FE2R-S	-40 to 125°C	QFN4X4-24	29548L	MSL3	Tape and Reel,3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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