8-Channel I²C Switch with Reset

Features

- Bidirectional Translator of 1:8 I²C Switch
- Active-Low Reset Input
- Three Address Terminals, Allowing up to 8 Devices on the I²C Bus
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- Allows Voltage-Level Translation Between 2.5-V, 3.3-V, and 5-V Buses
- Support Standard Mode and Fast Mode I²C Devices，0 to 400-kHz Clock Frequency
- Low RON Switches
- Supports Hot Insertion
- Latch-Up Performance Exceeds 200 mA per JESD 78
- ESD Protection Exceeds JESD 22
  - 3.5-kV Human-Body Model
  - 1.5-kV Charged-Device Model

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products with I²C Slave Address Conflicts (e.g., Multiple, Identical Temp Sensors)

Description

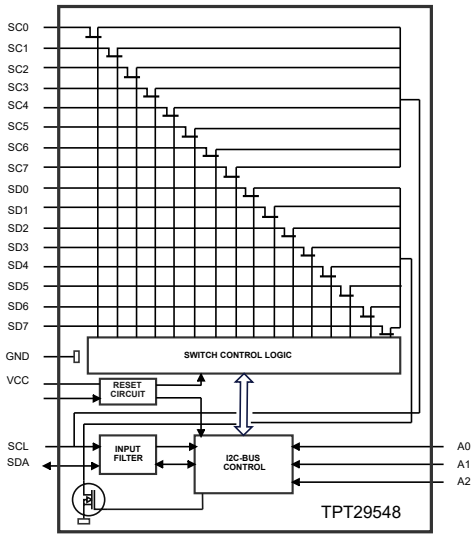
The TPT29548A is a 1:8 bidirectional translating I²C switch. The SCL/SDA upstream pair fans out to eight downstream channels. Any single SCn/SDn channel or combination of channels can be selected, determined by the programmable control register.

If one of the downstream I²C buses is stuck in a low state, then an active-low reset ($\overline{\text{RESET}}$) input helps the TPT29548A to recover. Pulling $\overline{\text{RESET}}$ low resets the I²C state machine and causes all the channels to be deselected, as the internal power-on reset function.

The pass gates of the switches are constructed so that the VCC terminal can be used to limit the maximum high voltage, which is passed by the TPT29548A. This allows the use of different bus voltages on each pair, so that 2.5-V or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5 V tolerant.

The TPT29548A is available in TSSOP24 and QFN24L packages, and is characterized from −40°C to +85°C.

Functional Block Diagram



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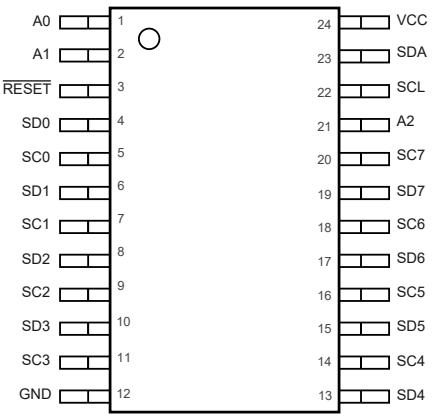
Revision History

Date	Revision	Notes
2022-02-21	Rev.A.0	Released version.
2022-07-08	Rev.A.1	Added the AC timing parameter of the I²C normal mode.
2024-03-04	Rev.B.1	Updated the part number in page 4 and the EC table in page 7.
2024-09-20	Rev.B.2	Added the hot insertion function in the Features.

Pin Configuration and Functions

TPT29548A
TSSOP24



TPT29548A
QFN4×4-24

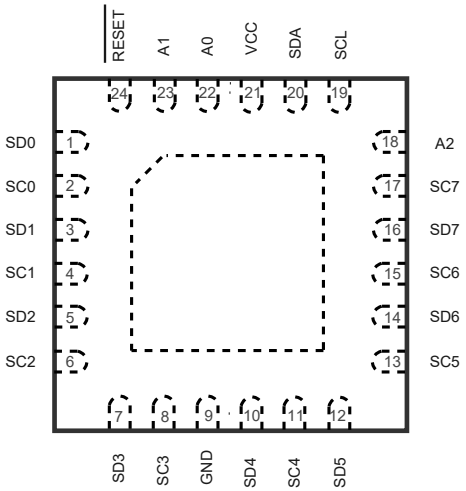


Table 1. Pin Functions

Pin No.		Name	I/O	Description
TSSOP24	DFN4×4-24			
1	22	A0	I	Address input 0. Connect directly to VCC or ground.
2	23	A1	I	Address input 1. Connect directly to VCC or ground.
3	24	$\overline{\text{RESET}}$	I	Reset input, active LOW. Connect to VCC or pull up the power of the master side through a pull-up resistor, if not used.
4	1	SD0	I/O	Data 0. Connect to the power of the slave channel 0 through a pull-up resistor.
5	2	SC0	I/O	Clock 0. Connect to the power of the slave channel 0 through a pull-up resistor.
6	3	SD1	I/O	Data 1. Connect to the power of the slave channel 1 through a pull-up resistor.
7	4	SC1	I/O	Clock 1. Connect to the power of the slave channel 1 through a pull-up resistor.
8	5	SD2	I/O	Data 2. Connect to the power of the slave channel 2 through a pull-up resistor.
9	6	SC2	I/O	Clock 2. Connect to the power of the slave channel 2 through a pull-up resistor.
10	7	SD3	I/O	Data 3. Connect to the power of the slave channel 3 through a pull-up resistor.
11	8	SC3	I/O	Clock 3. Connect to the power of the slave channel 3 through a pull-up resistor.
12	9	GND	GND	Ground.

Pin No.		Name	I/O	Description
TSSOP24	DFN4×4-24			
13	10	SD4	I/O	Data 4. Connect to the power of the slave channel 4 through a pull-up resistor.
14	11	SC4	I/O	Clock 4. Connect to the power of the slave channel 4 through a pull-up resistor.
15	12	SD5	I/O	Data 5. Connect to the power of the slave channel 5 through a pull-up resistor.
16	13	SC5	I/O	Clock 5. Connect to the power of the slave channel 5 through a pull-up resistor.
17	14	SD6	I/O	Data 6. Connect to the power of the slave channel 6 through a pull-up resistor.
18	15	SC6	I/O	Clock 6. Connect to the power of the slave channel 6 through a pull-up resistor.
19	16	SD7	I/O	Data 7. Connect to the power of the slave channel 7 through a pull-up resistor.
20	17	SC7	I/O	Clock 7. Connect to the power of the slave channel 7 through a pull-up resistor.
21	18	A2	I	Address input 2. Connect directly to VCC or ground.
22	19	SCL	I	Clock bus. Connect to VCC through a pull-up resistor.
23	20	SDA	I	Data bus. Connect to VCC through a pull-up resistor.
24	21	VCC	Supply	Supply voltage.
	25	Epad		For QFN package, the exposed thermal pad must be connected to ground.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	−0.5	7	V
V_I	Input Voltage	−0.5	7	V
I_{IK}	Input Clamp Current, $V_I < 0$		±20	mA
I_{OK}	Output Clamp Current, $V_O < 0$		±25	mA
I_{CC}	Continuous Current Through GND		±100	mA
T_J	Maximum Junction Temperature		125	°C
T_A	Operating Temperature Range	−45	85	°C
T_{STG}	Storage Temperature Range	−60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data is taken with the JEDEC low effective thermal conductivity test board.
(3) This data is taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	3.5	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter			Min	Max	Unit
V_{CC}	Supply Voltage		2.3	5.5	V
V_{IH}	High-Level Input Voltage	SCL, SDA	0.7 × V_{CC}	5.5	V
		A2~A0, $\overline{RESET}$	0.7 × V_{CC}	5.5	V
V_{IL}	Low-Level Input Voltage	SCL, SDA	−0.5	0.3 × V_{CC}	V
		A2~A0, $\overline{RESET}$	−0.5	0.3 × V_{CC}	V
T_A	Operating Temperature Range		−40	85	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP24	75	25	°C/W
QFN24	65	28	°C/W

Electrical Characteristics-DC Parameters

All test conditions: V_{CC} = 2.3 V to 3.6 V, T_A = −40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{DD}	Supply Current in Operating Mode	V_{CC} = 5.5 V; no load; V_I = V_{CC} or GND; f_{SCL} = 100 kHz		5	30	μA
		V_{CC} = 5.5 V; no load; V_I = V_{CC} or GND; f_{SCL} = 400 kHz		14	40	μA
I_{stb}	Standby Current	V_{CC} = 5.5 V; no load; V_I = V_{CC} or GND		1.8	3	μA
V_{POR}	Power-on Reset Voltage, V_{CC} Rising	No load; V_I = V_{CC} OR GND		1.25	1.45	V
	Power-on Reset Voltage, V_{CC} Falling		0.8	1.2		V
Input SCL; Input/Output SDA						
V_{IL}	Low-Level Input Voltage	V_{CC} = 5.5 V			0.3V_{CC}	V
V_{IH}	High-Level Input Voltage	V_{CC} = 5.5 V	0.7V_{CC}			V
I_{OL}	Low-Level Output Current, SDA	V_{CC} = 5.5 V, V_{OL} = 0.4 V	3			mA
	Low-Level Output Current, INT	V_{CC} = 5.5 V, V_{OL} = 0.6 V	3			mA
I_L	Leakage Current	V_I = V_{CC} or GND	−1	0.1	1	μA
C_i	Input Capacitance (1)	V_I = GND (1)		15		pF
Select Inputs A0 to A2, RESET						
V_{IL}	Low-Level Input Voltage	V_{CC} = 5.5 V			0.3V_{CC}	V
V_{IH}	Hig-Level Input Voltage	V_{CC} = 5.5 V	0.7V_{CC}			V
I_{LI}	Input Leakage Current	Pin at V_{CC} or GND	−1	0.1	1	μA
C_i	Input Capacitance (1)	V_I = GND (1)		3		pF
Pass Gate						
R_{on}	On-State Resistance	V_{CC} = 4.5 V to 5.5 V; V_O = 0.4 V; I_O = 15 mA	4	7	20	Ω
$V_{O\ (SW)}$	Switch Output Voltage (1)	$V_{I\ (SW)}$ = V_{CC} = 5.0 V; $I_{O\ (SW)}$ = −100 μA		3.55		V
		$V_{I\ (SW)}$ = V_{CC} = 4.5 V to 5.5 V; I = −100 μA	2.6		4.5	V
I_{LI}	Leakage Current	V_I = VCC or GND	−1	0.1	1	μA
C_{io}	Input/Output Capacitance (1)	V_I = GND		3		pF

(1) Parameters are provided by the lab bench test and design simulation.

All test conditions: V_{CC} = 4.5 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{DD}	Supply Current in Operating Mode	V_{CC} = 5.5 V; no load; V_I = V_{CC} or GND; f_{SCL} = 100 kHz		5	30	µA
		V_{CC} = 5.5 V; no load; V_I = V_{CC} or GND; f_{SCL} = 400 kHz		14	40	µA
I_{stb}	Standby Current	V_{CC} = 5.5 V; no load; V_I = V_{CC} or GND		1.8	3	µA
V_{POR}	Power-on Reset Voltage, V_{CC} Rising	No load; V_I = V_{CC} OR GND		1.25	1.45	V
	Power-on Reset Voltage, V_{CC} Falling		0.8	1.2		V
Input SCL; Input/Output SDA						
V_{IL}	Low-Level Input Voltage	V_{CC} = 5.5 V			0.3V_{CC}	V
V_{IH}	High-Level Input Voltage	V_{CC} = 5.5 V	0.7V_{CC}			V
I_{OL}	Low-Level Output Current, SDA	V_{CC} = 5.5 V, V_{OL} = 0.4 V	3			mA
	Low-Level Output Current, INT	V_{CC} = 5.5 V, V_{OL} = 0.6 V	6			mA
I_L	Leakage Current	V_I = V_{CC} or GND	−1	0.1	1	µA
C_i	Input Capacitance (1)	V_I = GND (1)		15		pF
Select Inputs A0 to A2, RESET						
V_{IL}	Low-Level Input Voltage	V_{CC} = 5.5 V			0.3V_{CC}	V
V_{IH}	Hig-Level Input Voltage	V_{CC} = 5.5 V	0.7V_{CC}			V
I_{LI}	Input Leakage Current	Pin at V_{CC} or GND	−1	0.1	1	µA
C_i	Input Capacitance (1)	V_I = GND (1)		3		pF
Pass Gate						
R_{on}	On-State Resistance	V_{CC} = 4.5 V to 5.5 V; V_O = 0.4 V; I_O = 15 mA	4	7	20	Ω
$V_{O\ (SW)}$	Switch Output Voltage (1)	$V_{I\ (SW)}$ = V_{CC} = 5.0 V; $I_{O\ (SW)}$ = −100 µA		3.55		V
		$V_{I\ (SW)}$ = V_{CC} = 4.5 V to 5.5 V; I = −100 µA	2.6		4.5	V
I_{LI}	Leakage Current	V_I = VCC or GND	−1	0.1	1	µA
C_{io}	Input/Output Capacitance (1)	V_I = GND		3		pF

(1) Parameters are provided by the lab bench test and design simulation.

Electrical Characteristics-AC Parameters

I²C Interface Timing Requirements

All test conditions: over recommended operating free-air temperature range, unless otherwise noted.

Symbol	Description	Condition	I²C Normal Mode		I²C BUS-Fast mode		Unit
			Min	Max	Min	Max	
fscl	I²C Clock Frequency		0	100	0	400	kHz
tsch	I²C Clock High Time		4		0.6		μs
tscl	I²C Clock Low Time		4.7		1.3		μs
tsp	I²C Spike Time			50		50	ns
tsds	I²C serial-data setup time		250		100		ns
tsdh	I²C Serial-Data Hold Time		0		0		ns
ticr	I²C Input Rise Time			1000	20	300	ns
ticf	I²C Input Fall Time (1)			300	20 + 0.1Cb	300	ns
tocf	I²C Output Fall Time (1)	10-pF to 400-pF bus		300	20 + 0.1Cb	300	ns
tbuf	I²C Bus Free Time Between Stop and Start		4.7		1.3		μs
tsts	I²C Start or Repeated Start Condition Setup		4.7		0.6		μs
tsth	I²C Start or Repeated Start Condition Hold		4		0.6		μs
tsps	I²C Stop Condition Setup		4		0.6		μs
tvd(data)	Valid Data Time	SCL low to SDA output valid		3.5		0.9	μs
tvd(ack)	Valid Data Time of ACK Condition	ACK signal from SCL low to SDA (out) low		3.5		0.9	μs
t_{PD}	Propagation Delay (2)	from SDA to SDx, or SCL to SCx		0.3		0.3	ns
Cb	I²C Bus Capacitive Load (1)			400		400	pF

(1) All the parameters in the above table are requested by I²C standard, NOT tested in production.
(2) Cb is the total capacitance of one bus line in pF.
(3) The propagation delay is calculated from the 20 typical Ron and the 15-pF load capacitance.

Switching Characteristics

All test conditions: over recommended operating free-air temperature range, $C_L \leq 100$ pF, unless otherwise noted.

Symbol	Description	Condition	Min	Max	Unit
$\overline{\text{RESET}}$ Timing Requirements					
$t_{w\ (rst)\ L}$	Low-Level Reset Time		4		ns
t_{rst}	Reset Time	SDA clear		500	ns
$t_{REC;\ STA}$	Recovery Time to Start Condition		0		ns

Parameter Measurement Waveforms

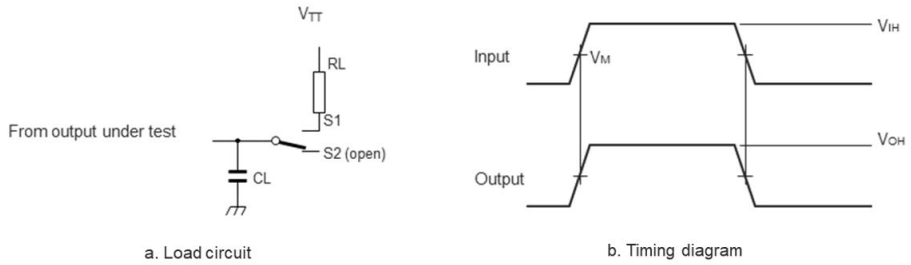


Figure 1. Load Circuit for Outputs

Detailed Description

Overview

The TPT29548A is a 1:8 bidirectional translating I²C switch. The SCL/SDA upstream pair fans out to eight downstream channels. Any single SCn/SDn channel or combination of channels can be selected, determined by the programmable control register.

If one of the downstream I²C buses is stuck in a low state, then an active-low reset ($\overline{\text{RESET}}$) input helps the TPT29548A to recover. Pulling $\overline{\text{RESET}}$ low resets the I²C state machine and causes all the channels to be deselected, as the internal power-on reset function.

The pass gates of the switches are constructed such that the VCC terminal can be used to limit the maximum high voltage, which is passed by the TPT29548A. This allows the use of different bus voltages on each pair, so that 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5 V tolerant.

The TPT29548A removes the reserved register 0×0C, and QFN4×4-24 pin 1 is in the Q2 quadrant.

Functional Block Diagram

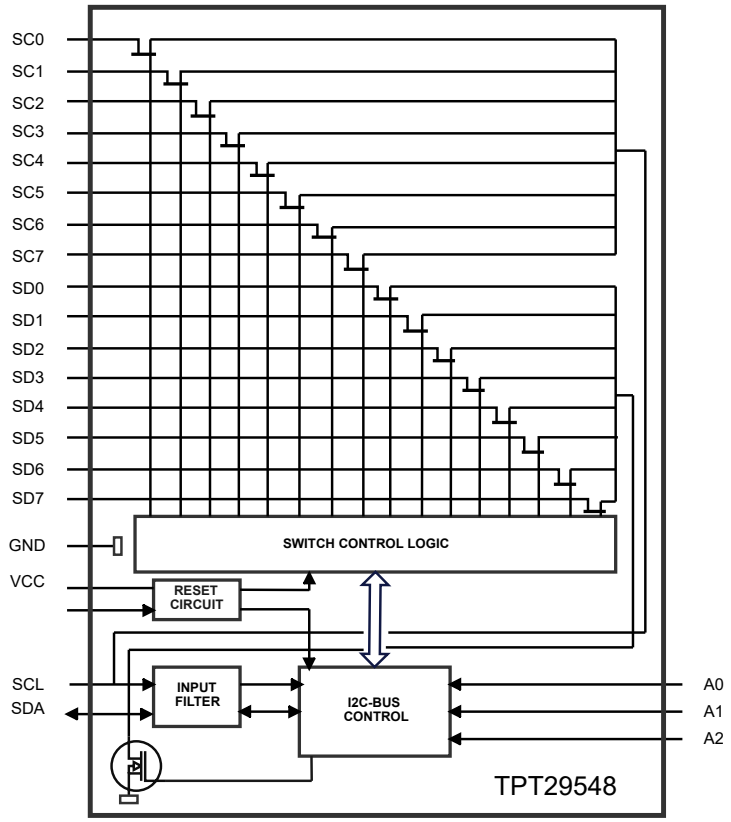


Figure 2. Functional Block Diagram

Feature Description

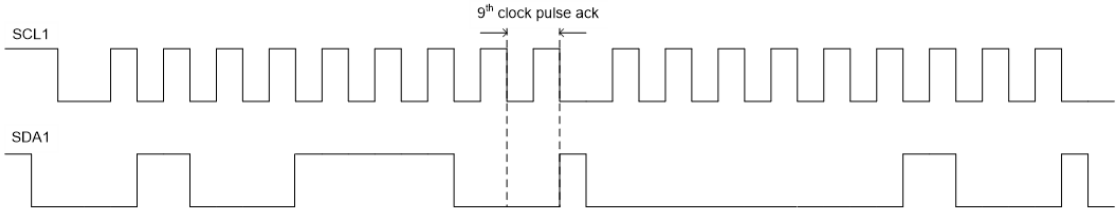


Figure 3. I²C Bus (2.3 V to 5.5 V) Waveform

Device Address

Following a START condition, the bus master must output the address of the slave it has access to. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins, and they must be pulled HIGH or LOW. The address of the TPT29548A is shown below.

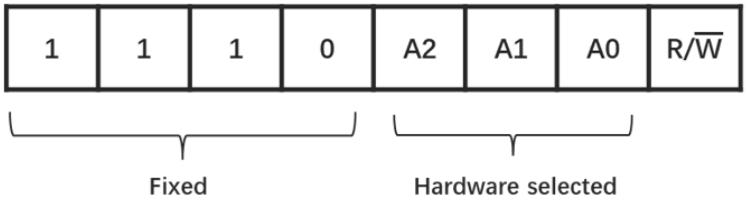


Figure 4. Slave Device Address

Control Register

Following the successful acknowledgment of the slave address, the bus master sends a byte to the TPT29548A, which is stored in the control register. If multiple bytes are received by the TPT29548A, it saves the last byte received. This register can be written and read via the I²C bus.

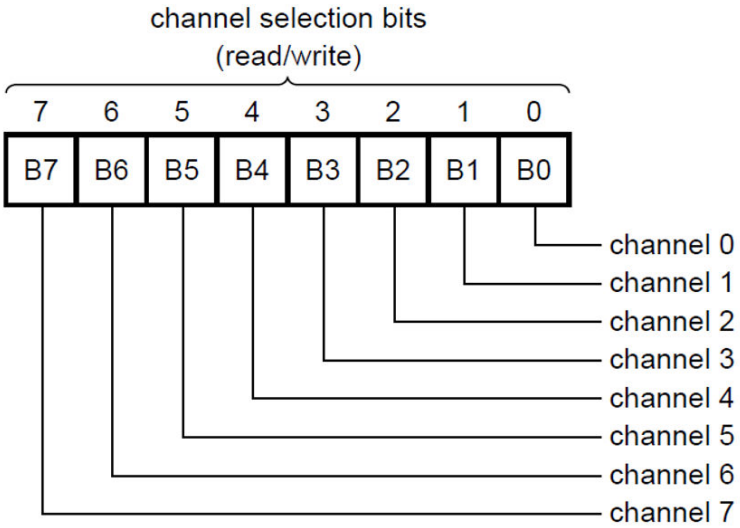


Figure 5. Control Register

Control Register Definition

One or several SCx/SDx downstream pairs, or channels, are selected by the contents of the control register. This register is written after the TPT29548A has been addressed. The 2 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel becomes active after a STOP condition has been placed on the I^2C bus. This ensures that all SCx/SDx lines are in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 2. Control Register: Write-Channel Selection; Read-Channel Status

B7	B6	B5	B4	B3	B2	B1	B0	Command
x	x	x	x	x	x	x	0	Channel 0 disable
x	x	x	x	x	x	x	1	Channel 0 enable
x	x	x	x	x	x	0	x	Channel 1 disable
x	x	x	x	x	x	1	x	Channel 1 enable
x	x	x	x	x	0	x	x	Channel 2 disable
x	x	x	x	x	1	x	x	Channel 2 enable
x	x	x	x	0	x	x	x	Channel 3 disable
x	x	x	x	1	x	x	x	Channel 3 enable
x	x	x	0	x	x	x	x	Channel 4 disable
x	x	x	1	x	x	x	x	Channel 4 enable
x	x	0	x	x	x	x	x	Channel 5 disable
x	x	1	x	x	x	x	x	Channel 5 enable
x	0	x	x	x	x	x	x	Channel 6 disable
x	1	x	x	x	x	x	x	Channel 6 enable
0	x	x	x	x	x	x	x	Channel 7 disable
1	x	x	x	x	x	x	x	Channel 7 enable

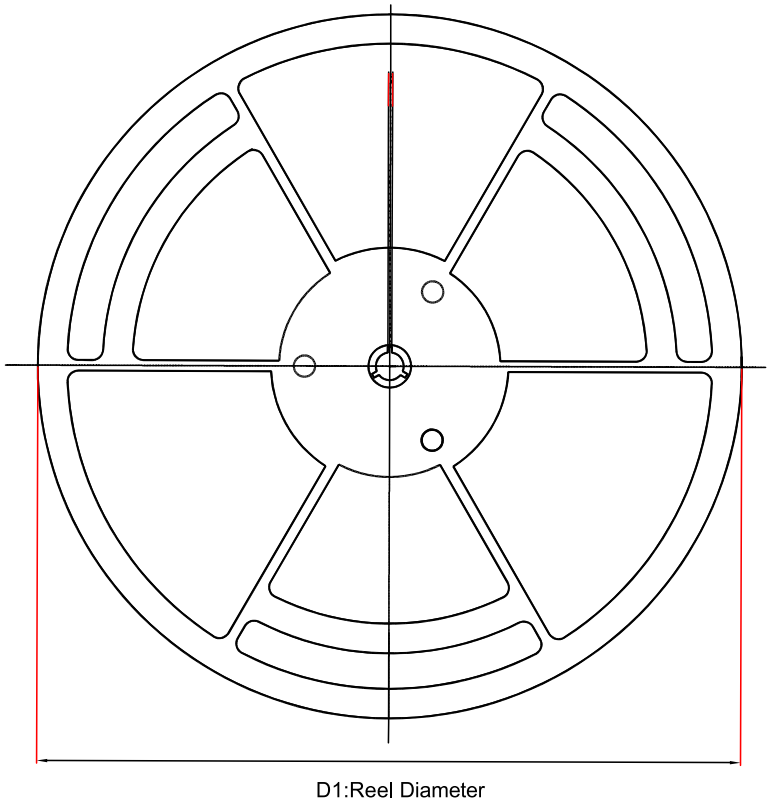
(1) Multiple channels can be enabled at the same time. Example: B7 = 0, B6 = 1, B5 = 0, B4 = 0, B3 = 1, B2 =1, B1 = 0, B0 = 0, which means that channels 7, 5, 4, 1, and 0 are disabled and channels 6, 3, and 2 are enabled. Care should be taken not to exceed the maximum bus capacitance. The default condition is all zeroes.

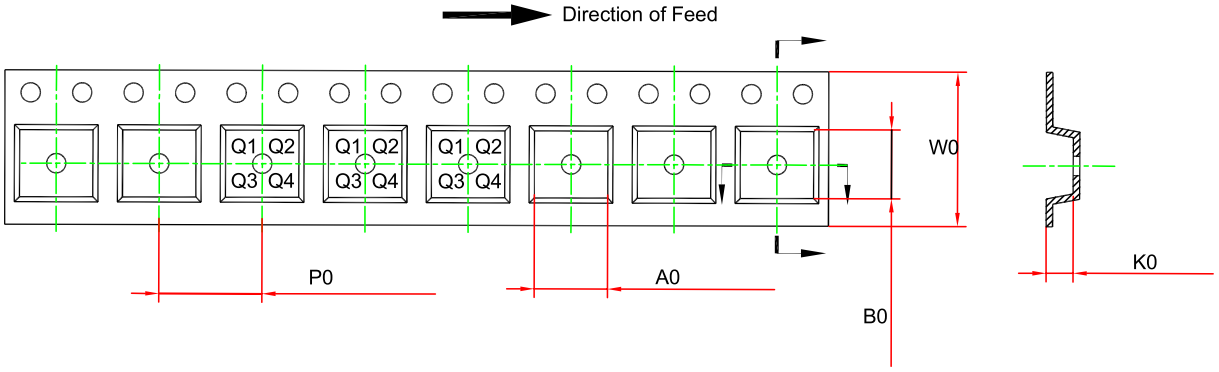
Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Tape and Reel Information



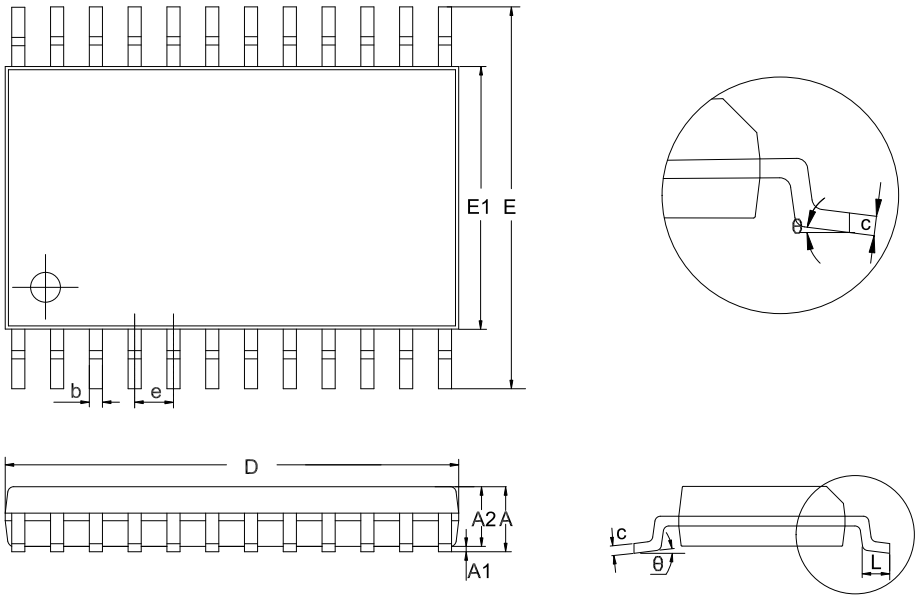


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT29548A-TS5R	TSSOP24	330	22.4	6.8	8.3	1.6	8	16	Q1
TPT29548A-QF8R	QFN24	330	17.6	4.3	4.3	1.1	8	12	Q2

Package Outline Dimensions

TSSOP24

Package Outline Dimensions TS5(TSSOP-24-A)



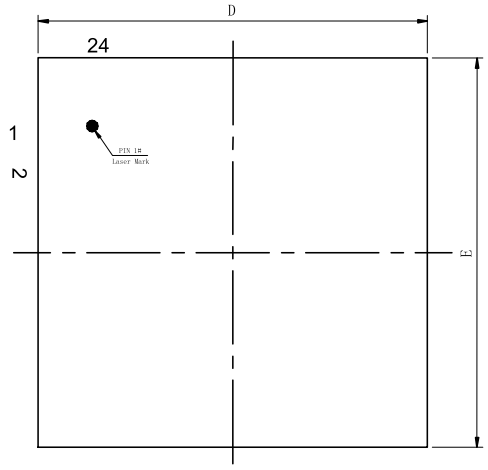
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	7.700	7.900	0.303	0.311
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

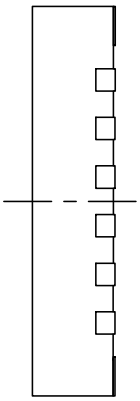
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

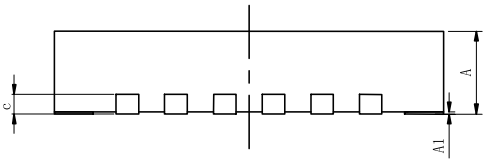
QFN4X4-24

Package Outline Dimensions QF8(QFN4X4-24-B)

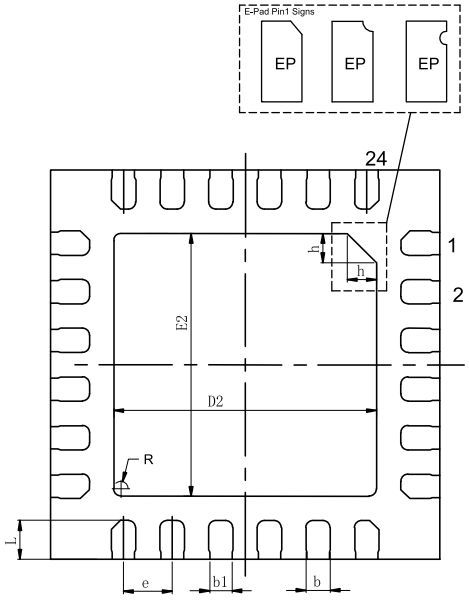


TOP VIEW





SIDE VIEW



BOTTOM VIEW

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
b1	0.160 REF		0.006 REF	
c	0.180	0.250	0.007	0.010
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
e	0.500 BSC		0.020 BSC	
L	0.350	0.450	0.014	0.018
D2	2.150	2.350	0.085	0.093
E2	2.150	2.350	0.085	0.093
h	0.300	0.400	0.008	0.016

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29548A-TS5R	−40 to 85°C	TSSOP24	9548A	3	Tape and Reel, 4000	Green
TPT29548A-QF8R	−40 to 85°C	QFN24	9548A	3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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