

Features

- Bidirectional Translator of 1:8 I²C Switch
- Active-Low Reset Input
- Three Address Terminals, Allowing up to 8 Devices on the I²C Bus
- Operating Power-Supply Voltage Range of 2.3 to 5.5 V
- Allows Voltage-Level Translation between 2.5-V, 3.3-V, and 5-V Buses
- Support Standard-Mode and Fast-Mode I²C Devices, 0 to 400-kHz Clock Frequency
- Low RON Switches
- Latch-up Performance Exceeds 200 mA per JESD 78
- ESD Protection Exceeds JESD 22
 - 3.5-kV Human Body Model
 - 1.5-kV Charged Device Model

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products with I²C Slave Address Conflicts (e.g., Multiple, Identical Temp Sensors)

Description

The TPT29548 is a 1:8 bidirectional translating I²C switch. The SCL/SDA upstream pair fans out to eight downstream channels. Any single SCn/SDn channel or combination of channels can be selected, which is determined by the programmable control register.

If one of the downstream I²C buses is stuck in a low state, an active-low reset (**RESET**) input helps the TPT29548 recover. Pulling **RESET** low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed so that the VCC terminal can be used to limit the maximum high voltage, which is passed by the TPT29548. This allows the use of different bus voltages on each pair, so that 2.5-V or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5-V tolerant.

The TPT29548 is available in the TSSOP24 and QFN4X4-24L package, and is characterized from -40°C to +85°C.

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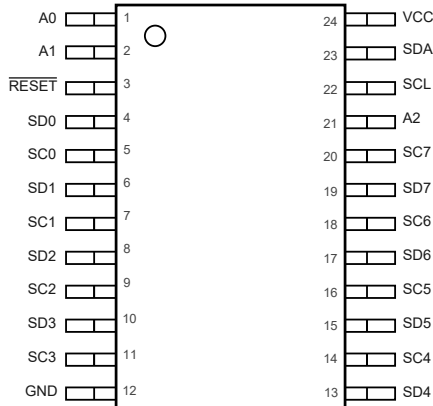
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Revision History

Date	Revision	Notes
2020-10-16	Rev.Pre.0	Initial version.
2020-12-09	Rev.Pre.1	Added the typical test data.
2021-01-18	Rev.Pre.2	Updated the TSSOP24 package information.
2021-02-04	Rev.Pre.3	Updated the electrical data.
2021-03-10	Rev.Pre.4	Updated the register description.
2021-06-15	Rev.A.0	Released version.
2021-08-27	Rev.B.0	Updated the symbol type error.
2022-02-17	Rev.B.1	Added the AC timing parameter of I ² C normal mode.
2022-04-25	Rev.B.2	Updated the pin1 quadrant as Q2.
2024-12-24	Rev.B.3	Updated to a new datasheet format. Updated the POD.

Pin Configuration and Functions

TPT29548
TSSOP24
Top View



TPT29548
DFN4X4-24L
Top View

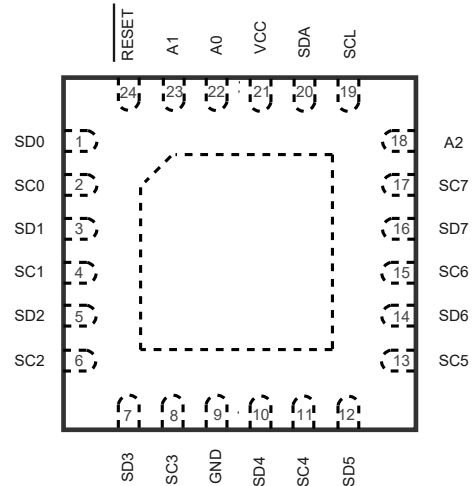


Table 1. Pin Functions

Pin No.		Name	I/O	Description
TSSOP24	DFN4X4-2 4L			
1	22	A0	Input	Address input 0. Connect directly to VCC or ground.
2	23	A1	Input	Address input 1. Connect directly to VCC or ground.
3	24	RESET	Input	Reset input, active LOW. Connect to VCC or pull up the power of the master side through a pull-up resistor, if not used.
4	1	SD0	I/O	Data 0. Connect to the power of slave channel 0 through a pull-up resistor.
5	2	SC0	I/O	Clock 0. Connect to the power of slave channel 0 through a pull-up resistor.
6	3	SD1	I/O	Data 1. Connect to the power of slave channel 1 through a pull-up resistor.
7	4	SC1	I/O	Clock 1. Connect to the power of slave channel 1 through a pull-up resistor.
8	5	SD2	I/O	Data 2. Connect to the power of slave channel 2 through a pull-up resistor.
9	6	SC2	I/O	Clock 2. Connect to the power of slave channel 2 through a pull-up resistor.
10	7	SD3	I/O	Data 3. Connect to the power of slave channel 3 through a pull-up resistor.

8-Channel I²C Switch with Reset

Pin No.		Name	I/O	Description
TSSOP24	DFN4X4-2 4L			
11	8	SC3	I/O	Clock 3. Connect to the power of slave channel 3 through a pull-up resistor.
12	9	GND	GND	Ground.
13	10	SD4	I/O	Data 4. Connect to the power of slave channel 4 through a pull-up resistor.
14	11	SC4	I/O	Clock 4. Connect to the power of slave channel 4 through a pull-up resistor.
15	12	SD5	I/O	Data 5. Connect to the power of slave channel 5 through a pull-up resistor.
16	13	SC5	I/O	Clock 5. Connect to the power of slave channel 5 through a pull-up resistor.
17	14	SD6	I/O	Data 6. Connect to the power of slave channel 6 through a pull-up resistor.
18	15	SC6	I/O	Clock 6. Connect to the power of slave channel 6 through a pull-up resistor.
19	16	SD7	I/O	Data 7. Connect to the power of slave channel 7 through a pull-up resistor.
20	17	SC7	I/O	Clock 7. Connect to the power of slave channel 7 through a pull-up resistor.
21	18	A2	Input	Address input 2. Connect directly to VCC or ground.
22	19	SCL	Input	Clock bus. Connect to VCC through a pull-up resistor.
23	20	SDA	Input	Data bus. Connect to VCC through a pull-up resistor.
24	21	VCC	Supply	Supply voltage.

Specifications

Absolute Maximum Ratings ⁽¹⁾

Parameter		Min	Max	Unit
V _{CC}	Supply Voltage	-0.5	7	V
V _I	Input Voltage	-0.5	7	V
I _{IK}	Input Clamp Current, V _I < 0	-20	20	mA
I _{OK}	Output Clamp Current, V _O < 0	-25	25	mA
I _{CC}	Continuous Current through GND	-100	100	mA
T _J	Maximum Junction Temperature		125	°C
T _A	Operating Temperature Range	-45	85	°C
T _{STG}	Storage Temperature	-60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) This data was taken with the JEDEC low effective thermal conductivity test board.

(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	3.5	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter			Min	Max	Unit
V _{CC}	Supply Voltage		2.3	5.5	V
V _{IH}	High-Level Input Voltage	SCL, SDA	0.7 × V _{CC}	5.5	V
		A2~A0, $\overline{\text{RESET}}$	0.7 × V _{CC}	5.5	V
V _{IL}	Low-Level Input Voltage	SCL, SDA	-0.5	0.3 × V _{CC}	V
		A2~A0, $\overline{\text{RESET}}$	-0.5	0.3 × V _{CC}	V
T _A	Operating Temperature Range		-40	85	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP24	75	25	°C/W
QFN4X4-24L	65	28	°C/W

8-Channel I²C Switch with Reset

Electrical Characteristics-DC Parameters

All test conditions: $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I _{DD}	Supply Current in Operating Mode	V _{CC} = 5.5 V; no load; V _I = V _{CC} or GND; f _{SCL} = 100 kHz		5	30	μA
		V _{CC} = 5.5 V; no load; V _I = V _{CC} or GND; f _{SCL} = 400 kHz		14	40	μA
I _{stb}	Standby Current	V _{CC} = 5.5 V; no load; V _I = V _{CC} or GND		1.8	3	μA
V _{POR}	Power-on Reset Voltage, V _{CC} Rising	No load; V _I = V _{CC} or GND		1.25	1.45	V
	Power-on Reset Voltage, V _{CC} Falling		0.8	1.2		V
Input SCL; Input/Output SDA						
V _{IL}	Low-Level Input Voltage	V _{CC} = 5.5 V			0.3V _{CC}	V
V _{IH}	High-Level Input Voltage	V _{CC} = 5.5 V	0.7V _{CC}			V
I _{OL}	Low-Level Output Current, SDA	V _{CC} = 5.5 V, V _{OL} = 0.4 V	3			mA
	Low-Level Output Current, INT	V _{CC} = 5.5 V, V _{OL} = 0.6 V	3			mA
I _L	Leakage Current	V _I = V _{CC} or GND	−1	0.1	1	μA
C _i	Input Capacitance	V _I = GND ⁽¹⁾		15		pF
Select Inputs A0 to A2, RESET						
V _{IL}	Low-Level Input Voltage	V _{CC} = 5.5 V			0.3V _{CC}	V
V _{IH}	High-Level Input Voltage	V _{CC} = 5.5 V	0.7V _{CC}			V
I _{LI}	Input Leakage Current	Pin at V _{CC} or GND	−1	0.1	1	μA
C _i	Input Capacitance	V _I = GND ⁽¹⁾		3		pF
Pass Gate						
R _{on}	On-State Resistance	V _{CC} = 4.5 V to 5.5 V; V _O = 0.4 V; I _O = 15 mA	4	7	20	Ω
V _{O (SW)}	Switch Output Voltage	V _{I(SW)} = V _{CC} = 5.0 V; I _{O(SW)} = −100 μA		3.55		V
		V _{I(SW)} = V _{CC} = 4.5 V to 5.5 V; I _{O(SW)} = −100 μA	2.6		4.5	V
I _L	Leakage Current	V _I = V _{CC} or GND	−1	0.1	1	μA
C _{io}	Input/Output Capacitance	V _I = GND		3		pF

(1) Parameters are provided by lab bench tests.

Electrical Characteristics-DC Parameters (Continued)

All test conditions: $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I _{DD}	Supply Current in Operating Mode	V _{CC} = 5.5 V; no load; V _I = V _{CC} or GND; f _{SCL} = 100 kHz		5	30	μA
		V _{CC} = 5.5 V; no load; V _I = V _{CC} or GND; f _{SCL} = 400 kHz		14	40	μA
I _{stb}	Standby Current	V _{CC} = 5.5 V; no load; V _I = V _{CC} or GND		1.8	3	μA
V _{POR}	Power-on Reset Voltage, V _{CC} Rising	No load; V _I = V _{CC} or GND		1.25	1.45	V
	Power-on Reset Voltage, V _{CC} Falling		0.8	1.2		V
Input SCL; Input/Output SDA						
V _{IL}	Low-Level Input Voltage	V _{CC} = 5.5 V			0.3V _{CC}	V
V _{IH}	High-Level Input Voltage	V _{CC} = 5.5 V	0.7V _{CC}			V
I _{OL}	Low-Level Output Current, SDA	V _{CC} = 5.5 V, V _{OL} = 0.4 V	3			mA
	Low-Level Output Current, INT	V _{CC} = 5.5 V, V _{OL} = 0.6 V	6			mA
I _L	Leakage Current	V _I = V _{CC} or GND	−1	0.1	1	μA
C _i	Input Capacitance ⁽¹⁾	V _I = GND ⁽¹⁾		15		pF
Select Inputs A0 to A2, RESET						
V _{IL}	Low-Level Input Voltage	V _{CC} = 5.5 V			0.3V _{CC}	V
V _{IH}	High-Level Input Voltage	V _{CC} = 5.5 V	0.7V _{CC}			V
I _{LI}	Input Leakage Current	Pin at V _{CC} or GND	−1	0.1	1	μA
C _i	Input Capacitance ⁽¹⁾	V _I = GND ⁽¹⁾		3		pF
Pass Gate						
R _{on}	On-State Resistance	V _{CC} = 4.5 V to 5.5 V; V _O = 0.4 V; I _O = 15 mA	4	7	20	Ω
V _{O (SW)}	Switch Output Voltage	V _{I(SW)} = V _{CC} = 5.0 V; I _{O(SW)} = −100 μA		3.55 ⁽¹⁾		V
		V _{I(SW)} = V _{CC} = 4.5 V to 5.5 V; I _{O(SW)} = −100 μA	2.6		4.5	V
I _L	Leakage Current	V _I = V _{CC} or GND	−1	0.1	1	μA
C _{io}	Input/Output Capacitance ⁽¹⁾	V _I = GND		3		pF

(1) Parameters are provided by lab bench tests.

Electrical Characteristics-AC Parameters

I²C Interface Timing Requirements

All test conditions: over recommended operating free-air temperature range, unless otherwise noted.

Symbol	Description	Condition	I ² C Normal Mode		I ² C BUS-Fast mode		Unit
			Min	Max	Min	Max	
f _{scl}	I ² C Clock Frequency		0	100	0	400	kHz
t _{sch}	I ² C Clock High Time		4		0.6		μs
t _{scl}	I ² C Clock Low Time		4.7		1.3		μs
t _{sp}	I ² C Spike Time			50		50	ns
t _{sd}	I ² C Serial-Data Setup Time		250		100		ns
t _{sdh}	I ² C Serial-Data Hold Time		10		0		ns
t _{icr}	I ² C Input Rise Time			1,000	20	300	ns
t _{icf}	I ² C Input Fall Time ⁽¹⁾			300	20 + 0.1Cb	300	ns
t _{ocf}	I ² C Output Fall Time ⁽¹⁾	10-pF to 400-pF bus		300	20 + 0.1Cb	300	ns
t _{buf}	I ² C Bus Free Time between Stop and Start		4.7		1.3		μs
t _{sts}	I ² C Start or Repeated Start Condition Setup		4.7		0.6		μs
t _{sth}	I ² C Start or Repeated Start Condition Hold		4		0.6		μs
t _{sp}	I ² C Stop Condition Setup		4		0.6		μs
t _{vd(data)}	Valid Data Time	SCL low to SDA output valid		3.5		0.9	μs
t _{vd(ack)}	Valid Data Time of ACK Condition	ACK signal from SCL low to SDA (out) low		3.5		0.9	μs
t _{PD}	Propagation Delay ⁽²⁾	From SDA to SDx, or SCL to SCx		0.3		0.3	ns
C _b	I ² C Bus Capacitive Load ⁽¹⁾			400		400	pF

(1) C_b is the total capacitance of one bus line in pF.

(2) The propagation delay is calculated from the 20 typical Ron and the 15-pF load capacitance.

Electrical Characteristics-AC Parameters (Continued)**Switching Characteristics**

All test conditions: over recommended operating free-air temperature range, $C_L \leq 100$ pF, unless otherwise noted.

Symbol	Description	Condition	Min	Max	Unit
Tvd; DAT	Data Valid Time	High to low		1	μ s
		Low to high		0.55	μ s
Tvd; DAT	Data Valid Time Acknowledge Time			1	ns
RESET					
$t_{w(rst) L}$	Low-Level Reset Time		4		ns
t_{rst}	Reset Time	SDA clear		500	ns
$t_{REC; STA}$	Recovery Time to Start Condition		0		ns

(1) Parameters are provided by lab bench tests and design simulation.

Parameter Measurement Waveforms

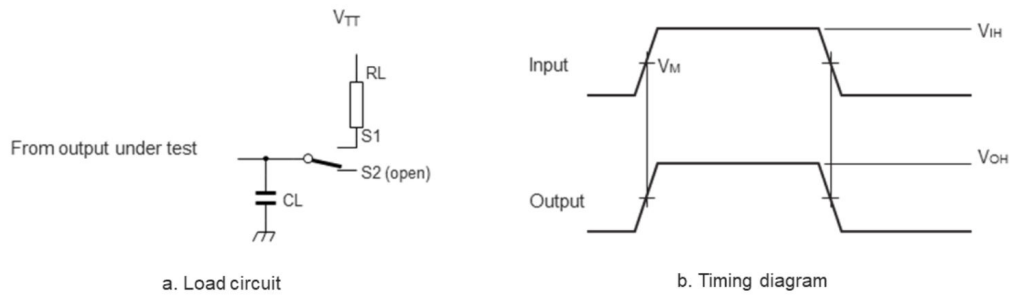


Figure 1. Load Circuit for Outputs

Detailed Description

Overview

The TPT29548 is a 16-bit GPIO expander with interrupt and weak pull-up resistors for I²C-bus applications. The power supply voltage range is from 1.65 V to 5.5 V and allows the TPT29548 to interconnect with 1.8-V microcontrollers.

Functional Block Diagram

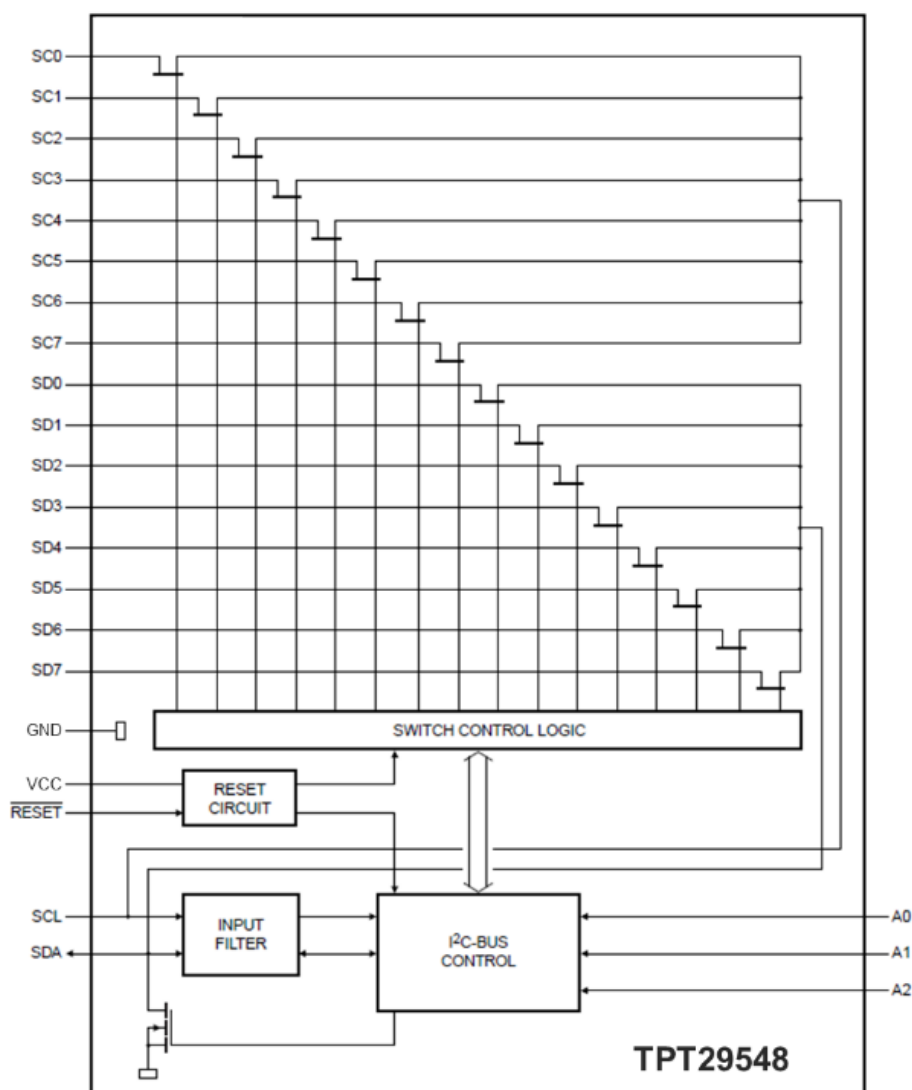


Figure 2. Functional Block Diagram

Feature Description

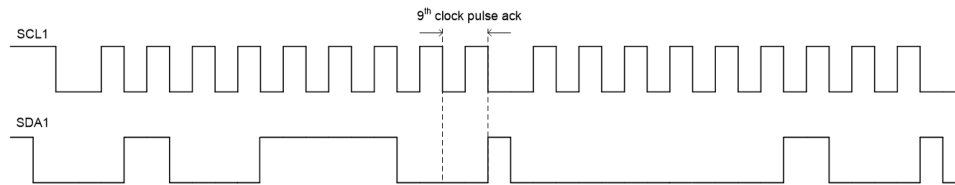


Figure 3. I²C Bus (2.3 V to 5.5 V) Waveform

Device Address

Following a START condition, the bus master must output the address of the slave it is accessing. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW. The address of the TPT29548 is shown as below.

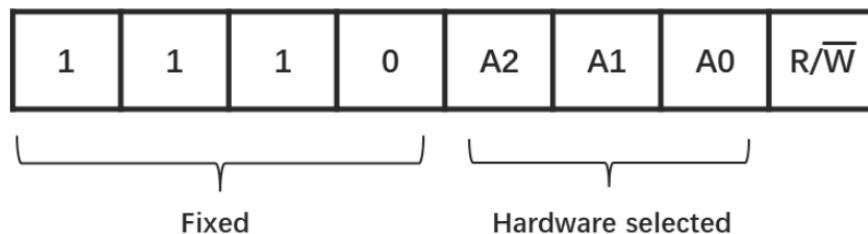


Figure 4. Slave Device Address

Control Register

Following the successful acknowledgment of the slave address, the bus master sends a byte to the TPT29548, which is stored in the control register. If multiple bytes are received by the TPT29548, it saves the last byte received. This register can be written and read via the I²C-bus.

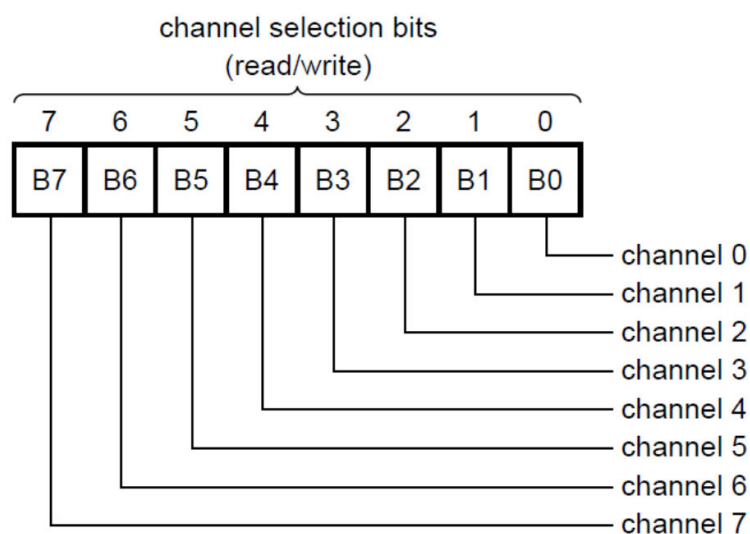


Figure 5. Control Register

Control Register Definition

One or several SCx/SDx downstream pair(s), or channel(s), are selected by the contents of the control register. This register is written after the TPT29548 has been addressed. The 2 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel becomes active after a STOP condition has been placed on the I²C-bus. This ensures that all SCx/SDx lines are in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 2. Control Register: Write-Channel Selection; Read-Channel Status

B7	B6	B5	B4	B3	B2	B1	B0	Command
x	x	x	x	x	x	x	0	Channel 0 disable
x	x	x	x	x	x	x	1	Channel 0 enable
x	x	x	x	x	x	0	x	Channel 1 disable
x	x	x	x	x	x	1	x	Channel 1 enable
x	x	x	x	x	0	x	x	Channel 2 disable
x	x	x	x	x	1	x	x	Channel 2 enable
x	x	x	x	0	x	x	x	Channel 3 disable
x	x	x	x	1	x	x	x	Channel 3 enable
x	x	x	0	x	x	x	x	Channel 4 disable
x	x	x	1	x	x	x	x	Channel 4 enable
x	x	0	x	x	x	x	x	Channel 5 disable
x	x	1	x	x	x	x	x	Channel 5 enable
x	0	x	x	x	x	x	x	Channel 6 disable
x	1	x	x	x	x	x	x	Channel 6 enable
0	x	x	x	x	x	x	x	Channel 7 disable
1	x	x	x	x	x	x	x	Channel 7 enable

(1) Multiple channels can be enabled at the same time. Example: B7 = 0, B6 = 1, B5 = 0, B4 = 0, B3 = 1, B2 = 1, B1 = 0, B0 = 0, means that channels 7, 5, 4, 1, and 0 are disabled while channels 6, 3, and 2 are enabled. The maximum bus capacitance should not be exceeded. Default condition is all zeroes.

Reserved Register

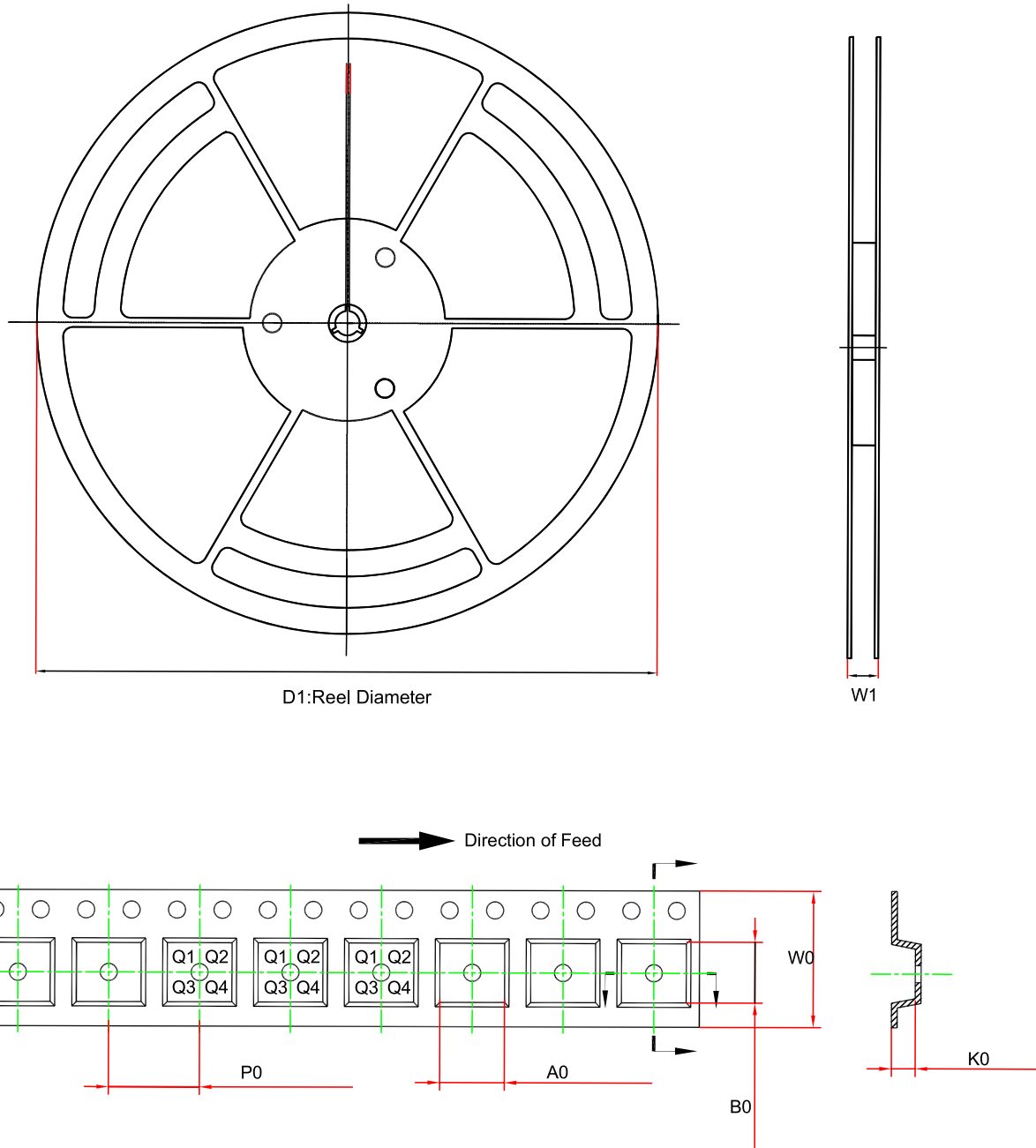
As part of the SMBUS function, the register 0X0C of the TPT29548 is reserved. Any operation of these registers is not suggested.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Tape and Reel Information

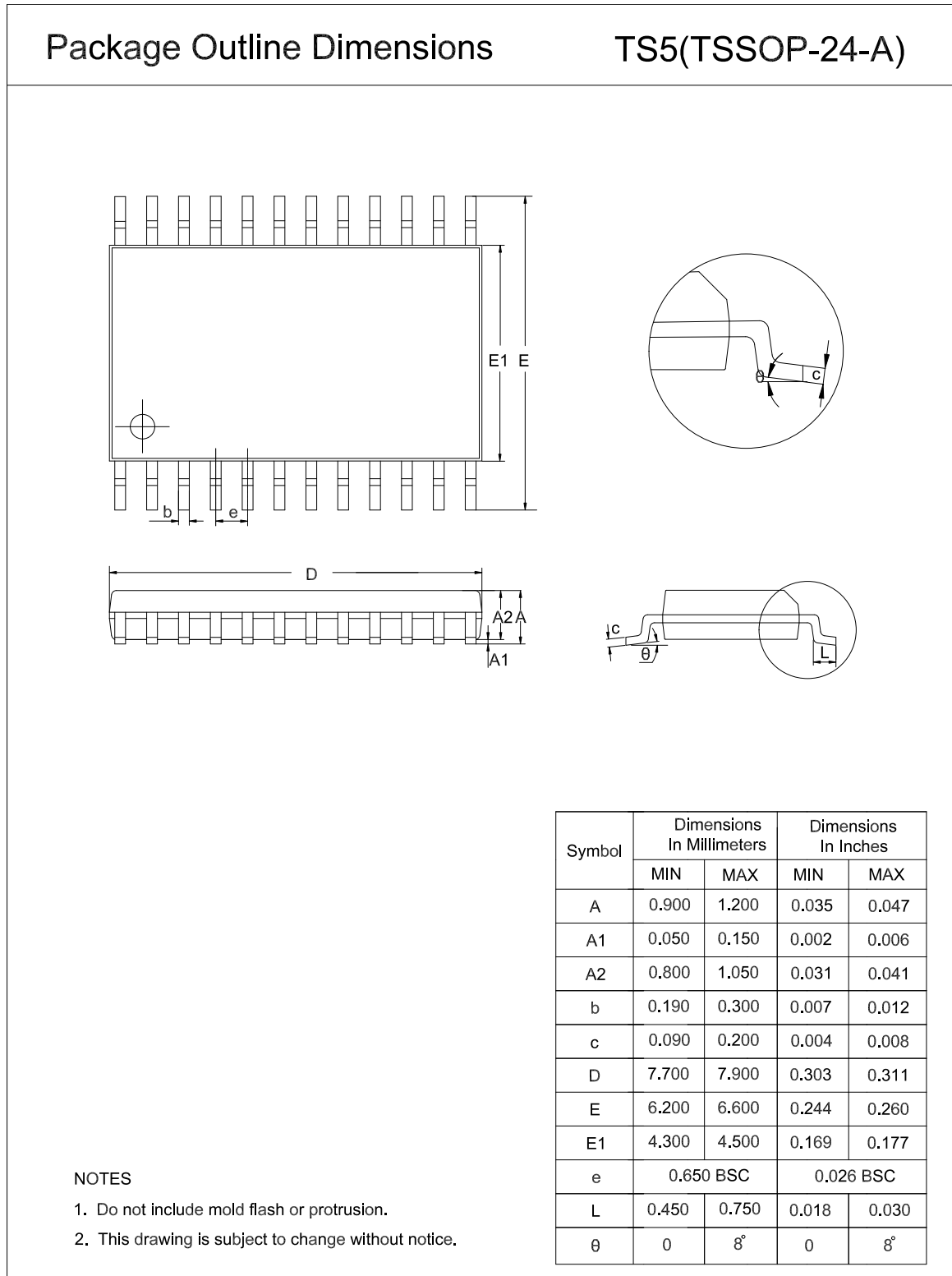


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) ⁽¹⁾	B0 (mm) ⁽¹⁾	K0 (mm) ⁽¹⁾	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT29548-TS5R	TSSOP23	330	22.4	6.8	8.3	1.6	8	16	Q1
TPT29548-QF8R	QFN4X4-24	330	17.6	4.3	4.3	1.1	8	12	Q1

(1) The value is for reference only. Contact the 3PEAK factory for more information.

Package Outline Dimensions

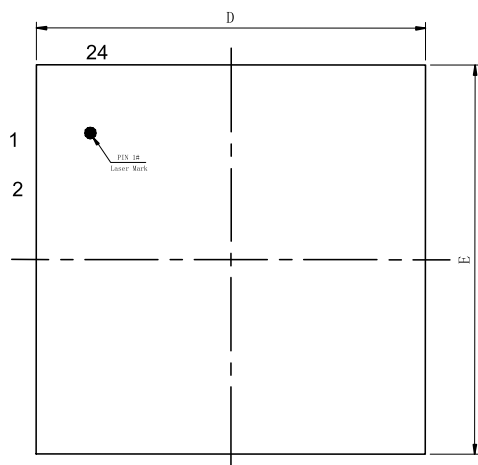
TSSOP24



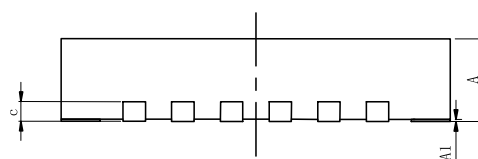
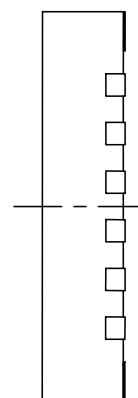
QFN4X4-24

Package Outline Dimensions

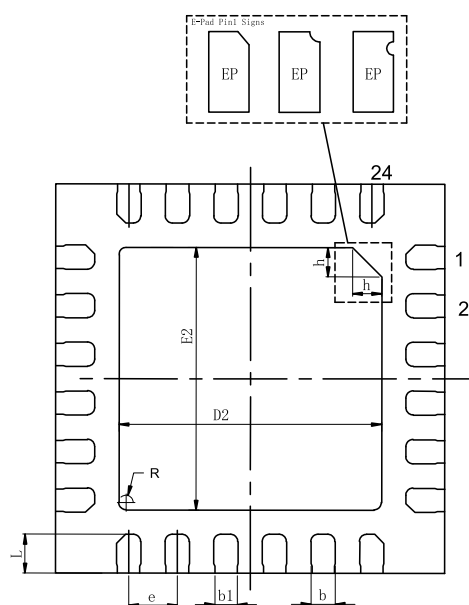
QF8(QFN4X4-24-A)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
b1	0.230 REF		0.009 REF	
c	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
e	0.500 BSC		0.020 BSC	
L	0.280	0.480	0.011	0.019
D2	2.600	2.800	0.102	0.110
E2	2.600	2.800	0.102	0.110
h	0.250	0.350	0.010	0.014

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29548-TS5R	-40 to 85°C	TSSOP24	29548	3	Tape and Reel, 4,000	Green
TPT29548-QF8R	-40 to 85°C	QFN4X4-24	29548	3	Tape and Reel, 3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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