1.8-V 4-channel I²C Switch with Reset

Features

- Bidirectional Translator of 1:4 I²C Switch
- Active-Low Reset Input
- Three Address Terminals, Allowing up to 8 Devices on the I²C Bus
- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- Allows Voltage-Level Translation among 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- Support Standard Mode and Fast Mode I²C Devices, 0 to 400-kHz Clock Frequency
- Low R_{on} Switches
- Supports Hot Insertion
- Latch-Up Performance Reaches 600 mA per JESD 78
- ESD Protection Exceeds JESD 22
  - 7.0-kV Human-Body Model
  - 1.5-kV Charged-Device Model

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products with I²C Slave Address Conflicts (e.g., Multiple, Identical Temp Sensors)

Description

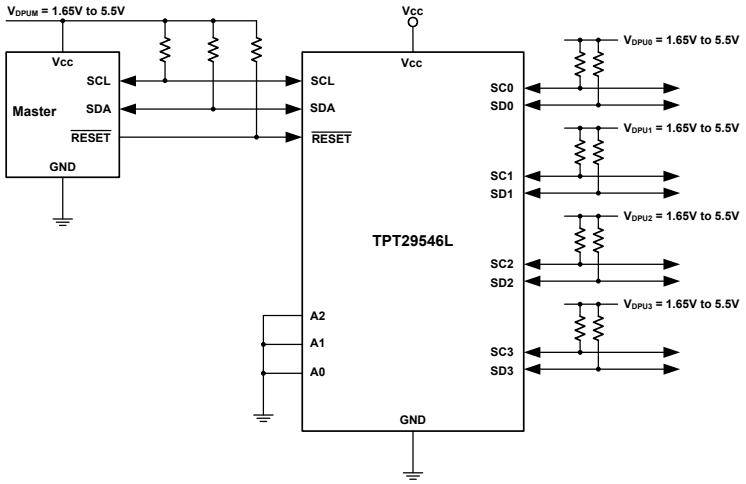
The TPT29546L is a 1:4 bidirectional translating I²C switch. The SCL/SDA upstream pair fans out to four downstream channels. Any single SCn/SDn channel or combination of channels can be selected, determined by the programmable control register.

If one of the downstream I²C buses is stuck in a low state, then an active-low reset ($\overline{RESET}$) input helps the TPT29546L to recover. Pulling $\overline{RESET}$ low resets the I²C state machine and causes all the channels to be deselected, as the internal power-on reset function.

The pass gates of the switches are constructed so that the V_{CC} terminal can be used to limit the maximum high voltage, which is passed by the TPT29546L and operates from 1.6 V to 5.5 V. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5-V tolerant.

The TPT29546L is available in the TSSOP16 package, and is characterized from −40°C to +125°C.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2025-10-21	Rev.A.0	Released version

Pin Configuration and Functions

TPT29546L
TSSOP16

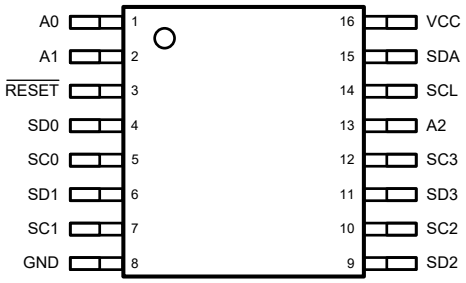


Table 1. Pin Functions

Pin No.	Name	I/O	Description
1	A0	I	Address input 0. Connect directly to V_{CC} or ground.
2	A1	I	Address input 1. Connect directly to V_{CC} or ground.
3	$\overline{\text{RESET}}$	I	Reset input, active LOW. Connect to V_{CC} or pull up the power of the master side through a pull-up resistor, if not used.
4	SD0	I/O	Data 0. Connect to the power of the slave channel 0 through a pull-up resistor.
5	SC0	I/O	Clock 0. Connect to the power of the slave channel 0 through a pull-up resistor.
6	SD1	I/O	Data 1. Connect to the power of the slave channel 1 through a pull-up resistor.
7	SC1	I/O	Clock 1. Connect to the power of the slave channel 1 through a pull-up resistor.
8	GND	GND	Ground.
9	SD2	I/O	Data 2. Connect to the power of the slave channel 2 through a pull-up resistor.
10	SC2	I/O	Clock 2. Connect to the power of the slave channel 2 through a pull-up resistor.
11	SD3	I/O	Data 3. Connect to the power of the slave channel 3 through a pull-up resistor.
12	SC3	I/O	Clock 3. Connect to the power of the slave channel 3 through a pull-up resistor.
13	A2	I	Address input 2. Connect directly to V_{CC} or ground.
14	SCL	I/O	Clock bus. Connect to VCC through a pull-up resistor.
15	SDA	I/O	Data bus. Connect to VCC through a pull-up resistor.
16	VCC	Supply	Supply voltage.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	−0.5	7	V
V_I	Input Voltage	−0.5	7	V
I_{IK}	Input Clamp Current, V_I < 0	−20	20	mA
I_{OK}	Output Clamp Current, V_O < 0	−25	25	mA
I_{CC}	Continuous Current Through GND	−100	100	mA
T_J	Maximum Junction Temperature		130	°C
T_A	Operating Temperature Range	−45	125	°C
T_{STG}	Storage Temperature Range	−60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter			Min	Max	Unit
V_{CC}	Supply Voltage		1.65	5.5	V
V_{IH}	High-Level Input Voltage	SCL, SDA	0.7 × V_{CC}	5.5	V
		A2~A0, $\overline{\text{RESET}}$	0.7 × V_{CC}	5.5	V
V_{IL}	Low-Level Input Voltage	SCL, SDA	−0.5	0.3 × V_{CC}	V
		A2~A0, $\overline{\text{RESET}}$	−0.5	0.3 × V_{CC}	V
T_A	Operating Temperature Range		−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP16	125	61	°C/W

Electrical Characteristics - DC Parameters

All test conditions: V_{CC} = 1.65 V to 1.95 V, T_A = −40°C to +125°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{DD}	Supply Current in Operating Mode	No load; V_I = V_{CC} or GND; f_{SCL} = 100 kHz		0.7	2	µA
		No load; V_I = V_{CC} or GND; f_{SCL} = 400 kHz		2.6	5	µA
I_{stb}	Standby Current	No load; V_I = V_{CC} or GND		0.2	1	µA
V_{POR}	Power-on Reset Voltage, V_{CC} Rising	No load; V_I = V_{CC} or GND		1.25	1.5	V
	Power-on Reset Voltage, V_{CC} Falling		0.8	1.15		V
Input SCL; Input/Output SDA						
V_{IL}	Low-Level Input Voltage				0.3×V_{CC}	V
V_{IH}	High-Level Input Voltage		0.7×V_{CC}			V
I_{OL}	Low-Level Output Current, SDA	V_{OL} = 0.4 V	3	8		mA
		V_{OL} = 0.6 V	6	9		mA
I_L	Leakage Current	V_I = V_{CC} or GND	−1		1	µA
C_i	Input Capacitance (1)	V_I = GND		15		pF
C_{io}	Input/Output Capacitance (1)	V_I = GND		15		pF
Select Inputs A0 to A2, $\overline{\text{RESET}}$						
V_{IL}	Low-Level Input Voltage				0.3×V_{CC}	V
V_{IH}	High-Level Input Voltage		0.7×V_{CC}			V
I_{LI}	Input Leakage Current	V_I = V_{CC} or GND	−1		1	µA
C_i	Input Capacitance (1)	V_I = GND		3		pF
Pass Gate						
R_{on}	On-State Resistance	V_O = 0.4 V; I_O = 10 mA	10	34	70	Ω
$V_{O\ (SW)}$	Switch Output Voltage	$V_{I\ (SW)}$ = V_{CC} = 1.8 V; $I_{O\ (SW)}$ = −100 µA (1)		1.1		V
		$V_{I\ (SW)}$ = V_{CC} = 1.65 V to 1.95 V; $I_{O\ (SW)}$ = −100 µA	0.7		1.25	V

(1) Parameters are provided by the lab bench test and design simulation.

All test conditions: V_{CC} = 2.3 V to 2.7 V, T_A = −40°C to +125°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{DD}	Supply Current in Operating Mode (1)	No load; V_I = V_{CC} or GND; f_{SCL} = 100 kHz		1.3	5	μA
		No load; V_I = V_{CC} or GND; f_{SCL} = 400 kHz		4.3	10	μA
I_{stb}	Standby Current (1)	No load; V_I = V_{CC} or GND		0.3	1	μA
V_{POR}	Power-on Reset Voltage, V_{CC} Rising	No load; V_I = V_{CC} or GND		1.25	1.5	V
	Power-on Reset Voltage, V_{CC} Falling		0.8	1.15		V
Input SCL; Input/Output SDA						
V_{IL}	Low-Level Input Voltage				0.3×V_{CC}	V
V_{IH}	High-Level Input Voltage		0.7×V_{CC}			V
I_{OL}	Low-Level Output Current, SDA	V_{OL} = 0.4 V	6	14		mA
		V_{OL} = 0.6 V	10	19		mA
I_L	Leakage Current (1)	V_I = V_{CC} or GND	−1		1	μA
C_i	Input Capacitance (1)	V_I = GND		15		pF
C_{io}	Input/Output Capacitance (1)	V_I = GND		15		pF
Select Inputs A0 to A2, $\overline{\text{RESET}}$						
V_{IL}	Low-Level Input Voltage				0.3×V_{CC}	V
V_{IH}	High-Level Input Voltage		0.7×V_{CC}			V
I_{LI}	Input Leakage Current (1)	V_I = V_{CC} or GND	−1		1	μA
C_i	Input Capacitance (1)	V_I = GND		3		pF
Pass Gate						
R_{on}	On-State Resistance	V_O = 0.4 V; I_O = 10 mA	7	15	45	Ω
$V_{O\ (SW)}$	Switch Output Voltage	$V_{I\ (SW)}$ = V_{CC} = 2.5 V; $I_{O\ (SW)}$ = −100 μA (1)		1.5		V
		$V_{I\ (SW)}$ = V_{CC} = 2.3 V to 2.7 V; $I_{O\ (SW)}$ = −100 μA	1.1		2.0	V

(1) Parameters are provided by the lab bench test and design simulation.

All test conditions: V_{CC} = 3.0 V to 3.6 V, T_A = −40°C to +125°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{DD}	Supply Current in Operating Mode (1)	No load; V_I = V_{CC} or GND; f_{SCL} = 100 kHz		2.2	8	μA
		No load; V_I = V_{CC} or GND; f_{SCL} = 400 kHz		7.3	16	μA
I_{stb}	Standby Current (1)	No load; V_I = V_{CC} or GND		0.5	2	μA
V_{POR}	Power-on Reset Voltage, V_{CC} Rising	No load; V_I = V_{CC} or GND		1.25	1.5	V
	Power-on Reset Voltage, V_{CC} Falling		0.8	1.15		V
Input SCL; Input/Output SDA						
V_{IL}	Low-Level Input Voltage				0.3×V_{CC}	V
V_{IH}	High-Level Input Voltage		0.7×V_{CC}			V
I_{OL}	Low-Level Output Current, SDA	V_{OL} = 0.4 V	6	20		mA
		V_{OL} = 0.6 V	10	27		mA
I_L	Leakage Current (1)	V_I = V_{CC} or GND	−1		1	μA
C_i	Input Capacitance (1)	V_I = GND		15		pF
C_{io}	Input/Output Capacitance (1)	V_I = GND		15		pF
Select Inputs A0 to A2, $\overline{\text{RESET}}$						
V_{IL}	Low-Level Input Voltage				0.3×V_{CC}	V
V_{IH}	High-Level Input Voltage		0.7×V_{CC}			V
I_{LI}	Input Leakage Current (1)	V_I = V_{CC} or GND	−1		1	μA
C_i	Input Capacitance (1)	V_I = GND		3		pF
Pass Gate						
R_{on}	On-State Resistance	V_O = 0.4 V; I_O = 15 mA	5	12	30	Ω
$V_{O\ (SW)}$	Switch Output Voltage	$V_{I\ (SW)}$ = V_{CC} = 3.3 V; $I_{O\ (SW)}$ = −100 μA (1)		1.9		V
		$V_{I\ (SW)}$ = V_{CC} = 3.0 V to 3.6 V; $I_{O\ (SW)}$ = −100 μA	1.6		2.8	V

(1) Parameters are provided by the lab bench test and design simulation.

All test conditions: V_{CC} = 4.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{DD}	Supply Current in Operating Mode	No load; V_I = V_{CC} or GND; f_{SCL} = 100 kHz		5.2	15	µA
		No load; V_I = V_{CC} or GND; f_{SCL} = 400 kHz		17.2	30	µA
I_{stb}	Standby Current	No load; V_I = V_{CC} or GND		0.8	2	µA
V_{POR}	Power-on Reset Voltage, V_{CC} Rising	No load; V_I = V_{CC} or GND		1.25	1.5	V
	Power-on Reset Voltage, V_{CC} Falling		0.8	1.15		V
Input SCL; Input/Output SDA						
V_{IL}	Low-Level Input Voltage				0.3×V_{CC}	V
V_{IH}	High-Level Input Voltage		0.7×V_{CC}			V
I_{OL}	Low-Level Output Current, SDA	V_{OL} = 0.4 V	6	27		mA
		V_{OL} = 0.6 V	10	39		mA
I_L	Leakage Current	V_I = V_{CC} or GND	−1		1	µA
C_i	Input Capacitance (1)	V_I = GND		15		pF
C_{io}	Input/Output Capacitance (1)	V_I = GND		15		pF
Select Inputs A0 to A2, $\overline{\text{RESET}}$						
V_{IL}	Low-Level Input Voltage				0.3×V_{CC}	V
V_{IH}	High-Level Input Voltage		0.7×V_{CC}			V
I_{LI}	Input Leakage Current	V_I = V_{CC} or GND	−1		1	µA
C_i	Input Capacitance (1)	V_I = GND		3		pF
Pass Gate						
R_{on}	On-State Resistance	V_O = 0.4 V; I_O = 15 mA	4	10	20	Ω
$V_{O\ (SW)}$	Switch Output Voltage	$V_{I\ (SW)}$ = V_{CC} = 5 V; $I_{O\ (SW)}$ = −100 µA (1)		3.6		V
		$V_{I\ (SW)}$ = V_{CC} = 4.5 V to 5.5 V; $I_{O\ (SW)}$ = −100 µA	2.6		4.5	V

(1) Parameters are provided by the lab bench test and design simulation.

Electrical Characteristics - AC Parameters

I²C Interface Timing Requirements

All test conditions: within recommended operating free-air temperature range, unless otherwise noted.

Symbol	Description	Condition	I²C Normal Mode		I²C Fast Mode		Unit
			Min	Max	Min	Max	
f_{scl}	I²C Clock Frequency		0	100	0	400	kHz
t_{sch}	I²C Clock High Time		4		0.6		μs
t_{scl}	I²C Clock Low Time		4.7		1.3		μs
t_{sp}	I²C Spike Time			50		50	ns
t_{sds}	I²C Serial-Data Setup Time		250		100		ns
t_{sdh}	I²C Serial-Data Hold Time		0		0		ns
t_{icr}	I²C Input Rise Time			1000	20	300	ns
t_{icf}	I²C Input Fall Time (1)			300	20 + 0.1C_b (2)	300	ns
t_{ocf}	I²C Output Fall Time (1)	10-pF to 400-pF bus		300	20 + 0.1C_b (2)	300	ns
t_{buf}	I²C Bus Free Time Between Stop and Start		4.7		1.3		μs
t_{sts}	I²C Start or Repeated Start Condition Setup		4.7		0.6		μs
t_{sth}	I²C Start or Repeated Start Condition Hold		4		0.6		μs
t_{sps}	I²C Stop Condition Setup		4		0.6		μs
$t_{vd(data)}$	Valid Data Time	SCL low to SDA output valid		3.5		0.9	μs
$t_{vd(ack)}$	Valid Data Time of ACK Condition	ACK signal from SCL low to SDA (out) low		3.5		0.9	μs
t_{PD}	Propagation Delay (3)	from SDA to SDx, or SCL to SCx		0.3		0.3	ns
C_b	I²C Bus Capacitive Load (2)			400		400	pF

(1) All the parameters in the above table are requested by I²C standard, not tested in production.
(2) C_b is the total capacitance of one bus line in pF.
(3) The propagation delay is calculated from the 20-Ω typical R_{on} and the 15-pF load capacitance.

Switching Characteristics

All test conditions: within recommended operating free-air temperature range, $C_L \leq 100$ pF, unless otherwise noted.

Symbol	Description	Condition	Min	Max	Unit
$\overline{\text{RESET}}$ Timing Requirements					
$t_{w\ (rst)\ L}$	Low-Level Reset Time	V_{CC} = 1.65 V to 5.5 V	6		ns
t_{rst}	Reset Time	SDA clear		500	ns
$t_{REC;\ STA}$	Recovery Time to Start Condition		0		ns

Parameter Measurement Waveforms

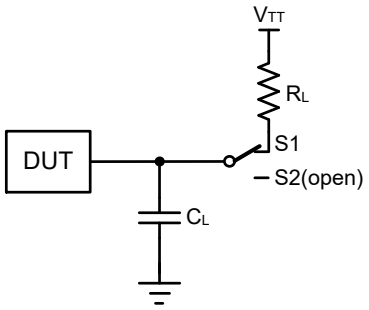


Figure 1. Load Circuit for Outputs

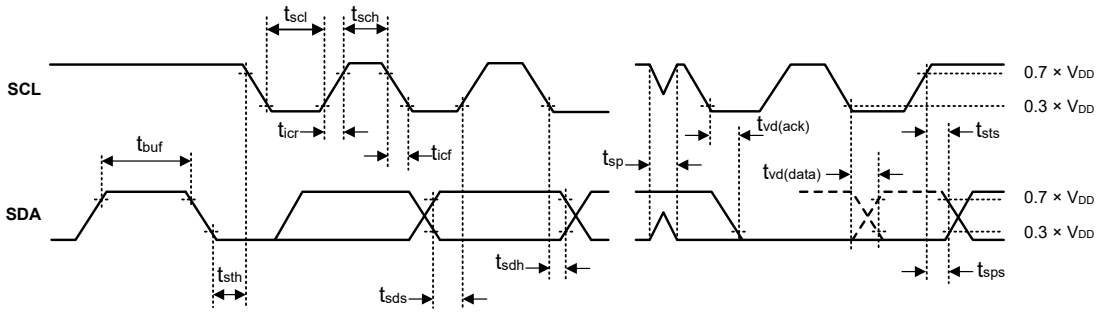


Figure 2. Definition of Timing on the I²C-bus

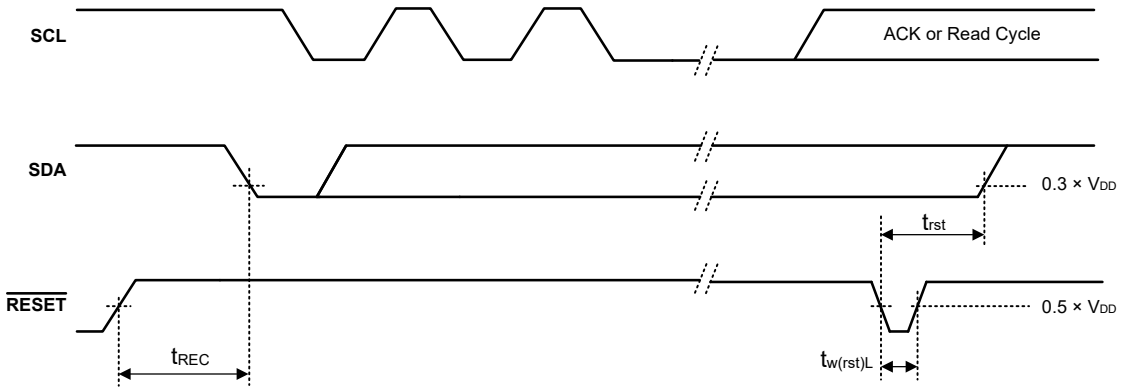


Figure 3. Definition of $\overline{\text{RESET}}$ Timing

Detailed Description

Overview

The TPT29546L is a 1:4 bidirectional translating I²C switch. The SCL/SDA upstream pair fans out to four downstream channels. Any single SCn/SDn channel or combination of channels can be selected, determined by the programmable control register.

If one of the downstream I²C buses is stuck in a low state, then an active-low reset ($\overline{\text{RESET}}$) input helps the TPT29546L to recover. Pulling $\overline{\text{RESET}}$ low resets the I²C state machine and causes all the channels to be deselected, as the internal power-on reset function.

The pass gates of the switches are constructed so that the VCC terminal can be used to limit the maximum high voltage, which is passed by the TPT29546L and operates from 1.65 V to 5.5 V. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5-V tolerant.

Functional Block Diagram

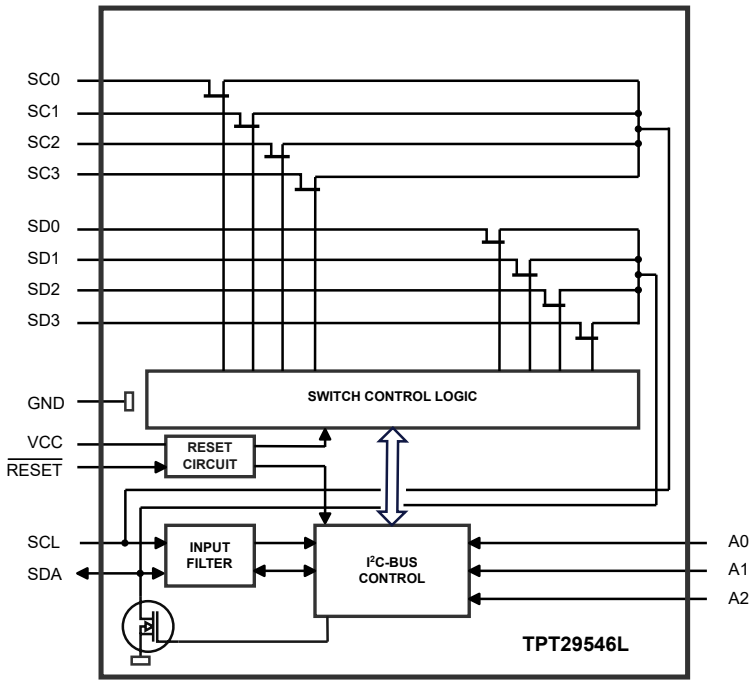


Figure 4. Functional Block Diagram

Feature Description

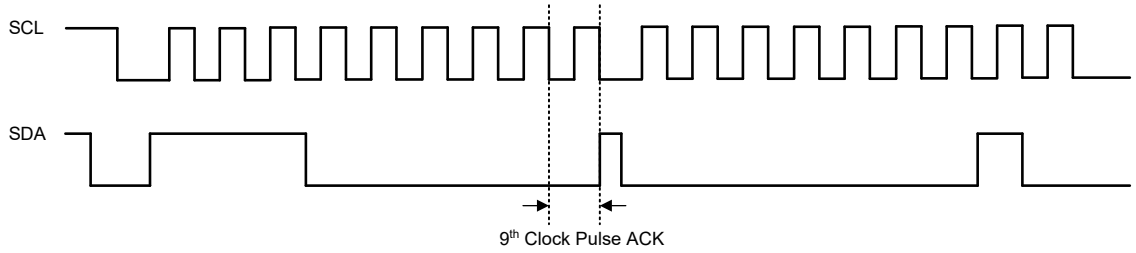


Figure 5. I²C Bus Waveform

Device Address

Following a START condition, the bus master must output the address to which the slave has access. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins, and they must be pulled HIGH or LOW. The address of the TPT29546L is shown below.

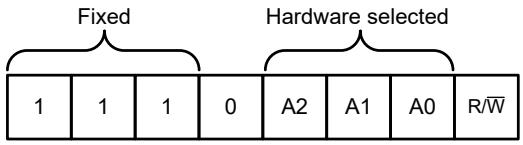


Figure 6. Slave Device Address

Control Register

Following the successful acknowledgment of the slave address, the bus master sends a byte to the TPT29546L, which is stored in the control register. If multiple bytes are received by the TPT29546L, it saves the last byte received. This register can be written and read via the I²C bus.

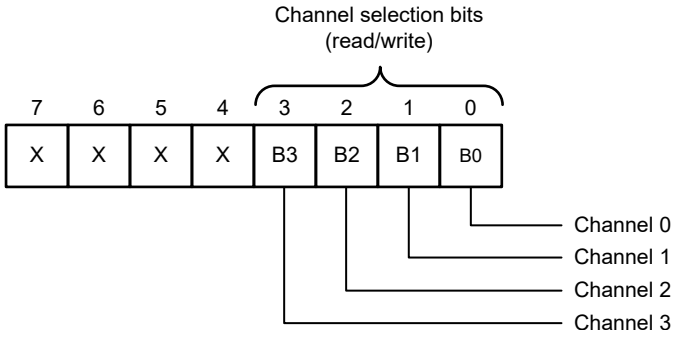


Figure 7. Control Register

Control Register Definition

One or several SCx/SDx downstream pairs, or channels, are selected by the contents of the control register. This register is written after the TPT29546L has been addressed. The control byte is used to determine which channel is to be selected. When a channel is selected, the channel becomes active after a STOP condition has been placed on the I²C bus. This

ensures that all SCx/SDx lines are in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 2. Control Register: Write-Channel Selection; Read-Channel Status

B7	B6	B5	B4	B3	B2	B1	B0	Command
x	x	x	x	x	x	x	0	Channel 0 disable
x	x	x	x	x	x	x	1	Channel 0 enable
x	x	x	x	x	x	0	x	Channel 1 disable
x	x	x	x	x	x	1	x	Channel 1 enable
x	x	x	x	x	0	x	x	Channel 2 disable
x	x	x	x	x	1	x	x	Channel 2 enable
x	x	x	x	0	x	x	x	Channel 3 disable
x	x	x	x	1	x	x	x	Channel 3 enable
0	0	0	0	0	0	0	0	No channel selected, power-up/reset default state

(1) Multiple channels can be enabled at the same time. Example: B3 = 1, B2 =1, B1 = 0, B0 = 0, which means that channels 1, 0 are disabled and channels 3, 2 are enabled. Care should be taken not to exceed the maximum bus capacitance. The default condition is all zeroes.

Bus Transactions

The TPT29546L has only one register, which can be written by sending data directly after the target address, without the need to send a register address.

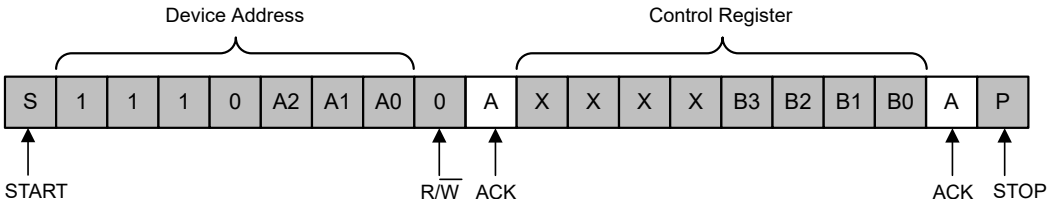


Figure 8. Write Control Register

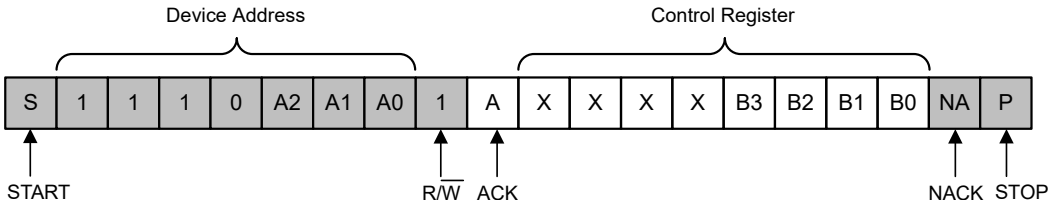


Figure 9. Read Control Register

$\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input is an active-low signal that helps recover from bus fault conditions. By pulling this signal LOW for at least tw(rst)L, the TPT29546L resets its register, I²C-bus state machine, and deselects all channels. The $\overline{\text{RESET}}$ input must be connected to the V_{CC} via a pull-up resistor.

Power-on Reset

When power is supplied to the V_{CC} pin, the TPT29546L remains in a reset state due to an internal power-on reset until VCC reaches the V_{PORR} threshold. At that moment, the reset is lifted, and the registers of the device and I²C state machine are initialized to their default settings (all zeros), resulting in all channels being deselected. To reset the device again, V_{CC} must be decreased to below the V_{PORF} level.

Voltage Translation

For the TPT29546L to act as a voltage translator, the $V_{o(sw)}$ voltage should be equal to or lower than the lowest bus voltage. $V_{o(sw)}$ is the pass gate voltage (V_{pass}) of the switches. The pass gates of the switches are constructed so that the VCC terminal can be used to limit the maximum high voltage, which is passed by the TPT29546L and operating from 1.65 V to 5.5 V. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5-V tolerant.

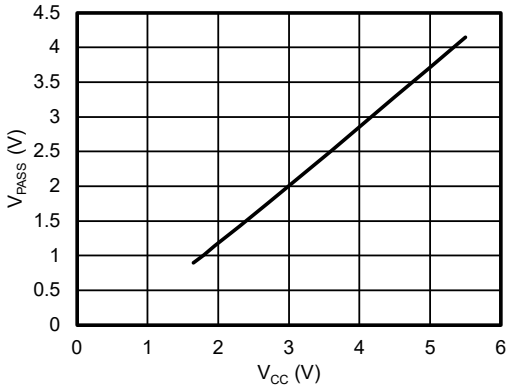


Figure 10. Pass Gate Voltage (V_{pass}) vs. Supply Voltage (V_{CC})

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT29546L can connect one I²C master device and four target devices, and it can resolve address conflicts for the downstream channels.

Typical Application

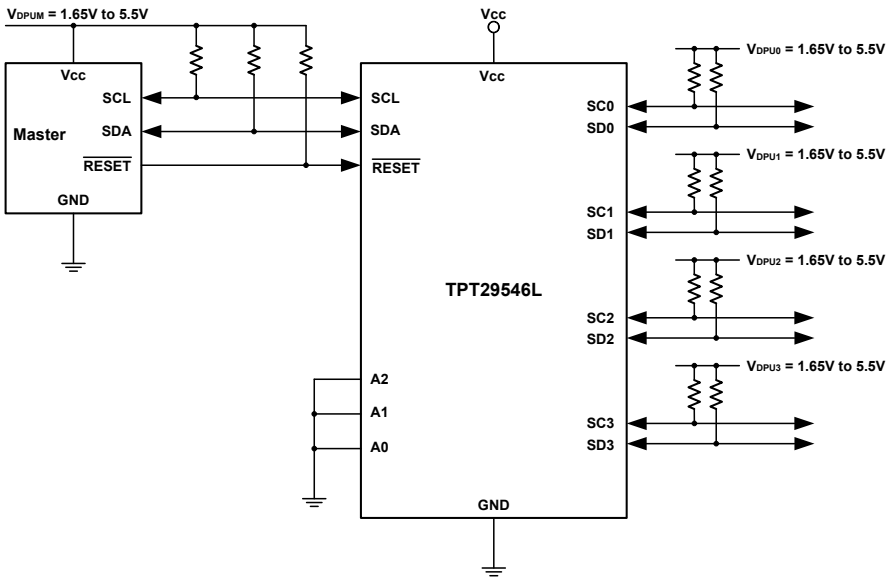


Figure 11. Typical Application Circuit

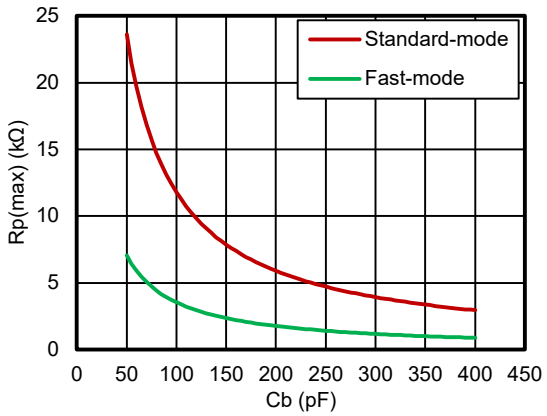
Pull-Up Resistance

The minimum pull-up resistance is a function of V_{DPUX}, $V_{OL(max)}$, and I_{OL}.

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of t_r and C_b.

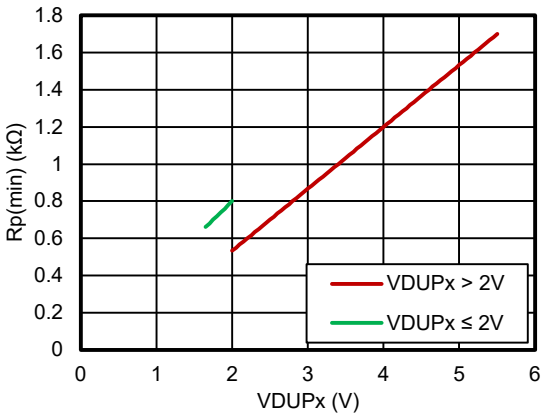
$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$



Standard-mode (f_{scl} = 100 kHz, t_r = 1 µs)

Fast-mode (f_{scl} = 400 kHz, t_r = 300 ns)

Figure 12. Maximum Pull-Up Resistance ($R_{p(max)}$) vs. Bus Capacitance (C_b)



V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{DPUX} > 2 V

V_{OL} = 0.2*V_{DPUX}, I_{OL} = 2 mA when V_{DPUX} ≤ 2 V

Figure 13. Minimum Pull-Up Resistance ($R_{p(min)}$) vs. Bus Capacitance (C_b)

Layout

Layout Example

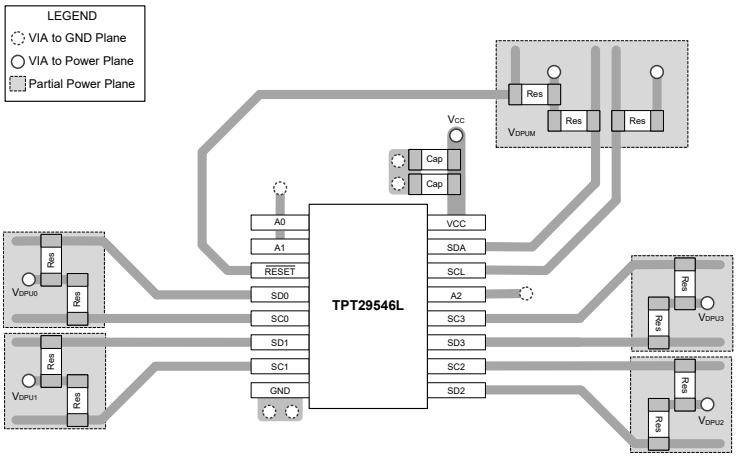
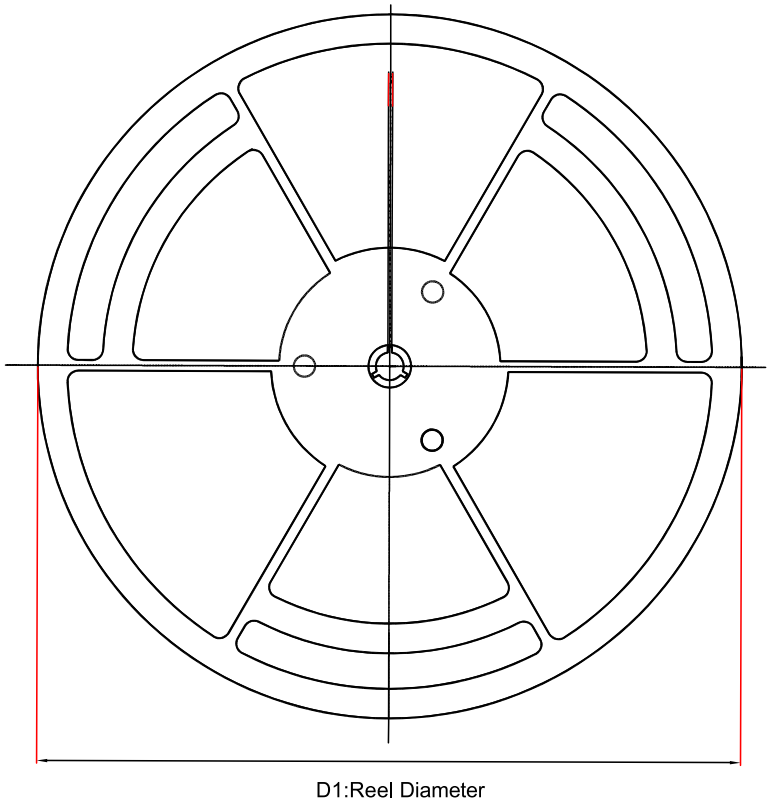
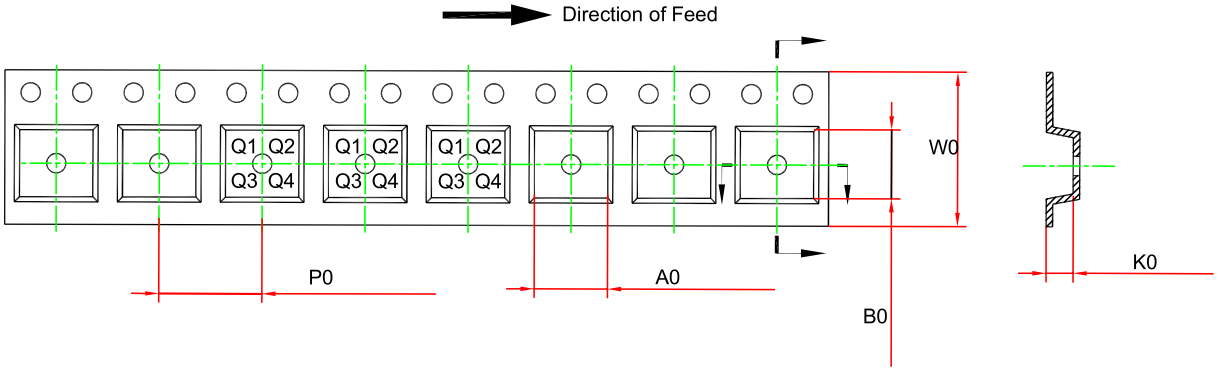


Figure 14. TPT29546L Layout Example

Tape and Reel Information



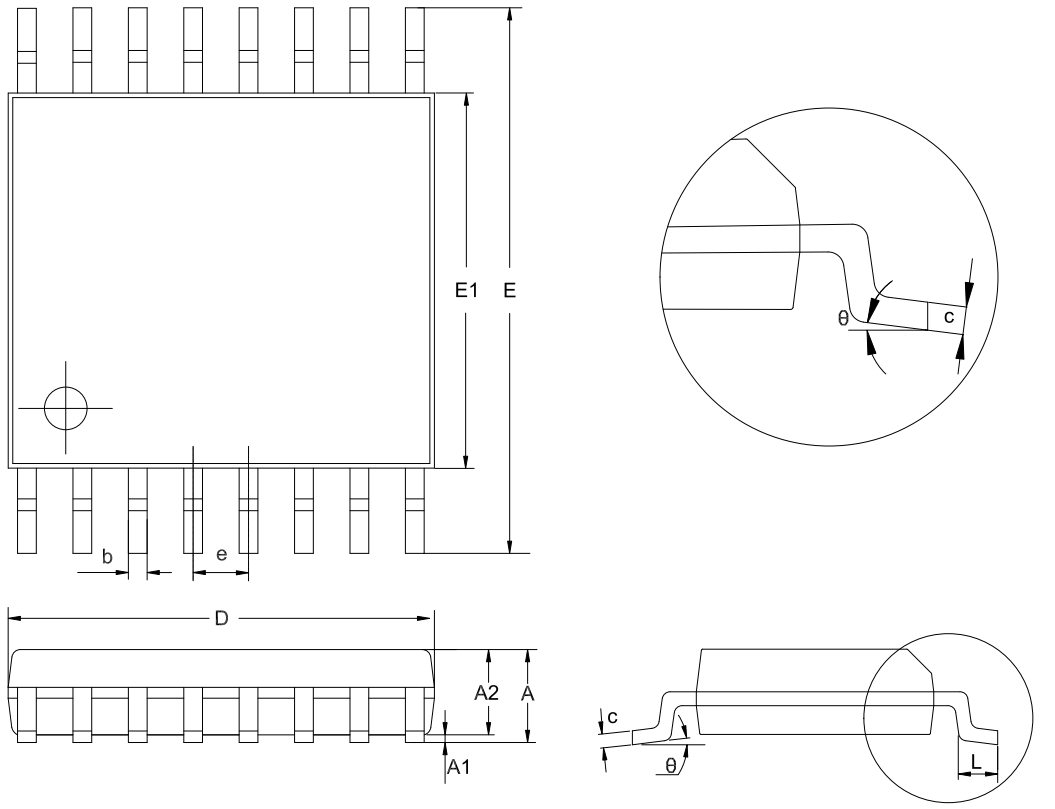


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT29546L-TS3R	TSSOP16	330	17.6	6.8	5.5	1.3	8	12	Q1

Package Outline Dimensions

TSSOP16

Package Outline Dimensions TS3(TSSOP-16-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29546L-TS3R	−40 to 125°C	TSSOP16	29546L	MSL3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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