Automotive I²C to 16-bit GPIO Expander with Interrupt and Reset

Features

- I²C-bus to 16-bit GPIO Expander
- Operating Power Supply Voltage from 1.65 V to 3.6 V
- Low Standby Current Consumption:
  - 1.5 μA (typical at 3.3 V V_{CC})
- 400-kHz Fast-mode I²C-bus
- 5-V Tolerant I/Os
- Internal Power-on Reset
- Open-drain Active LOW Interrupt Output ($\overline{INT}$)
- Configurable Slave Address with 2 Address Pins
- Latch-Up Performance exceeds 200 mA per JESD 78
- ESD Protection Exceeds JESD 22
  - ±4000-V Human Body Model
  - ±1500-V Charged Device Model
- AEC Q100: Automotive Grade 1

Applications

- Automotive ASAS, Infotainment,
- Automotive Body Electronics, EV/HEV
- Servers/Storages/Routers (Telecom Switching Equipment)
- Personal Computers

Description

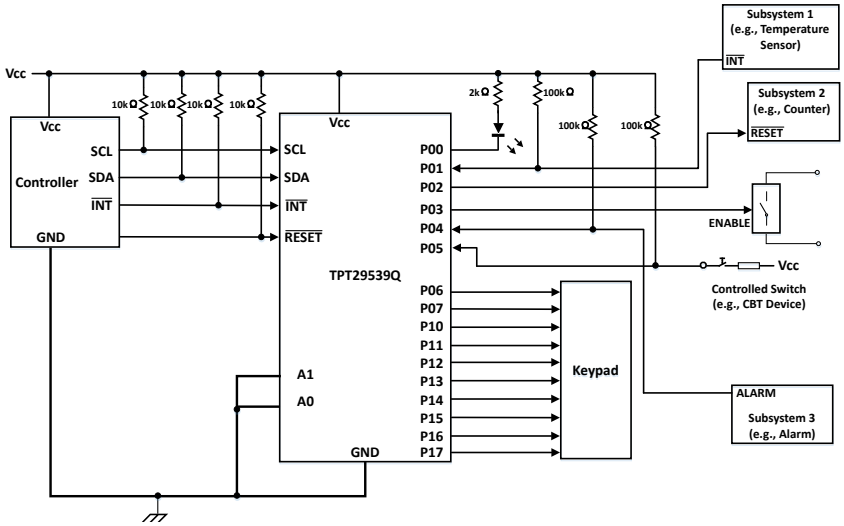
The TPT29539Q is a 16-bit GPIO expander with interrupt and weak pull-up resistors for I²C-bus applications. The power supplier voltage ranges from 1.65 V to 3.6 V, allowing for the TPT29539Q to interconnect with 1.8-V microcontrollers.

The TPT29539Q contains 16-bit Input and Output. The open-drain interrupt ($\overline{INT}$) output is changeable when any input state changes from its related register state. The device is used to indicate the system master that an input state has changed. ($\overline{INT}$) can be connected to the interrupt input of a microcontroller. The TPT29539Q can remain a simple slave device. The power-on reset sets the registers to their default values and initializes the device state machine. The TPT29539Q also has a hardware $\overline{INT}$ pin to reset the device to its default state.

All input/output pins do not have internal pull-up resistors, thus the device can save power consumption as communicating with external I/Os. Two hardware pins (A0, A1) select the fixed I²C-bus address and allow up to eight devices to share the same I²C-bus.

The TPT29539Q is available in the TSSOP24 package, and is characterized from −40°C to +125°C to meet automotive application requirements.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2023-12-18	Rev.A.0	Released version
2024-02-07	Rev.A.1	Updated Typical Application Circuit
2024-02-20	Rev.A.2	Updated the V_{OH}/I_{OL}/I_{CC} test condition
2024-03-31	Rev.A.3	Updated the standby I_{CC} as input low condition
2024-06-26	Rev.A.4	Added the Reset timing and updated the tps spec
2024-08-12	Rev.A.5	Corrected the typo of the K0 value of 1.6 to 1.25 in the Tape and Reel Information section

Pin Configuration and Functions

TPT29539Q
TSSOP24 Package
Top View

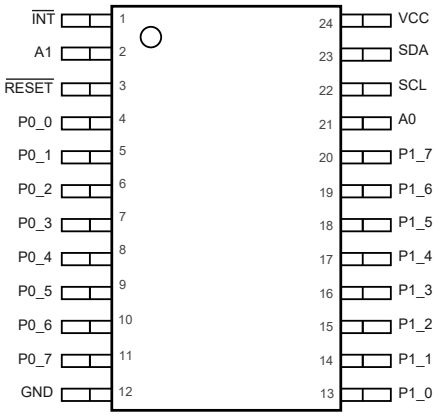


Table 1. Pin Functions: TPT29539Q

Pin No.	Name	I/O	Description
21	A0	Input	Address input 0. Connect directly to VCC or ground
2	A1	Input	Address input 1. Connect directly to VCC or ground
3	$\overline{\text{RESET}}$	Input	RESET input, active LOW
12	GND	GND	Ground
1	$\overline{\text{INT}}$	Output	Interrupt output. Connect to VCC through a pull-up resistor
4	P0_0	I/O	P-port I/O. Push-pull design structure. At power on, P0_0 is configured as an input
5	P0_1	I/O	P-port I/O. Push-pull design structure. At power on, P0_1 is configured as an input
6	P0_2	I/O	P-port I/O. Push-pull design structure. At power on, P0_2 is configured as an input
7	P0_3	I/O	P-port I/O. Push-pull design structure. At power on, P0_3 is configured as an input
8	P0_4	I/O	P-port I/O. Push-pull design structure. At power on, P0_4 is configured as an input
9	P0_5	I/O	P-port I/O. Push-pull design structure. At power on, P0_5 is configured as an input
10	P0_6	I/O	P-port I/O. Push-pull design structure. At power on, P0_6 is configured as an input
11	P0_7	I/O	P-port I/O. Push-pull design structure. At power on, P0_7 is configured as an input
13	P1_0	I/O	P-port I/O. Push-pull design structure. At power on, P1_0 is configured as an input
14	P1_1	I/O	P-port I/O. Push-pull design structure. At power on, P1_1 is configured as an input
15	P1_2	I/O	P-port I/O. Push-pull design structure. At power on, P1_2 is configured as an input
16	P1_3	I/O	P-port I/O. Push-pull design structure. At power on, P1_3 is configured as an input
17	P1_4	I/O	P-port I/O. Push-pull design structure. At power on, P1_4 is configured as an input
18	P1_5	I/O	P-port I/O. Push-pull design structure. At power on, P1_5 is configured as an input
19	P1_6	I/O	P-port I/O. Push-pull design structure. At power on, P1_6 is configured as an input
20	P1_7	I/O	P-port I/O. Push-pull design structure. At power on, P1_7 is configured as an input

Pin No.	Name	I/O	Description
22	SCL	Input	Serial clock bus. Connect to VCC through a pull-up resistor
23	SDA	I/O	Serial data bus. Connect to VCC through a pull-up resistor
24	VCC	Supply	Supply voltage

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	−0.5	3.6	V
V_I	Input Voltage	−0.5	3.6	V
V_O	Output Voltage	−0.5	3.6	V
I_{IK}	Input Clamp Current, $V_I < 0$		−20	mA
I_{OK}	Output Clamp Current, $V_O < 0$		−20	mA
I_{IOK}	Input-Output Clamp Current, $V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous Output Low Current, V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous Output High Current, V_O = 0 to V_{CC}		−50	mA
I_{CC}	Continuous Current through GND		−250	mA
	Continuous Current through V_{CC}		160	mA
T_J	Maximum Junction Temperature		135	°C
T_{stg}	Storage Temperature	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Over-operating free-air temperature range (unless otherwise noted).

Parameter			Min	Max	Unit
V_{CC}	Supply Voltage		1.65	3.6	V
VIO	Output IO Voltage	P0_7 ~ P0_0, P1_7 ~ P1_0	0	3.6	V
	Input IO Voltage	P0_7 ~ P0_0, P1_7 ~ P1_0	0	3.6	V
	IO Voltage	SCL, SDA, A1, A0, $\overline{RESET}$, $\overline{INT}$	0	3.6	V
V_{IH}	High-Level Input Voltage	SCL, SDA	0.7 × V_{CC}	V_{CC}	V
		$\overline{RESET}$, A2 ~ A0, P0_7 ~ P0_0, P1_7 ~ P1_0	0.7 × V_{CC}	V_{CC}	V
V_{IL}	Low-Level Input Voltage	SCL, SDA	−0.5	0.3 × V_{CC}	mV
		$\overline{RESET}$, A2 ~ A0, P0_7 ~ P0_0, P1_7 ~ P1_0	−0.5	0.3 × V_{CC}	mV
I_{OH}	High-Level Output Current	P0_7 ~ P0_0, P1_7 ~ P1_0		−10	mA
I_{OL}	Low-Level Output Current	P0_7 ~ P0_0, P1_7 ~ P1_0		25	mA
		$\overline{INT}$, SDA		6	mA
T_A	Operating Temperature Range		−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP24	68	21	°C/W

Electrical Characteristics

All test conditions: V_{CC} = 1.65 V ~ 3.6 V, T_A = −40 ~ +125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Input Electrical Specifications						
V_{POR}	Power-on Reset Voltage，V_{CC} rising	V_I = V_{CC} or GND; I_O = 0 mA		1.25	1.5	V
	Power-on Reset Voltage，V_{CC} falling	V_I = V_{CC} or GND; I_O = 0 mA	0.7	1.2		V
I_{OL}	LOW-level Output Current, SDA	V_{OL} = 0.4 V; V_{CC} = 1.65 V to 3.6 V	3			mA
	LOW-level Output Current, $\overline{INT}$	V_{OL} = 0.4 V; V_{CC} = 1.65 V to 3.6 V	3			mA
	LOW-level Output Current, P port	V_{OL} = 0.5 V; V_{CC} = 1.65 V	8			mA
		V_{OL} = 0.5 V; V_{CC} = 2.3 V (1)	8			mA
		V_{OL} = 0.5 V; V_{CC} = 3.0 V	8			mA
	LOW-level Output Current, P port	V_{OL} = 0.7 V; V_{CC} = 1.65 V	10			mA
		V_{OL} = 0.7 V; V_{CC} = 2.3 V (1)	10			mA
		V_{OL} = 0.7 V; V_{CC} = 3.0 V	10			mA
V_{OH}	HIGH-level Output Voltage, P port	I_{OH}= −8 mA; V_{CC}= 1.65 V	1.2			V
		I_{OH}= −8 mA; V_{CC}= 2.3 V (1)	1.8			V
		I_{OH}= −8 mA; V_{CC}= 3.0 V	2.6			V
	HIGH-level Output Voltage, P port	I_{OH}= −10 mA; V_{CC}= 1.65 V	1.0			V
		I_{OH} = −10 mA; V_{CC}= 2.3 V (1)	1.7			V
		I_{OH} = −10 mA; V_{CC}= 3.0 V	2.5			V
I_I	Input Current: A0, A1, $\overline{RESET}$	V_{CC}= 1.65 V to 3.6 V, V_I= V_{CC} or GND	−1		1	μA
	Input Current: SCL, SDA	V_{CC}= 1.65 V to 3.6 V, V_I= V_{CC} or GND	−1		1	μA
I_{IH}	HIGH-level Input Current: P port	V_I= V_{CC}; V_{CC}= 1.65 V to 3.6 V			1	μA
I_{IL}	LOW-level Input Current: P Port	V_I= GND; V_{CC}= 1.65 V to 3.6 V	−1			μA

(1) Parameters are provided by lab bench tests and design simulation. Not tested in production.

Electrical Characteristics (Continued)

All test conditions: V_{CC} = 1.65 V ~ 3.6 V, T_A = −40 ~ +125°C, unless otherwise noted.

Parameter		Conditions		Min	Typ	Max	Unit
I_{cc}	Supply Current	Active mode, IO = 0 mA; I/O = inputs; fSCL = 400 kHz	V_{CC}= 3.6 V		9	30	μA
			V_{CC}= 2.7 V (1)		6.2	19	μA
			V_{CC}= 1.95 V		4.2	11	μA
		Standby Mode, input low, IO = 0 mA; I/O = inputs; fS_{SCL} = 0 kHz	V_{CC}= 3.6 V		3.0	5.0	μA
			V_{CC}= 2.7 V (1)		2.0	4.5	μA
			V_{CC}= 1.95 V		1.5	3.5	μA
		Standby Mode, input high, IO = 0 mA; I/O = inputs; f_{SCL} = 0 kHz	V_{CC}= 3.6 V		1.5	5.0	μA
			V_{CC}= 2.7 V (1)		1.0	4.5	μA
			V_{CC}= 1.95 V		0.6	3.5	μA
C_i (1)	Input Capacitance	V_I= V_{CC} or GND; V_{CC}= 1.65 V to 3.6 V (1)			3		pF
C_{io} (1)	Input/Output Capacitance	$V_{I/O}$= V_{CC} or GND; V_D= 1.65 V to 3.6 V (1)			3		pF
		$V_{I/O}$= V_{CC} or GND; V_{CC}= 1.65 V to 3.6 V (1)			5		pF

(1) Parameters are provided by lab bench tests and design simulation. Not tested in production.

I²C Interface Timing Requirements (1)

Over recommended operating free-air temperature range, unless otherwise noted.

Description		Conditions	Standard Mod		Fast Mode		Unit
			Min	Max	Min	Max	
fscl	I²C clock frequency		0	100	0	400	kHz
tsch	I²C clock high time		4		0.6		μs
tscl	I²C clock low time		4.7		1.3		μs
tsp	I²C spike time			50		50	ns
tsds	I²C serial-data setup time		250		100		ns
tsdh	I²C serial-data hold time		0		0		ns
ticr (2)	I²C input rise time			1000	20	300	ns
ticf (3)	I²C input fall time			300	20 × (V_{CC}/ 3.6 V)	300	ns
tocf (3)	I²C output fall time	10-pF to 400-pF bus		300	20 × (V_{CC}/ 3.6 V)	300	ns
tbuf	I²C bus free time between stop and start		4.7		1.3		μs
tsts	I²C start or repeated start condition setup		4.7		0.6		μs
tsth	I²C start or repeated start condition hold		4		0.6		μs
tsps	I²C stop condition setup		4		0.6		μs
tvd(data)	Valid data time	SCL low to SDA output valid		3.5		0.9	μs
tvd(ack)	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.5		0.9	μs
Cb	I²C bus capacitive load			400		400	pF

(1) All timing requirements should refer to I²C standard, and all parameters in table are NOT tested in production.
(2) ticr is decided by input signal rising time.
(3) Data is provided by bench validation, test condition: 150ohm series resistor connect to SDA pin, then 2.2 Kohm pull up to VCC, 150 pF Cload pull down to GND, t_{icr} = 29 ns, t_{ocf} = 25 ns, V_{OL} = 166 mv.

Switching Characteristics

Over recommended operating free-air temperature range, C_L ≦ 100 pF, unless otherwise noted.

Description		From (Input)	To (Output)	Standard Mod		Fast Mode		Unit
				Min	Max	Min	Max	
tiv	Interrupt valid time	P port	$\overline{INT}$		4		4	μs
tir	Interrupt reset delay time	SCL	$\overline{INT}$		4		4	μs
tpv	Output data valid; For V_{CC} = 2.3 V ~ 3.6 V	SCL	P port		400		400	ns
	Output data valid; For V_{CC} = 1.65 V ~ 2.3 V				400		400	ns
tps	Input data setup time	P port	SCL	150		150		ns
tph	Input data hold time	P port	SCL	1		1		μs

Parameter		Condition	min	typ	max	Unit
RESET Timing Requirements						
tW	Reset pules duration		60			ns
tREC	Reset recovery time		0		15	ns
tRESET	Time to reset	For VCC = 2.3 V~3.6 V	400			
	Time to reset	For VCC = 1.65 V – 2.3 V	550			ns

Parameter Measurement Waveforms

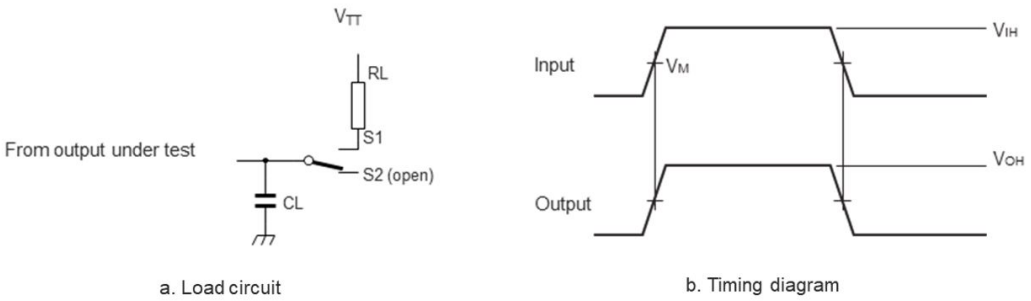


Figure 1. Load Circuit for Outputs

Typical Performance Characteristics

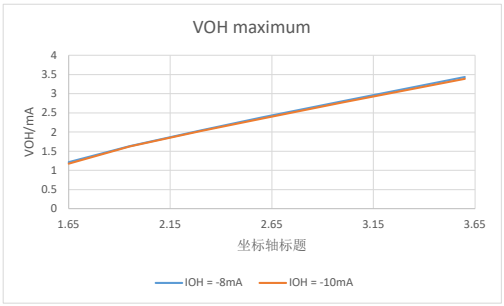


Figure 2. Voh Maximum Measurement

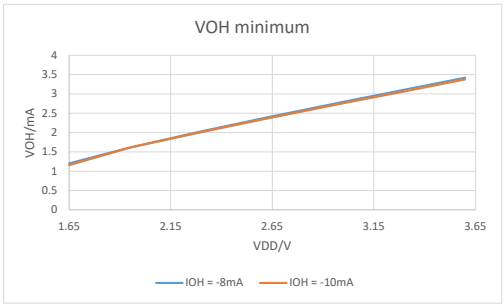


Figure 3. Voh Minimum Measurement

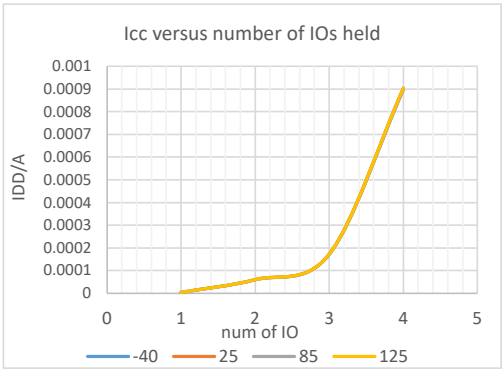


Figure 4. Icc versus Number of IOS Measurement

Detailed Description

Overview

The TPT29539Q is a 16-bit GPIO expander with interrupt and weak pull-up resistors for I²C-bus applications. The power supplier voltage ranges from 1.65 V to 3.6 V, allowing for the TPT29539Q to interconnect with 1.8-V microcontrollers.

The TPT29539Q contains 16-bit Input and Output. The open-drain interrupt ($\overline{INT}$) output is changeable when any input state changes from its related register state. The device is used to indicate the system master that an input state has changed. ($\overline{INT}$) can be connected to the interrupt input of a microcontroller. The TPT29539Q can remain a simple slave device. The power-on reset sets the registers to their default values and initializes the device state machine. The TPT29539Q also has a hardware $\overline{INT}$ pin to reset the device to its default state.

All input/output pins do not have internal pull-up resistors, thus the device can save power consumption as communicating with external I/Os. Two hardware pins (A0, A1) select the fixed I²C-bus address and allow up to eight devices to share the same I²C-bus.

The TPT29539Q is available in the TSSOP24 package, and is characterized from −40°C to +125°C to meet automotive application requirements.

Functional Block Diagram

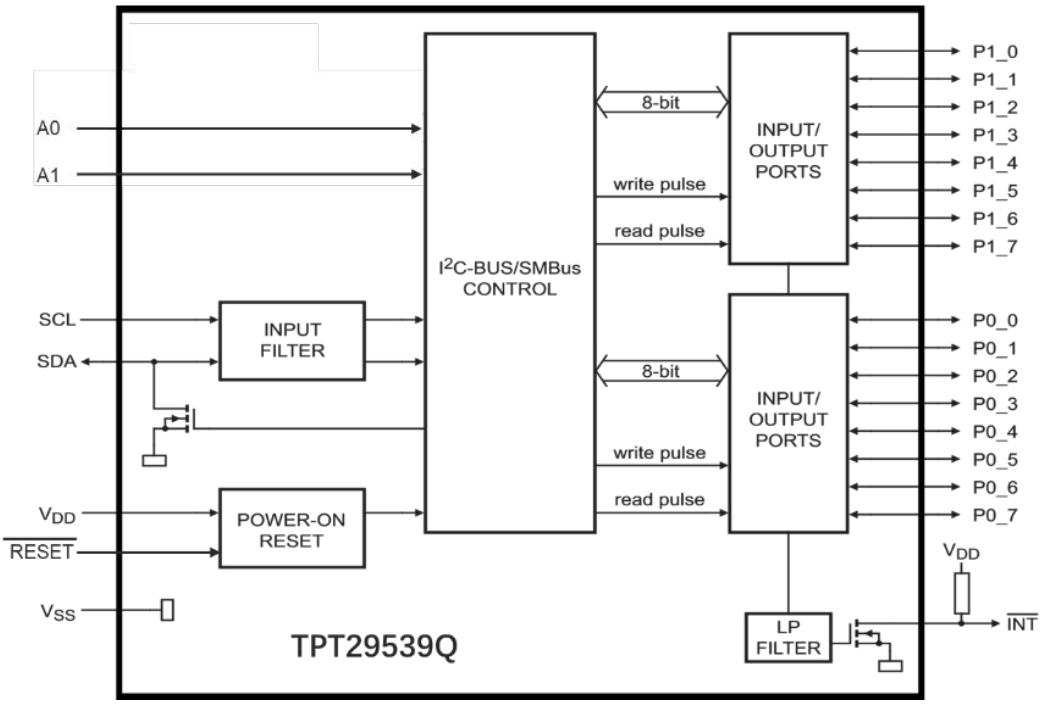


Figure 5. Functional Block Diagram

Feature Description

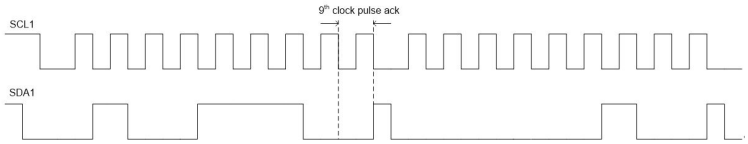


Figure 6. I2C BUS (1.65 V ~ 3.6 V) Waveform

Device Address

Following a START condition, the bus master must output the address of the slave it is accessing. All input/output pins have internal weak pull-up resistors to remove external components. Two hardware pins (A0, A1) select the fixed I2C-bus address and allow up to eight devices to share the same I2C-bus. To conserve power, address pins (A0, A1) must be pulled HIGH or LOW. The address of the TPT29539Q is shown below.

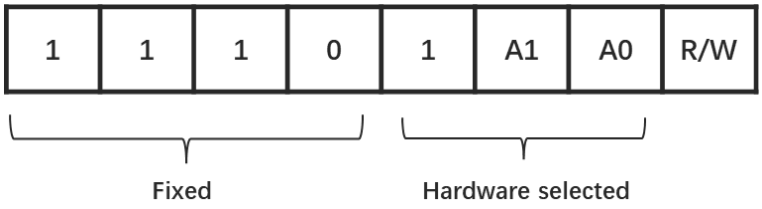


Figure 7. Slave Device Address

Control Register

Command Byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 2. Command Byte Description

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity Inversion port 0
5	Polarity Inversion port 1
6	Configuration port 0
7	Configuration port 1

Register 0 and 1: Input port registers

This register is an input-only port, which means the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3 (output port 1) ,and writes to this register have no effect.

The default value 'X' is determined by the externally logic level.

Table 3. Input Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 4. Input Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

Register 2 and 3: Output port registers

This register is an output-only port, which means the outcoming logic levels of the pins are defined as outputs by Register 6 (Configuration port 0) and 7 (Configuration port 1). Bit values in this register have no effect on pins defined as inputs. In fact, the value reading from this register is in the flip-flop controlling the output selection, not the actual pin value.

Table 5. Output Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 6. Output Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

Register 4 and 5: Polarity Inversion registers

This register allows the user to invert the polarity of the input port register data. If a bit in this register is set (written with '1'), the input port data polarity is inverted. If a bit in this register is cleared (written with '0'), the input port data polarity is retained.

Table 7. Polarity Inversion Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 8. Polarity Inversion Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

Register 6 and 7: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. Note that there is a high-value resistor tied to V_{DD} at each pin. At reset, the device's ports are inputs with a pull-up to V_{DD}.

Table 9. Configuration port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 10. Configuration port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT29539Q builds in 16-bit input and output, and interrupt $\overline{INT}$ can be connected to the interrupt input of a microcontroller, then the interrupt $\overline{INT}$ output will response to any input state change.

IO Configuration Requirements

To make sure the TPT29539Q can support the different application, the device is requested to set all GPIOs a default value after or before powering up the device. Or the backup method, after powering up the TPT29539Q, registers are reset to a default value by digital circuit while GPIOs status are not yet stable, because there is no pull-up/pull-down resistors inside. The digital circuit is monitoring and comparing the GPIOs status to the default value of the registers in real time and when they are not matched, during the unstable period, the $\overline{INT}$ is locked. This has been confirmed in lab testing by adding time delay in seconds after powering up the TPT29539Q (for GPIOs status to reach a stable status). After seconds, the $\overline{INT}$ function is ready to work, and the performance is exactly as designed. The delay time will depend on the different capacitance on board.

Typical Application

One application of the TPT29539Q device is used as below.

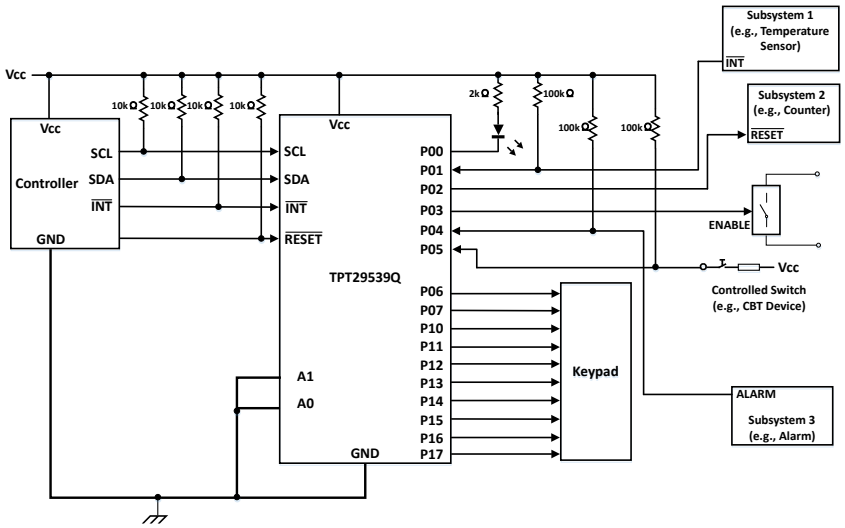


Figure 8. Typical Application Reference Circuit

Layout

Layout Guideline

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they will have to turn corners. Figure 9 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

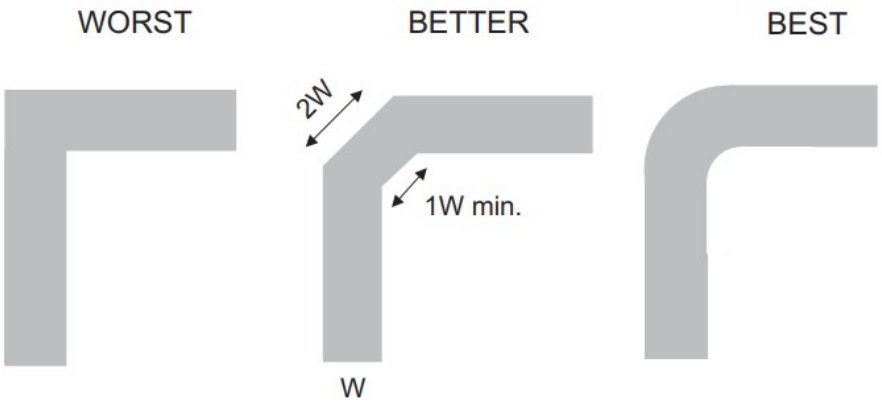


Figure 9. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Layout Example

Figure 10 illustrates an example of a PCB layout with the TPT29539Q. Some key considerations are as follows:

- Decouple the VDD pin with a 0.1-μF capacitor, placed it as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the VDD supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

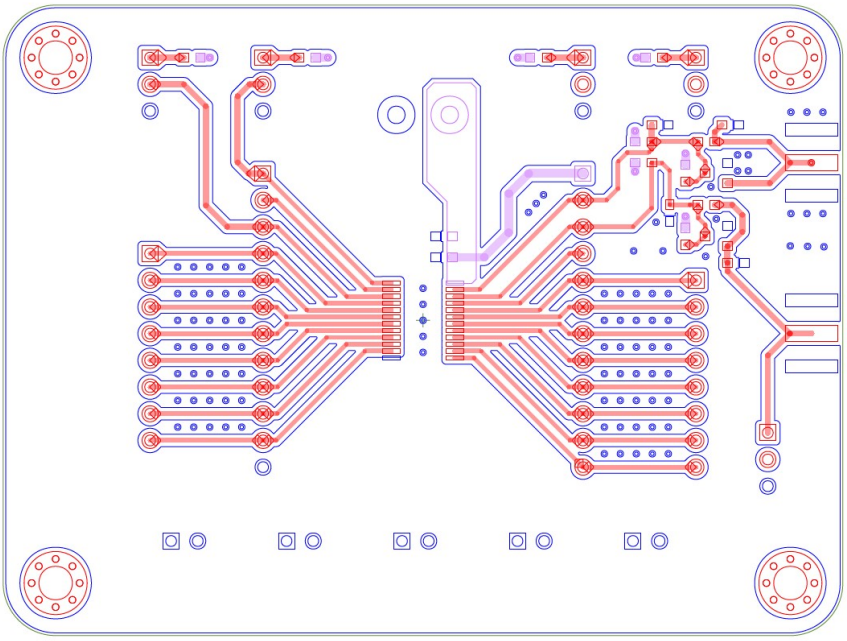
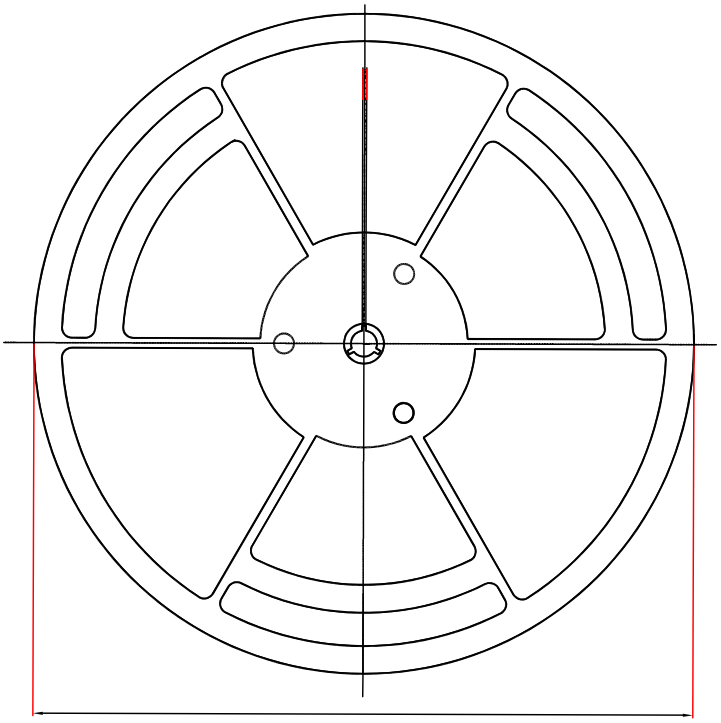
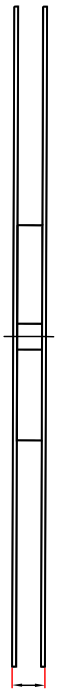
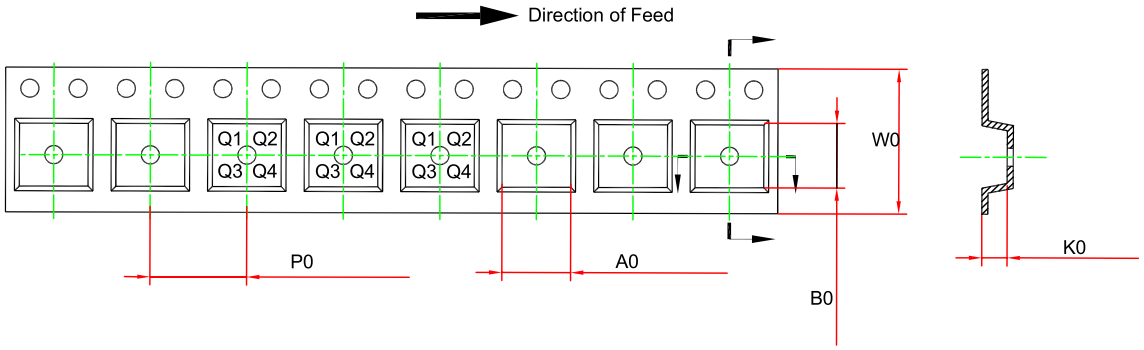


Figure 10. TPT29539Q Layout Example

Tape and Reel Information





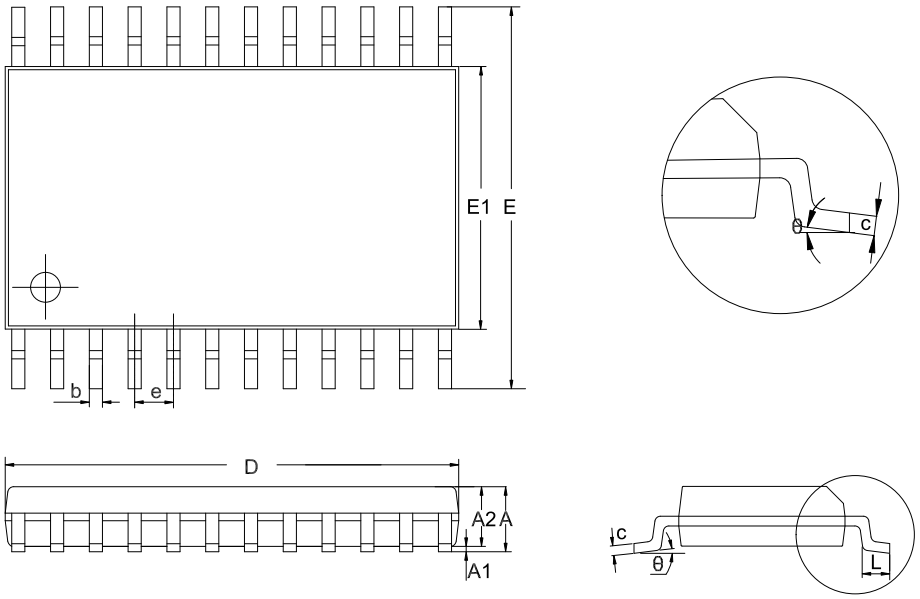


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT29539Q-TS5R-S	TSSOP24	330	21.6	6.8	8.3	1.25	8	16	Q1

Package Outline Dimensions

TSSOP24-A

Package Outline Dimensions TS5(TSSOP-24-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	7.700	7.900	0.303	0.311
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29539Q-TS5R-S	−40 to 125°C	TSSOP24	9539Q	MSL3	4,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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