Automotive I²C to 16-bit GPIO Expander with Interrupt and Reset

Features

- AEC-Q100: Automotive Grade 1
- Functional Safety-Capable
  - Documentation Available to Aid in Functional Safety System Design
- I²C-bus to 16-bit GPIO Expander
- Operating Power Supply Voltage from 1.65 V to 5.5 V
- Low Standby Current Consumption
- 400-kHz Fast-mode I²C-bus
- 5-V Tolerant, 16 I/O Ports, Default to Input Mode
- Internal Power-on Reset
- Active-Low Reset Input
- Open-drain Active LOW Interrupt Output ($\overline{INT}$)
- Configurable Slave Address with 2 Address Pins
- ESD Protection Exceeds JESD 22
  - ±4000-V Human Body Model
  - ±1500-V Charged Device Model

Applications

- Automotive ADAS, Infotainment,
- Automotive Body Electronics, EV/HEV
- Servers/Storages/Routers (Telecom Switching Equipment)
- Personal Computers

Description

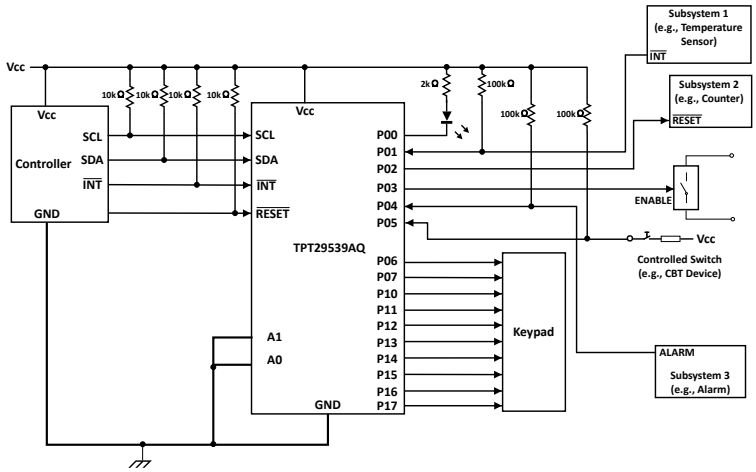
The TPT29539AQ is a 16-bit GPIO expander with interrupt and weak pull-up resistors for I²C-bus applications. The power supplier voltage ranges from 1.65 V to 5.5 V, allowing for the TPT29539AQ to interconnect with 1.8 V microcontrollers.

The TPT29539AQ contains 16-bit Input and Output. The open-drain interrupt ($\overline{INT}$) output is changeable when any input state changes from its related register state. The device is used to indicate the system master that an input state has changed. $\overline{INT}$ can be connected to the interrupt input of a microcontroller. The TPT29539AQ can remain a simple slave device. The power-on reset sets the registers to their default values and initializes the device state machine. The TPT29539AQ also has a hardware $\overline{RESET}$ pin to reset the device to its default state.

All input/output pins do not have internal pull-up resistors, thus the device can save power consumption as communicating with external I/Os. Two hardware pins (A0, A1) select the fixed I²C-bus address and allow up to four devices to share the same I²C-bus.

The TPT29539AQ is available in the TSSOP24 package, and is characterized from −40°C to +125°C to meet automotive application requirements.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2025-08-10	Rev.A.0	Released version.

Pin Configuration and Functions

TPT29539AQ
TSSOP24 Package
Top View

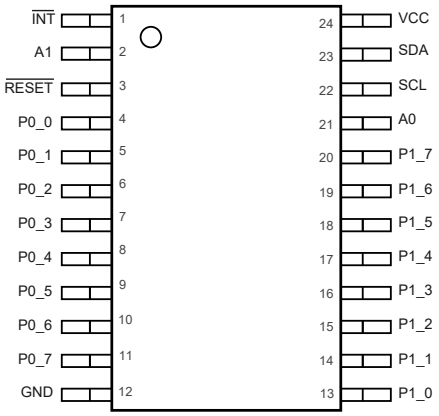


Table 1. Pin Functions: TPT29539AQ

Pin No.	Name	I/O	Description
21	A0	Input	Address input 0. Connect directly to VCC or ground.
2	A1	Input	Address input 1. Connect directly to VCC or ground.
3	$\overline{\text{RESET}}$	Input	RESET input, active-LOW.
12	GND	GND	Ground
1	$\overline{\text{INT}}$	Output	Interrupt output. Connect to VCC through a pull-up resistor.
4	P0_0	I/O	P-port I/O. Push-pull design structure. On powering on, P0_0 is configured as an input.
5	P0_1	I/O	P-port I/O. Push-pull design structure. On powering on, P0_1 is configured as an input.
6	P0_2	I/O	P-port I/O. Push-pull design structure. On powering on, P0_2 is configured as an input.
7	P0_3	I/O	P-port I/O. Push-pull design structure. On powering on, P0_3 is configured as an input.
8	P0_4	I/O	P-port I/O. Push-pull design structure. On powering on, P0_4 is configured as an input.
9	P0_5	I/O	P-port I/O. Push-pull design structure. On powering on, P0_5 is configured as an input.
10	P0_6	I/O	P-port I/O. Push-pull design structure. On powering on, P0_6 is configured as an input.
11	P0_7	I/O	P-port I/O. Push-pull design structure. On powering on, P0_7 is configured as an input.

Pin No.	Name	I/O	Description
13	P1_0	I/O	P-port I/O. Push-pull design structure. On powering on, P1_0 is configured as an input.
14	P1_1	I/O	P-port I/O. Push-pull design structure. On powering on, P1_1 is configured as an input.
15	P1_2	I/O	P-port I/O. Push-pull design structure. On powering on, P1_2 is configured as an input.
16	P1_3	I/O	P-port I/O. Push-pull design structure. On powering on, P1_3 is configured as an input.
17	P1_4	I/O	P-port I/O. Push-pull design structure. On powering on, P1_4 is configured as an input.
18	P1_5	I/O	P-port I/O. Push-pull design structure. On powering on, P1_5 is configured as an input.
19	P1_6	I/O	P-port I/O. Push-pull design structure. On powering on, P1_6 is configured as an input.
20	P1_7	I/O	P-port I/O. Push-pull design structure. On powering on, P1_7 is configured as an input.
22	SCL	Input	Serial clock bus. Connect to VCC through a pull-up resistor.
23	SDA	I/O	Serial data bus. Connect to VCC through a pull-up resistor.
24	VCC	Supply	Supply voltage

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	−0.5	6.0	V
V_I	Input Voltage	−0.5	6.0	V
I_{IK}	Input Clamp Current, $V_I < 0$		−20	mA
I_{OK}	Output Clamp Current, $V_O < 0$		−20	mA
I_{IOK}	Input-Output Clamp Current, $V_O < 0$ or $V_O > V_{CC}$	−20	20	mA
I_{OL}	Continuous Output Low Current, V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous Output High Current, V_O = 0 to V_{CC}		−50	mA
I_{CC}	Continuous Current through GND		−250	mA
	Continuous Current through V_{CC}		160	mA
T_J	Maximum Junction Temperature		135	°C
T_{stg}	Storage Temperature	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

Parameter			Min	Max	Unit
V_{CC}	Supply Voltage		1.65	5.5	V
VIO	Output IO Voltage	P0_7 ~ P0_0, P1_7 ~ P1_0	0	5.5	V
	Input IO Voltage	P0_7 ~ P0_0, P1_7 ~ P1_0	0	5.5	V
	IO Voltage	SCL, SDA, A1, A0, $\overline{RESET}$, $\overline{INT}$	0	5.5	V
V_{IH}	High-Level Input Voltage	SCL, SDA	0.7 × V_{CC}	V_{CC}	V
		$\overline{RESET}$, A2 ~ A0, P0_7 ~ P0_0, P1_7 ~ P1_0	0.7 × V_{CC}	V_{CC}	V
V_{IL}	Low-Level Input Voltage	SCL, SDA	−0.5	0.3 × V_{CC}	mV
		$\overline{RESET}$, A2 ~ A0, P0_7 ~ P0_0, P1_7 ~ P1_0	−0.5	0.3 × V_{CC}	mV
I_{OH}	High-Level Output Current	P0_7 ~ P0_0, P1_7 ~ P1_0		−10	mA
I_{OL}	Low-Level Output Current	P0_7 ~ P0_0, P1_7 ~ P1_0		25	mA
		$\overline{INT}$, SDA		6	mA
T_A	Operating Temperature Range		−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
TSSOP24	68	44	21	°C/W

Electrical Characteristics

All test conditions: V_{CC} = 1.65 V ~ 5.5 V, T_A = −40 ~ +125°C, unless otherwise noted.

Parameter		Conditions		Min	Typ	Max	Unit
V_{POR}	Power-on Reset Voltage, V_{CC} Rising	V_I = V_{CC} or GND; I_O = 0 mA			1.25	1.5	V
	Power-on Reset Voltage, V_{CC} Falling	V_I = V_{CC} or GND; I_O = 0 mA		0.7	1.2		V
I_{OL}	Low-level Output Current, SDA	V_{OL} = 0.4 V; V_{CC} = 1.65 V to 5.5 V		3			mA
	Low-level Output Current, $\overline{INT}$	V_{OL} = 0.4 V; V_{CC} = 1.65 V to 5.5 V		3			mA
	Low-level Output Current, P port	V_{OL} = 0.5 V; V_{CC} = 1.65 V to 5.5 V		8			mA
	Low-level Output Current, P port	V_{OL} = 0.7 V; V_{CC} = 1.65 V to 5.5 V		10			mA
V_{OH}	High-level Output Voltage, P port	I_{OH} = −8 mA; V_{CC} = 1.65 V		1.2			V
		I_{OH} = −8 mA; V_{CC} = 2.3 V (1)		1.8			V
		I_{OH} = −8 mA; V_{CC} = 3.0 V (1)		2.6			V
		I_{OH} = −8 mA; V_{CC} = 3.3 V		3.0			V
		I_{OH} = −8 mA; V_{CC} = 5.5 V		4.7			V
	High-level Output Voltage, P port	I_{OH} = −10 mA; V_{CC} = 1.65 V		1.0			V
		I_{OH} = −10 mA; V_{CC} = 2.3 V (1)		1.7			V
		I_{OH} = −10 mA; V_{CC} = 3.0 V (1)		2.5			V
		I_{OH} = −10 mA; V_{CC} = 3.3 V		2.9			V
		I_{OH} = −10 mA; V_{CC} = 5.5 V		4.5			V
I_I	Input Current: A0, A1, $\overline{RESET}$	V_I = V_{CC} or GND, V_{CC} = 1.65 V to 5.5 V		−1		1	µA
	Input Current: SCL, SDA	V_I = V_{CC} or GND, V_{CC} = 1.65 V to 5.5 V		−1		1	µA
I_{IH}	High-level Input Current: P port	V_I = V_{CC}; V_{CC} = 1.65 V to 5.5 V				1	µA
I_{IL}	Low-level Input Current: P Port	V_I = GND; V_{CC} = 1.65 V to 5.5 V		−1			µA
I_{CC}	Supply Current	Active mode, I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz	V_{CC} = 5.5 V		22.9	70	µA
			V_{CC} = 3.3 V		10.7	30	µA
			V_{CC} = 2.7 V (1)		8.2	19	µA
			V_{CC} = 1.65 V		4.7	11	µA
		Standby Mode, input low, I_O = 0 mA; I/O = inputs; f_{SCL} = 0 kHz	V_{CC} = 5.5 V		0.73	9.0	µA
			V_{CC} = 3.3 V		0.39	5.0	µA
			V_{CC} = 2.7 V (1)		0.30	4.5	µA
			V_{CC} = 1.65 V		0.16	3.5	µA
		Standby Mode, input high, I_O = 0 mA; I/O = inputs; f_{SCL} = 0 kHz	V_{CC} = 5.5 V		0.73	9.0	µA
			V_{CC} = 3.3 V		0.39	5.0	µA
			V_{CC} = 2.7 V (1)		0.30	4.5	µA
			V_{CC} = 1.65 V		0.16	3.5	µA

Parameter		Conditions	Min	Typ	Max	Unit
C_i	Input Capacitance: SCL	V_I = V_{CC} or GND; V_{CC} = 1.65 V to 5.5 V (1)		3		pF
C_{io}	Input/Output Capacitance: SDA	$V_{I/O}$ = V_{CC} or GND; V_{CC} = 1.65 V to 5.5 V (1)		3		pF
	Input/Output Capacitance: P ports	$V_{I/O}$ = V_{CC} or GND; V_{CC} = 1.65 V to 5.5 V (1)		5		pF

(1) Parameters are provided by lab bench tests and design simulation.

I²C Interface Timing Requirements

Over recommended operating free-air temperature range, unless otherwise noted. (1)

Description		Conditions	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
f_{scl}	I²C Clock Frequency		0	100	0	400	kHz
t_{sch}	I²C Clock High Time		4		0.6		μs
t_{scl}	I²C Clock Low Time		4.7		1.3		μs
t_{sp}	I²C Spike Time			50		50	ns
t_{sds}	I²C Serial-data Setup Time		250		100		ns
t_{sdh}	I²C Serial-data Hold Time		0		0		ns
t_{icr}	I²C Input Rise Time			1000	20	300	ns
t_{icf}	I²C Input Fall Time			300	20 × (V_{CC} / 5.5 V)	300	ns
t_{ocf}	I²C Output Fall Time	10-pF to 400-pF bus		300	20 × (V_{CC} / 5.5 V)	300	ns
t_{buf}	I²C Bus Free Time Between Stop and Start		4.7		1.3		μs
t_{sts}	I²C Start or Repeated Start Condition Setup		4.7		0.6		μs
t_{sth}	I²C Start or Repeated Start Condition Hold		4		0.6		μs
t_{sps}	I²C Stop Condition Setup		4		0.6		μs
$t_{vd(data)}$	Valid Data Time	SCL low to SDA output valid		3.5		0.9	μs
$t_{vd(ack)}$	Valid Data Time of ACK Condition	ACK signal from SCL low to SDA (out) low		3.5		0.9	μs
C_b	I²C Bus Capacitive Load (2)			400		400	pF

(1) All timing requirements should refer to the I²C standard, and parameters in the table are tested by the lab bench.
(2) C_b is the total capacitance of one bus line in pF.

Switching Characteristics

Over recommended operating free-air temperature range, $C_L \leq 100$ pF, unless otherwise noted.

Description		From (Input)	To (Output)	Standard Mode		Fast Mode		Unit
				Min	Max	Min	Max	
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4		4	μs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4		4	μs
t_{pv}	Output data valid; V_{CC} = 2.3 V ~ 5.5 V	SCL	P port		400		400	ns
	Output data valid; V_{CC} = 1.65 V ~ 2.3 V				400		400	ns
t_{ps}	Input data setup time	P port	SCL	150		150		ns
t_{ph}	Input data hold time	P port	SCL	1		1		μs

Parameter		Condition	min	max	Unit
$\overline{RESET}$ Timing Requirements					
t_W	Reset pulse duration		60		ns
t_{REC}	Reset recovery time		0	15	ns
t_{RESET}	Reset time	V_{CC} = 2.3 V to 5.5 V	400		ns
		V_{CC} = 1.65 V to 2.3 V	550		ns

Parameter Measurement Waveforms

I²C Interface Load Circuit and Waveforms

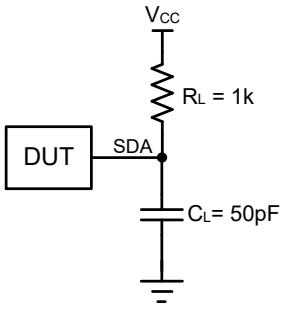


Figure 1. SDA Load Configuration

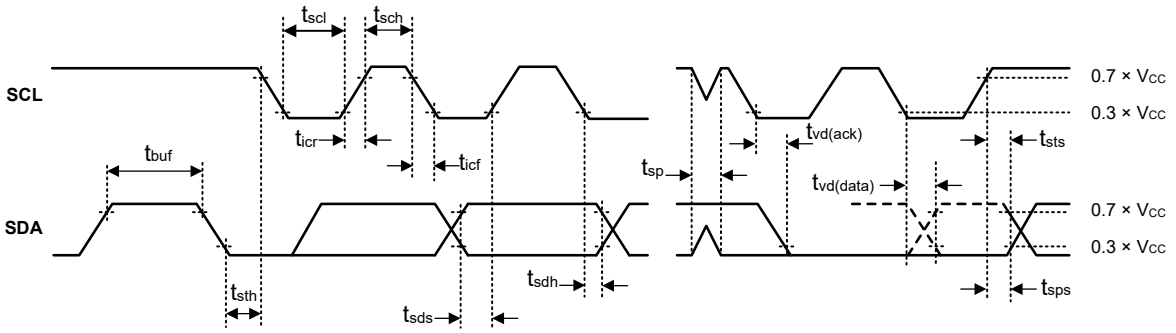


Figure 2. Definition of Timing on the I²C-bus

Interrupt Load Circuit and Waveforms

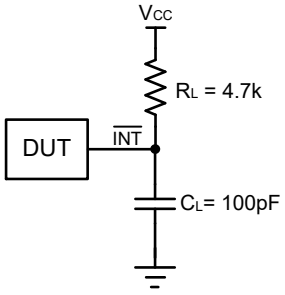


Figure 3. Interrupt Load Configuration

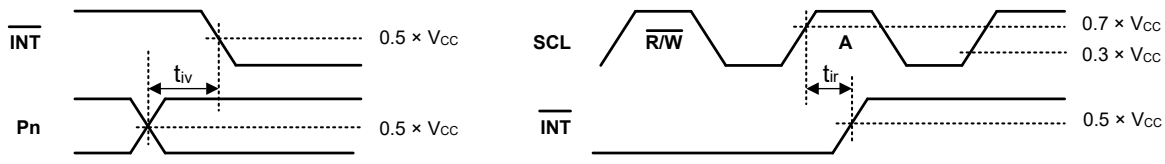


Figure 4. Definition of Interrupt Timing

P-Port Load Circuit and Waveforms

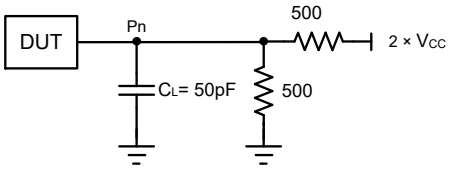


Figure 5. P-Port Load Configuration

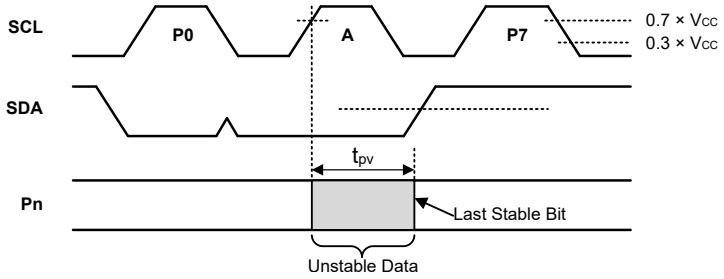


Figure 6. Definition of Write Mode Timing

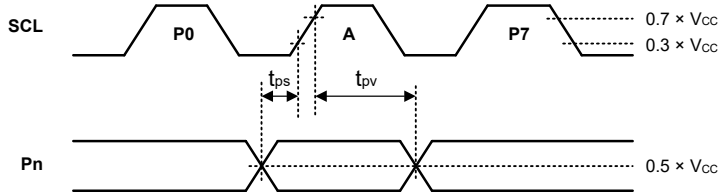


Figure 7. Definition of Read Mode Timing

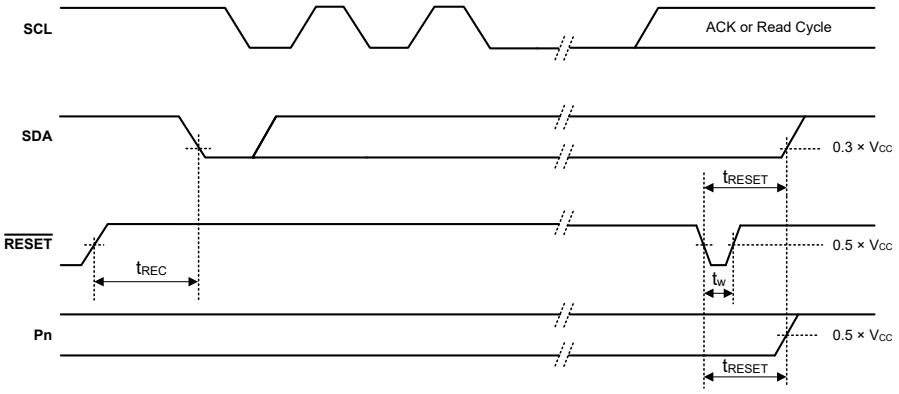


Figure 8. Definition of Reset Timing

Detailed Description

Overview

The TPT29539AQ is a 16-bit GPIO expander with interrupt and weak pull-up resistors for I²C-bus applications. The power supplier voltage ranges from 1.65 V to 5.5 V, allowing the TPT29539AQ to interconnect with 1.8 V microcontrollers.

The TPT29539AQ contains 16-bit Input and Output. The open-drain interrupt ($\overline{INT}$) output is changeable when any input state changes from its related register state. The device is used to indicate the system master that an input state has changed. $\overline{INT}$ can be connected to the interrupt input of a microcontroller. The TPT29539AQ can remain a simple slave device. The power-on reset sets the registers to their default values and initializes the device state machine. The TPT29539AQ also has a hardware $\overline{RESET}$ pin to reset the device to its default state.

All input/output pins do not have internal pull-up resistors, thus the device can save power consumption as communicating with external I/Os. Two hardware pins (A0, A1) select the fixed I²C-bus address and allow up to four devices to share the same I²C-bus.

The TPT29539AQ is available in the TSSOP24 package, and is characterized from −40°C to +125°C to meet automotive application requirements.

Functional Block Diagram

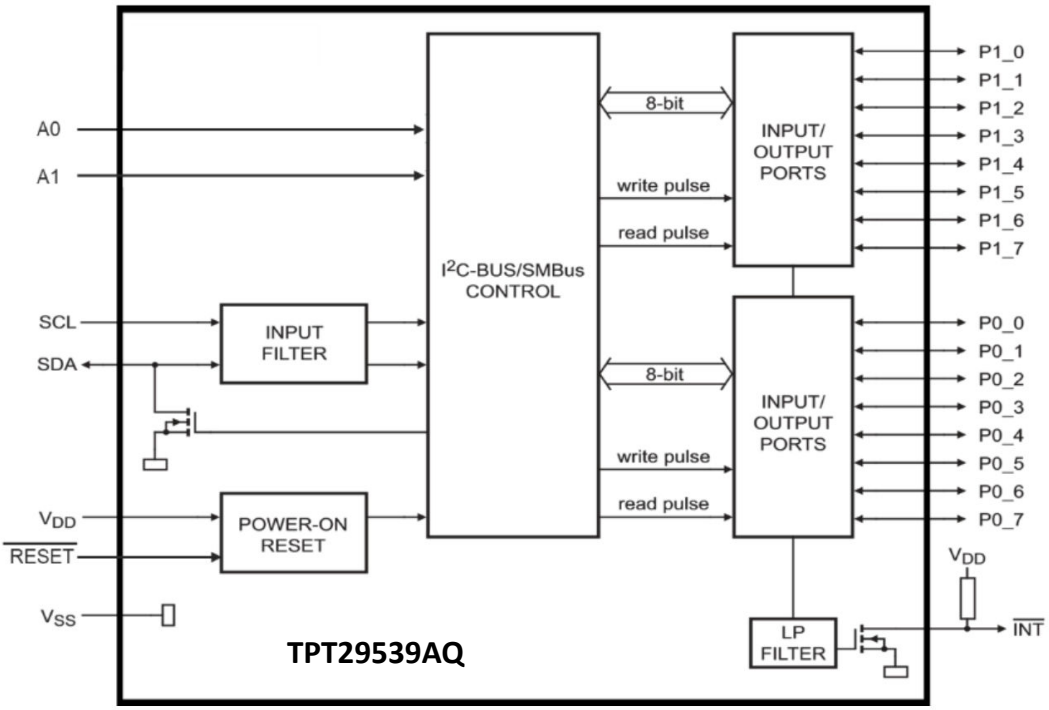


Figure 9. Functional Block Diagram

Feature Description

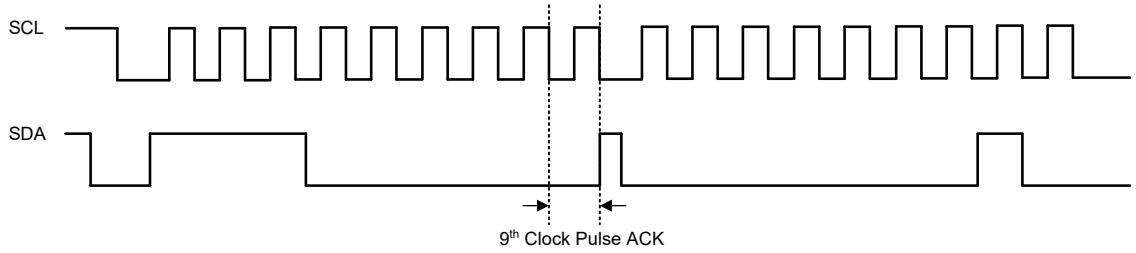


Figure 10. I²C Bus Waveform

Device Address

Following a START condition, the bus master must output the address of the slave it is accessing. All input/output pins have internal weak pull-up resistors to remove external components. Two hardware pins (A0, A1) select the fixed I²C-bus address and allow up to four devices to share the same I²C-bus. To conserve power, address pins (A0, A1) must be pulled HIGH or LOW. The address of the TPT29539AQ is shown below.

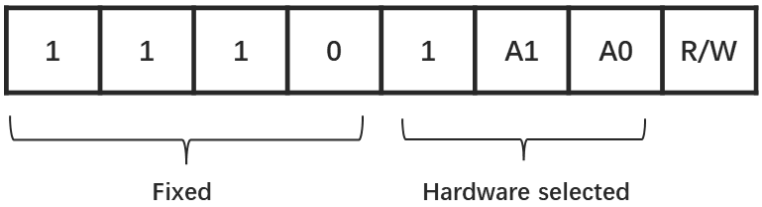


Figure 11. Slave Device Address

Control Register

Command Byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 2. Command Byte Description

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity Inversion port 0
5	Polarity Inversion port 1
6	Configuration port 0
7	Configuration port 1

Register 0 and 1: Input port registers

This register is an input-only port, which means the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3 (output port 1), and writes to this register have no effect.

The default value 'X' is determined by the externally logic level.

Table 3. Input Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 4. Input Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

Register 2 and 3: Output port registers

This register is an output-only port, which means the outcoming logic levels of the pins are defined as outputs by Register 6 (Configuration port 0) and 7 (Configuration port 1). Bit values in this register have no effect on pins defined as inputs. In fact, the value reading from this register is in the flip-flop controlling the output selection, not the actual pin value.

Table 5. Output Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 6. Output Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

Register 4 and 5: Polarity Inversion registers

This register allows the user to invert the polarity of the input port register data. If a bit in this register is set (written with '1'), the input port data polarity is inverted. If a bit in this register is cleared (written with '0'), the input port data polarity is retained.

Table 7. Polarity Inversion Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 8. Polarity Inversion Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

Register 6 and 7: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. Note that there is a high-value resistor tied to V_{DD} at each pin. At reset, the device's ports are inputs with a pull-up to V_{DD}.

Table 9. Configuration port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 10. Configuration port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

Bus Transactions

Writing to the port registers

The data is transmitted to the TPT29539AQ by sending the device address with the least significant bit set to logic '0'. The command byte is sent after the address and determines which register will receive the subsequent data.

The 8 registers of TPT29539AQ can be divided into 4 register pairs, which are the input port, output port, polarity inversion port, and configuration port, respectively. After sending data to one register, the next data byte will be sent to another register in the same pair. For example, if the first byte is sent to output port 1 (register 3), then the next byte will be stored in output port 0 (register 2). There is no limitation on the number of data bytes sent in a single write transmission. Therefore, each 8-bit register can be updated independently of the others.

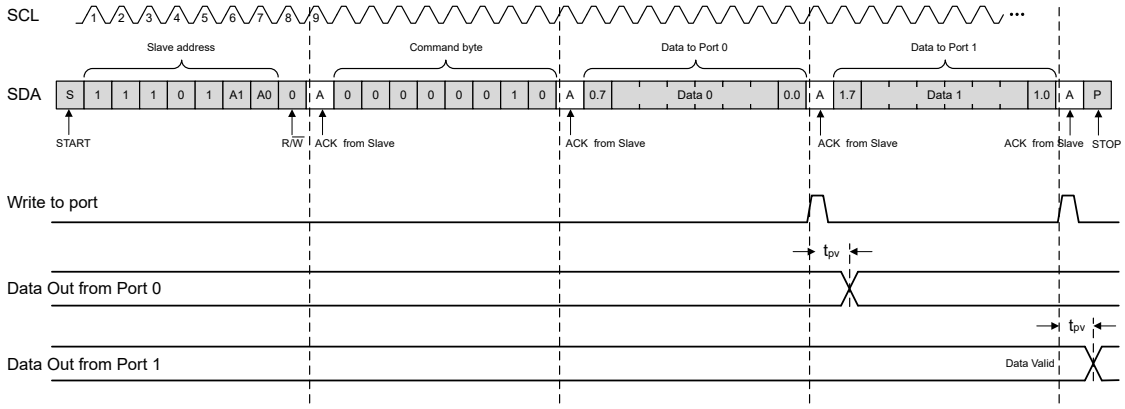


Figure 12. Write to Output Port Registers

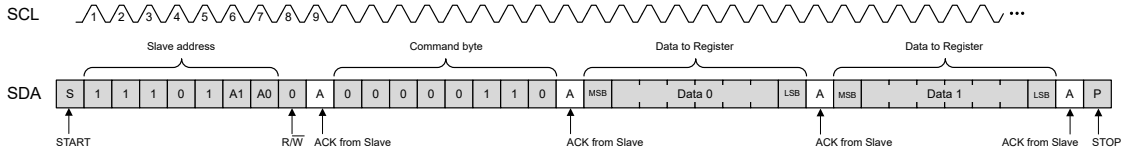


Figure 13. Write to Configuration Registers

Reading the port registers

To read data, the master device must first send the TPT29539AQ address with the least significant bit set to logic '0'. The command byte is sent following the address, determining which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to logic '1'. The TPT29539AQ will then receive the data from the register defined by the command byte. Data is clocked into the register on the rising edge of the acknowledge clock pulse. After reading the first byte, the master can continue to read data from the other register in the same pair by sending an ACK to the slave. For example, if the first byte is input port 1 (register 1), then the next byte read is input port 0 (register 0). There is no limit on the number of data bytes that can be received in one read transmission. For the last byte received, the master device must send a NACK, followed by sending a STOP condition.

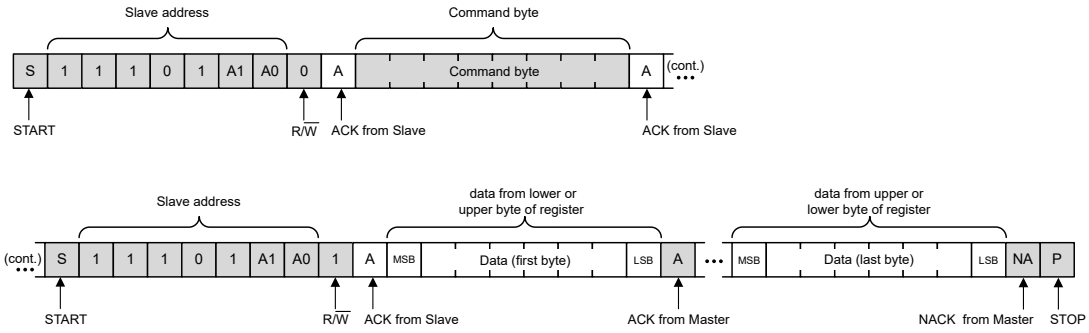


Figure 14. Read from Register

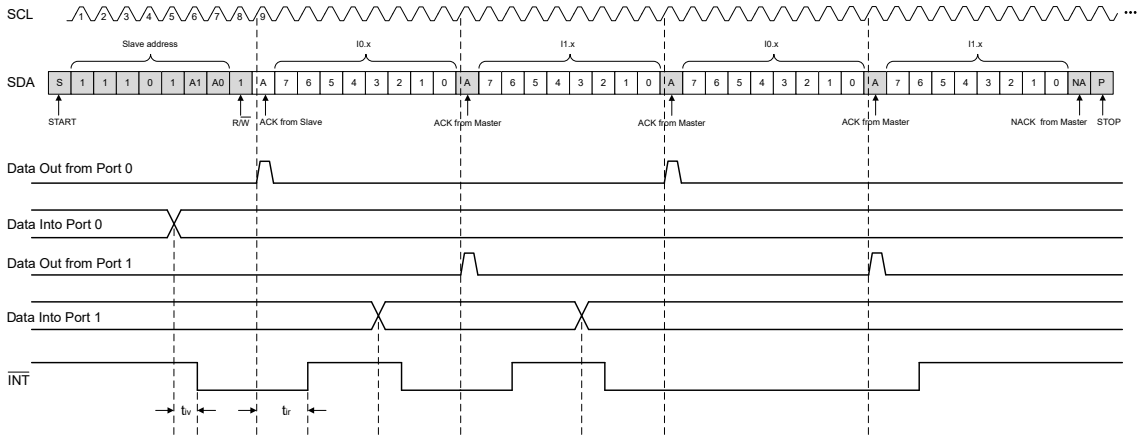


Figure 15. Read Input Port Register, Scenario 1

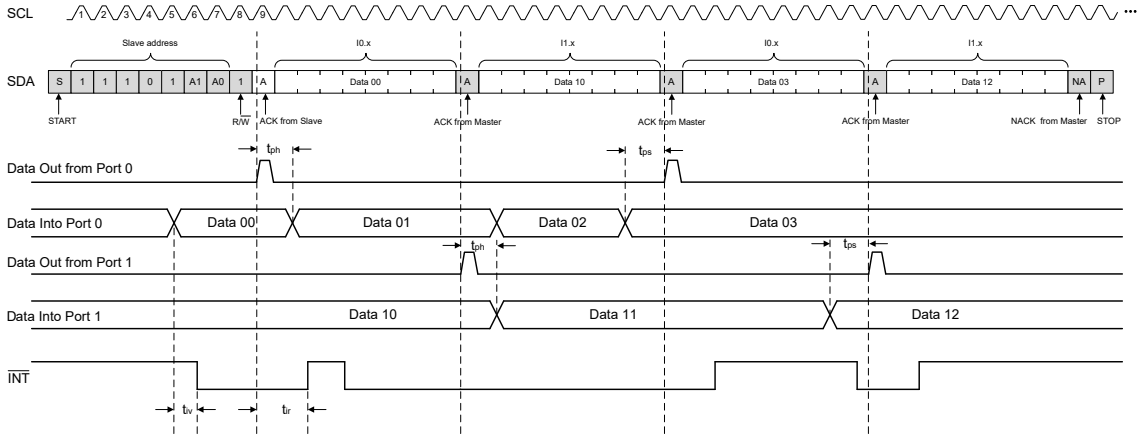


Figure 16. Read Input Port Register, Scenario 2

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT29539AQ builds in 16-bit input and output, and the interrupt $\overline{INT}$ can be connected to the interrupt input of a microcontroller, then the interrupt $\overline{INT}$ output will respond to any input state change.

IO Configuration Requirements

To make sure the TPT29539AQ can support different applications, the device is requested to set all GPIOs to a default value after or before powering up the device. Or the backup method, after powering up the TPT29539AQ, registers are reset to a default value by the digital circuit while GPIOs status are not yet stable, because there is no pull-up/pull-down resistors inside. The digital circuit is monitoring and comparing the GPIOs status to the default value of the registers in real time and when they are not matched, during the unstable period, the $\overline{INT}$ is locked. This has been confirmed in lab testing by adding time delay in seconds after powering up the TPT29539AQ (for GPIOs status to reach a stable status). After a few seconds, the $\overline{INT}$ function is ready to work, and the performance is exactly as designed. The delay time will depend on the different capacitances on board.

Typical Application

One application of the TPT29539AQ device is used as below.

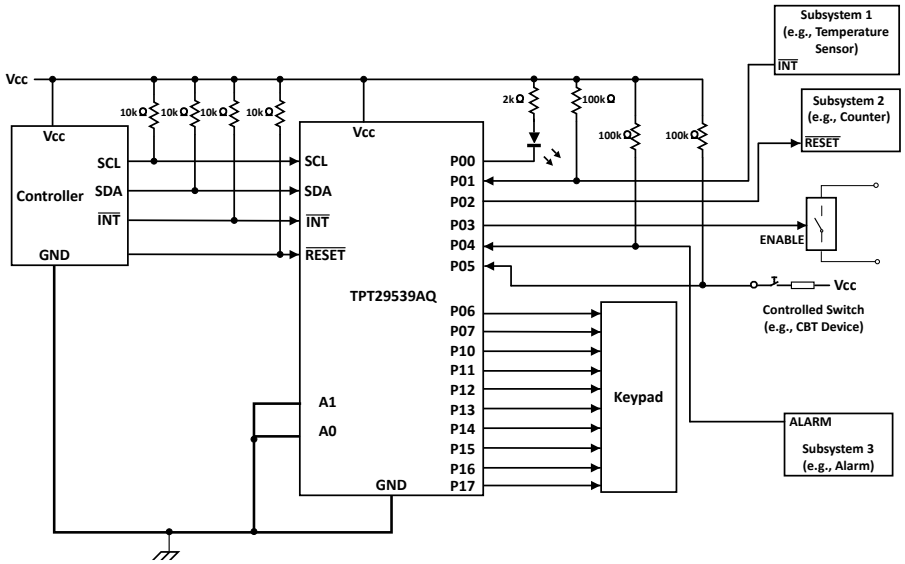


Figure 17. Typical Application Reference Circuit

Layout

Layout Guideline

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they will have to turn corners. Figure 18 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains a constant trace width and minimizes reflections.

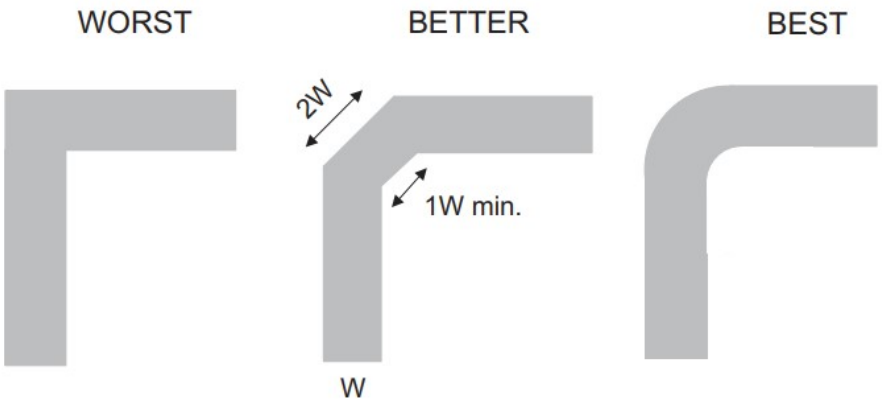


Figure 18. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Layout Example

Figure 19 illustrates an example of a PCB layout with the TPT29539AQ. Some key considerations are as follows:

- Decouple the V_{CC} pin with a 0.1-μF capacitor, and place it as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{CC} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

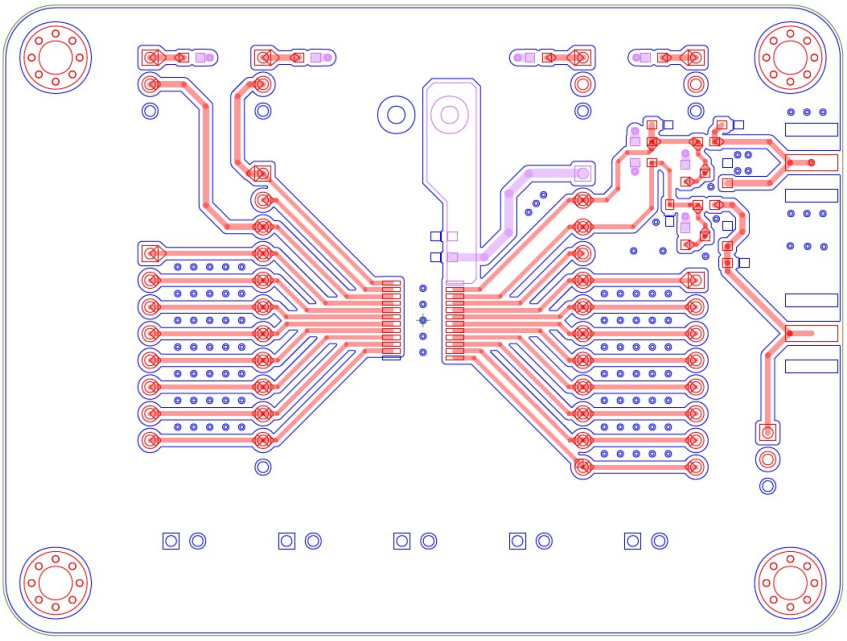
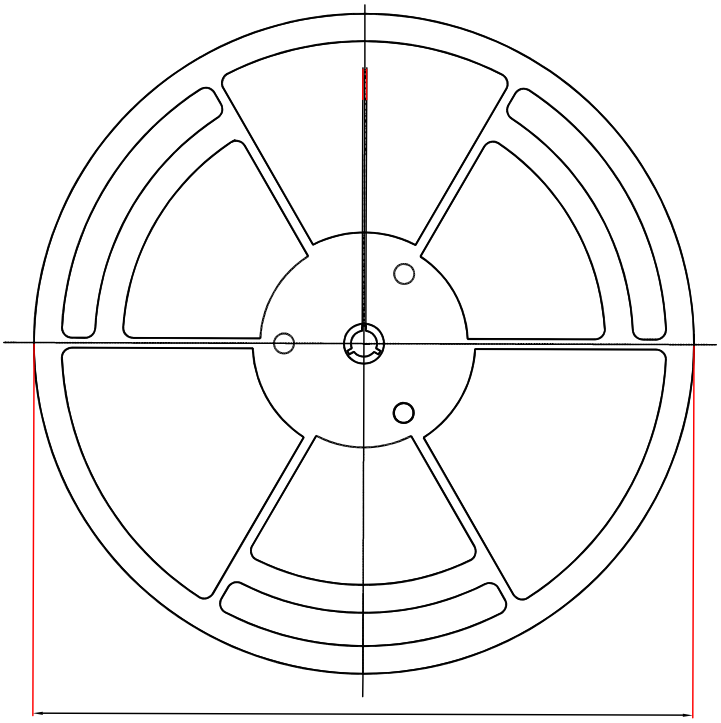
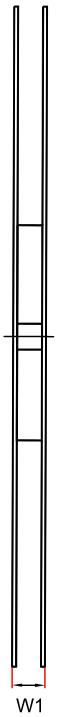
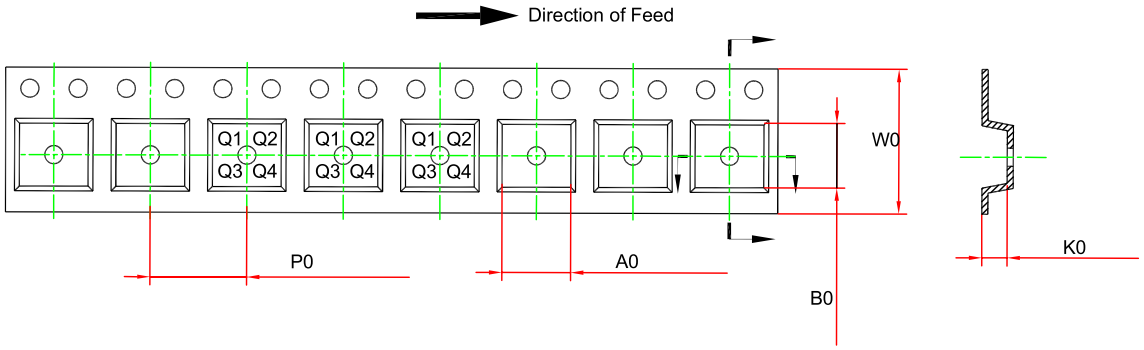


Figure 19. TPT29539AQ Layout Example

Tape and Reel Information





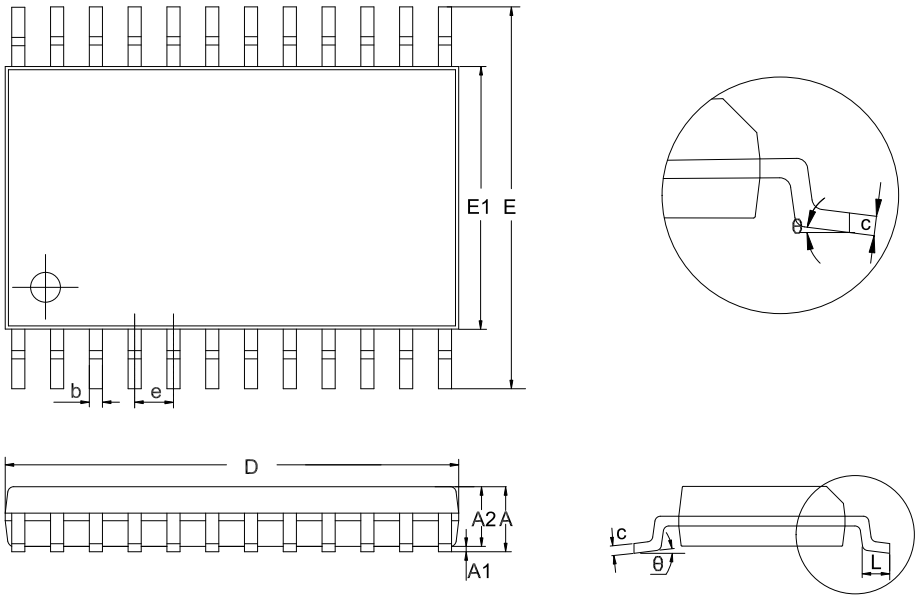


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT29539AQ-TS5R-S	TSSOP24	330	21.6	6.8	8.3	1.6	8	16	Q1

Package Outline Dimensions

TSSOP24

Package Outline Dimensions TS5(TSSOP-24-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	7.700	7.900	0.303	0.311
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29539AQ-TS5R-S	−40 to 125°C	TSSOP24	9539Q	MSL3	4,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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