I²C to 4-Bit GPIO Expander

Features

- I²C-Bus to 4-Bit GPIO Expander
- Operating Power Supply Voltage from 1.65 V to 5.5 V
- Low Standby Current
- 400-kHz Fast-Mode I²C Bus
- 5-V Tolerant I/Os
- Polarity Inversion Register
- Noise Filter on SCL/SDA Inputs
- Internal Power-on Reset
- Power-up with All Channels Configured as Inputs with Weak Pull-up Resistors
- ESD Protection Exceeds JESD 22
  - 3000-V Human Body Model
  - 1500-V Charged-Device Model

Description

The TPT29536A is a 4-bit GPIO expander with interruption and weak pull-up resistors for I²C-bus applications. The power supplier voltage range is from 1.65 V to 5.5 V, allowing the TPT29536A to interconnect with 1.8-V microcontrollers.

The TPT29536A contains the register of 4-bit Configuration, Input, Output, and Polarity Inversion registers. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The power-on reset sets the registers to their default values and initializes the device state machine.

All input/output pins have internal weak pull-up resistors to remove external components.

TPT29536A is available in the MSOP8 package.

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers

Typical Application Circuit

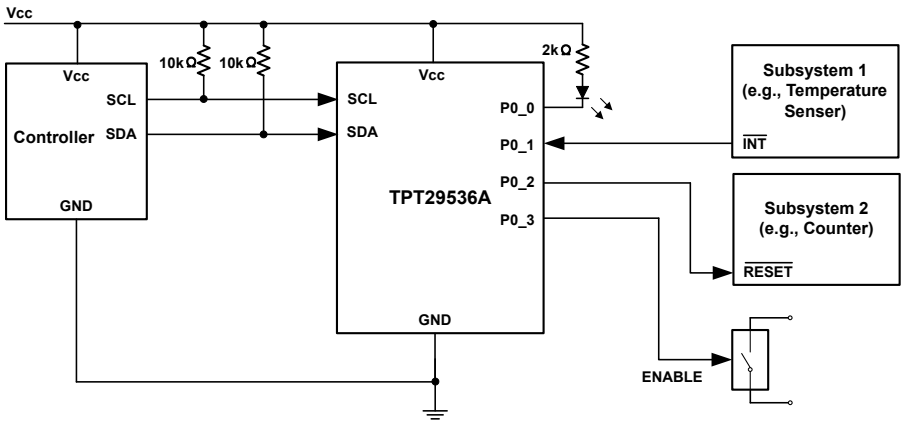

Table of Contents

Revision History

Date	Revision	Notes
2024-09-14	Rev.P.0	Initial version
2024-11-20	Rev.A.0	Released version

Pin Configuration and Functions

MSOP8 Package
Top View

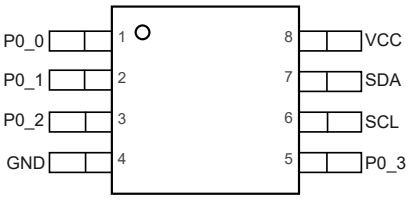

Table 1. Pin Functions: TPT29536A

Pin	Name	I/O	Description
4	GND	GND	Ground
1	P0_0	I/O	P-port I/O. Push-pull design structure. At power on, P0_0 is configured as an input
2	P0_1	I/O	P-port I/O. Push-pull design structure. At power on, P0_1 is configured as an input
3	P0_2	I/O	P-port I/O. Push-pull design structure. At power on, P0_2 is configured as an input
5	P0_3	I/O	P-port I/O. Push-pull design structure. At power on, P0_3 is configured as an input
6	SCL	Input	Serial clock bus. Connect to VCC through a pull-up resistor
7	SDA	Input	Serial data bus. Connect to VCC through a pull-up resistor
8	VCC	Supply	Supply voltage

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	−0.5	6	V
V_I	Input Voltage	−0.5	6	V
V_O	Output Voltage	−0.5	6	V
I_{IK}	Input Clamp Current, $V_I < 0$		−20	mA
I_{OK}	Output Clamp Current, $V_O < 0$		−20	mA
I_{IOK}	Input-Output Clamp Current, $V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous Output Low Current, V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous Output High Current, V_O = 0 to V_{CC}		−50	mA
I_{CC}	Continuous Current through GND		−250	mA
	Continuous Current through V_{CC}		160	mA
T_J	Maximum Junction Temperature		150	°C
T_{stg}	Storage Temperature	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±3	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Over-operating free-air temperature range (unless otherwise noted).

Parameter			Min	Max	Unit
V_{CC}	Supply Voltage		1.65	5.5	V
V_{IH}	High-Level Input Voltage	SCL, SDA	0.7 × V_{CC}	V_{CC}	V
		P0_3 ~ P0_0	0.7 × V_{CC}	5.5	V
V_{IL}	Low-Level Input Voltage	SCL, SDA	−0.5	0.3 × V_{CC}	V
		P0_3 ~ P0_0	−0.5	0.3 × V_{CC}	V
I_{OH}	High-Level Output Current	P0_3 ~ P0_0		−10	mA
I_{OL}	Low-Level Output Current	P0_3 ~ P0_0		25	mA
		SDA		6	mA
T_A	Operating Temperature Range	V_{CC} = 1.65 ~ 3.6 V	−40	125	°C
		V_{CC} = 4.5 ~ 5.5 V	−40	105	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as the minimum, is used in this datasheet.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP8	148.7	48.4	°C/W

Electrical Characteristics

All test conditions: V_{CC} = 1.65 V ~ 3.6 V, T_A = −40 ~ +125°C; V_{CC} = 4.5 V ~ 5.5 V, T_A = −40 ~ +105°C, unless otherwise noted.

Parameter		Conditions		Min	Typ	Max	Unit
Input Electrical Specifications							
V_{POR}	Power-on Reset Voltage, V_{CC} Rising	V_I = V_{CC} or GND; I_O = 0 mA			1.25	1.5	V
	Power-on Reset Voltage, V_{CC} Falling	V_I = V_{CC} or GND; I_O = 0 mA		0.7	1.2		V
I_{OL}	Low-Level Output Current, SDA	V_{OL} = 0.4 V; V_{CC} = 1.65 V to 5.5 V		3			mA
V_{OL}	Low-Level Output Voltage, P port	I_{OL} = 8 mA; V_{CC} = 1.65 V				0.5	V
		I_{OL} = 8 mA; V_{CC} = 2.3 V				0.5	V
		I_{OL} = 8 mA; V_{CC} = 3.0 V				0.5	V
		I_{OL} = 8 mA; V_{CC} = 4.5 V				0.5	V
	Low-Level Output Voltage, P port	I_{OL} = 10 mA; V_{CC} = 1.65 V				0.7	V
		I_{OL} = 10 mA; V_{CC} = 2.3 V				0.7	V
		I_{OL} = 10 mA; V_{CC} = 3.0 V				0.7	V
		I_{OL} = 10 mA; V_{CC} = 4.5 V				0.7	V
V_{OH}	High-Level Output Voltage, P port	I_{OH} = −8 mA; V_{CC} = 1.65 V		1.2			V
		I_{OH} = −8 mA; V_{CC} = 2.3 V		1.8			V
		I_{OH} = −8 mA; V_{CC} = 3.0 V		2.6			V
		I_{OH} = −8 mA; V_{CC} = 4.75 V		4.1			V
	High-Level Output Voltage, P port	I_{OH} = −10 mA; V_{CC} = 1.65 V		1.0			V
		I_{OH} = −10 mA; V_{CC} = 2.3 V		1.7			V
		I_{OH} = −10 mA; V_{CC} = 3.0 V		2.5			V
		I_{OH} = −10 mA; V_{CC} = 4.75 V		4.0			V
I_I	Input Current: SCL, SDA	V_{CC} = 1.65 V to 5.5 V, V_I = V_{CC} or GND		−1		1	μA
I_{IH}	High-Level Input Current: P port	V_I = V_{CC}; V_{CC} = 1.65 V to 5.5 V				1	μA
I_{IL}	Low-Level Input Current: P port	V_I = GND; V_{CC} = 1.65 V to 5.5 V		−100			μA
I_{cc}	Supply Current	Active mode, IO = 0 mA; I/O = inputs; f_{SCL} = 400 kHz	V_{CC} = 5.5 V		22.7	26	μA
			V_{CC} = 3.6 V		12	14	μA
			V_{CC} = 2.7 V		8.2	10	μA
			V_{CC} = 1.95 V		5.6	7	μA
		Standby Mode, input low, IO = 0 mA; I/O = inputs; fS_{SCL} = 0 kHz	V_{CC} = 5.5 V		0.22	0.29	mA
			V_{CC} = 3.6 V		0.15	0.2	mA
			V_{CC} = 2.7 V		0.11	0.16	mA

Parameter		Conditions		Min	Typ	Max	Unit
			V_{CC} = 1.95 V		0.08	0.11	mA
		Standby Mode, input high, IO = 0 mA; I/O = inputs; f_{SCL} = 0 kHz	V_{CC} = 5.5 V		0.73	1.5	µA
			V_{CC} = 3.6 V		0.43	1.2	µA
			V_{CC} = 2.7 V		0.3	1	µA
			V_{CC} = 1.95 V		0.19	0.95	µA
C_i	Input Capacitance	V_I = V_{CC} or GND; V_{CC} = 1.65 V to 5.5 V (1)			3		pF
C_{io}	Input/Output Capacitance	$V_{I/O}$ = V_{CC} or GND; V_D = 1.65 V to 5.5 V (1)			3		pF
		$V_{I/O}$ = V_{CC} or GND; V_{CC} = 1.65 V to 5.5 V (1)			5		pF

(1) Parameters are provided by lab bench tests and design simulation. Not tested in production.

I²C Interface Timing Requirements (1)

Over recommended operating free-air temperature range, unless otherwise noted.

Description		Conditions	Standard Mod		Fast Mode		Unit
			Min	Max	Min	Max	
fscl	I²C clock frequency		0	100	0	400	kHz
tsch	I²C clock high time		4		0.6		μs
tscl	I²C clock low time		4.7		1.3		μs
tsp	I²C spike time			50		50	ns
tsds	I²C serial-data setup time		250		100		ns
tsdh	I²C serial-data hold time		0		0		ns
ticr (2)	I²C input rise time			1000	20	300	ns
Ticf (3)	I²C input fall time			300	20 × (V_{CC}/ 5.5 V)	300	ns
tocf (3)	I²C output fall time	10-pF to 400-pF bus		300	20 × (V_{CC}/ 5.5 V)	300	ns
tbuf	I²C bus free time between stop and start		4.7		1.3		μs
tsts	I²C start or repeated start condition setup		4.7		0.6		μs
tsth	I²C start or repeated start condition hold		4		0.6		μs
tsps	I²C stop condition setup		4		0.6		μs
tvd(data)	Valid data time	SCL low to SDA output valid		3.5		0.9	μs
tvd(ack)	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.5		0.9	μs
Cb	I²C bus capacitive load			400		400	pF

(1) All timing requirements should refer to the I²C standard, and all parameters in the table are NOT tested in production.
(2) ticr is decided by input signal rising time.
(3) Data is provided by bench validation, test condition: 150 ohm series resistor connect to SDA pin, then 2.2 Kohm pull up to VCC, 150 pF Cload pull down to GND, t_{icr} = 29 ns, t_{ocf} = 25 ns, V_{OL} = 166 mv

Switching Characteristics

Over recommended operating free-air temperature range, C_L ≦ 100 pF, unless otherwise noted.

Description		From (Input)	To (Output)	Standard Mod		Fast Mode		Unit
				Min	Max	Min	Max	
tpv	Output data valid; For V_{CC} = 2.3 V ~ 5.5 V	SCL	P port		400		400	ns
	Output data valid; For V_{CC} = 1.65 V ~ 2.3 V				400		400	ns
tps	Input data setup time	P port	SCL	150		150		ns
tph	Input data hold time	P port	SCL	1		1		µs

Parameter Measurement Waveforms

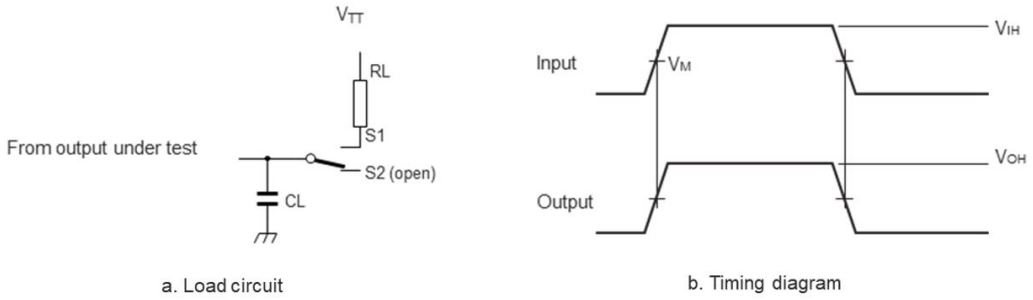

Figure 1. Load Circuit for Outputs

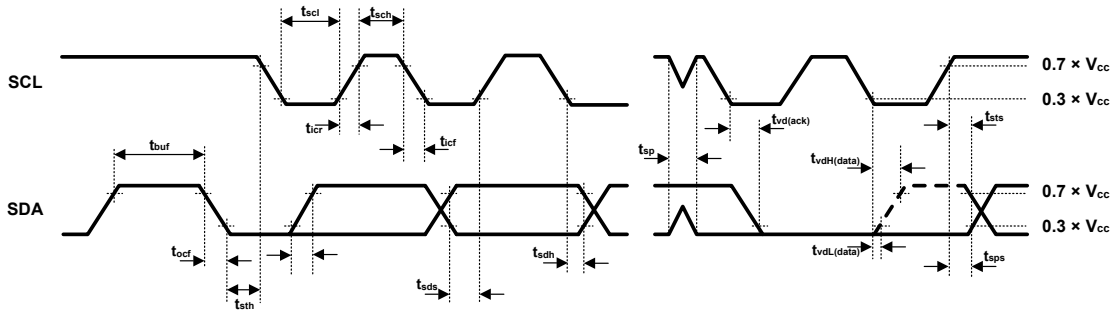

Figure 2. Definition of Timing on the I²C-bus

Typical Performance Characteristics

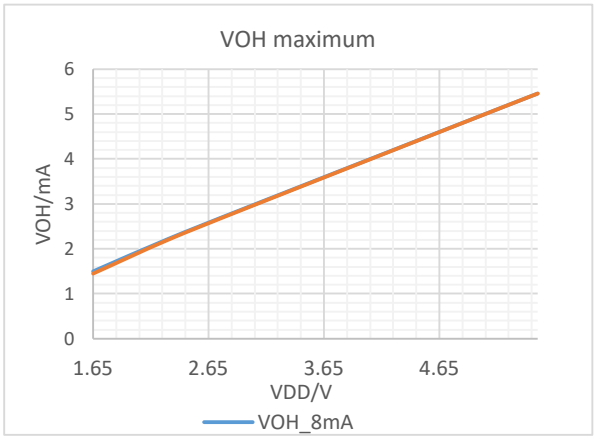

Figure 3. VOH Maximum Measurement

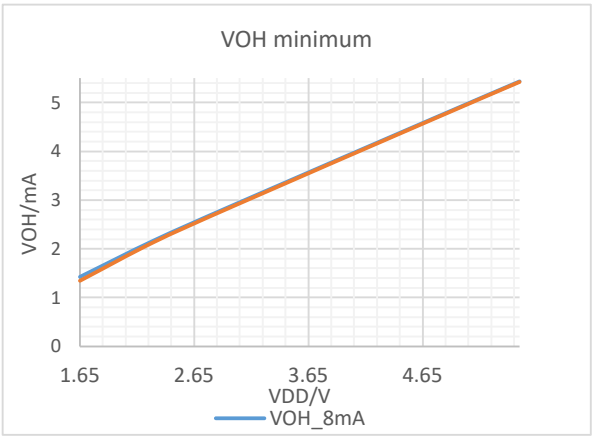

Figure 4. VOH Minimum Measurement

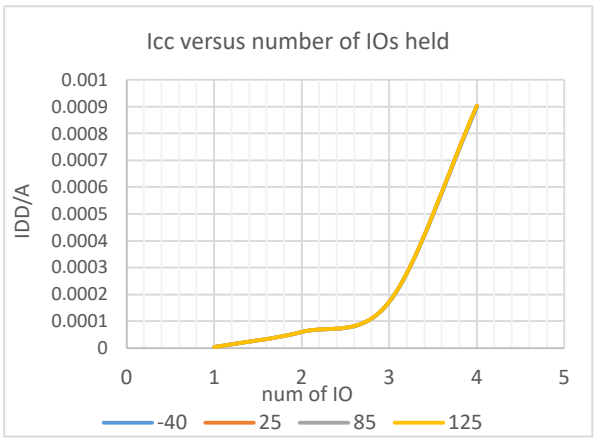

Figure 5. I_{CC} versus Number of I/Os Measurement

Detailed Description

Overview

The TPT29536A is a 4-bit GPIO expander with interruption and weak pull-up resistors for I²C-bus applications. The power supplier voltage range is from 1.65 V to 5.5 V, allowing the TPT29536A to interconnect with 1.8-V microcontrollers.

The TPT29536A contains the register of 4-bit Configuration, Input, Output, and Polarity Inversion registers. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The power-on reset sets the registers to their default values and initializes the device state machine.

All input/output pins have internal weak pull-up resistors to remove external components.

Functional Block Diagram

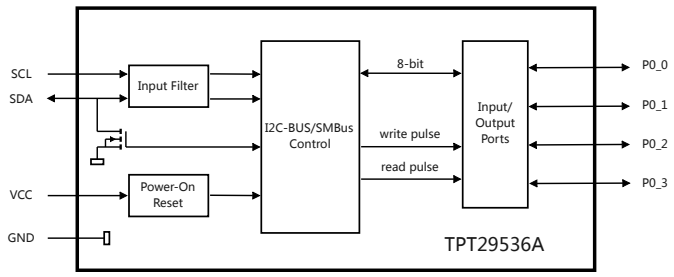

Figure 6. Functional Block Diagram

Feature Description

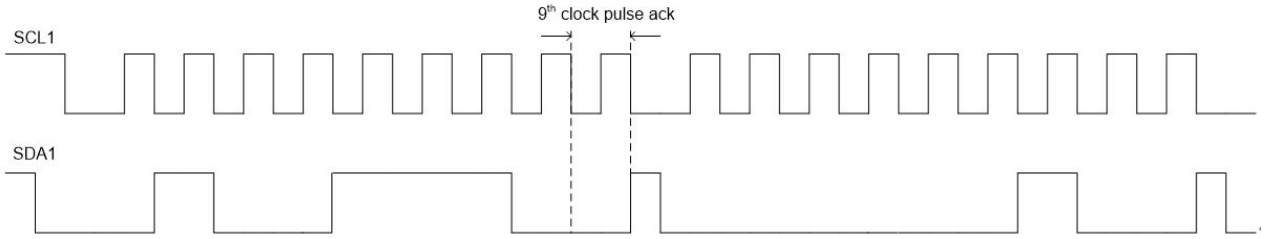

Figure 7. I²C BUS (1.65 V ~ 5.5 V) Waveform

5-V Tolerant I/O Ports

The TPT29536A supports the I/O voltage from 1.8 V to 5 V and allows the TPT29536A to connect to kinds of devices with I/O communication. To minimize the current consumption, suggest the input signal should meet the VIH and VIL spec in the Electrical Characteristics table. There is a weak pull-up resistor inside, and 100-K ohm for each I/O port. The user can choose certain value pull-up resistors external circuits depending on different applications.

When an I/O is configured as an input, creating a high-impedance input with a weak pull-up (100 kΩ typical) to V_{CC}. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, depending on the state of the Output Port register. The low-impedance paths that exist between the pin and either VCC or GND, as the external voltage is applied to an I/O configured as an output.

Power-on Reset

When power is connected to TPT29536A V_{CC}, an internal Power-On Reset (POR) is in a reset condition until V_{CC} has reached V_{POR}. At this point, the reset condition is released, and the TPT29536A registers and state machine set up to their default states. The V_{CC} must be lowered below V_{PORF} to reset the device and then restored to the operating voltage.

Device Address

Following a START condition, the bus master must output the address of the slave it is accessing. The TPT29536A has a fixed address shown as below.

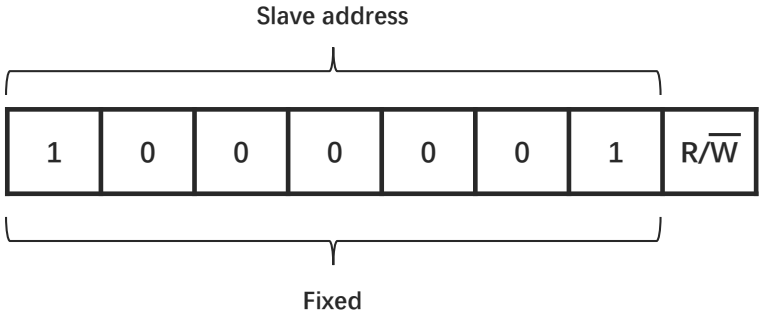

Figure 8. Slave Device Address

Control Register

Command Byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers is written or read.

Table 2. Command Byte Description

Command	Protocol	Function
0	Read byte	Input Port register
1	Read/write byte	Output Port register
2	Read/write byte	Polarity Inversion register
3	Read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Register 0: Input port registers

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default 'X' is determined by the externally applied logic level, normally logic 1 when no external signal is externally applied because of the internal pull-up resistors.

Table 3. Register 0: Input Port register bit description

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Access	read only	read only	read only	read only	read only	read only	read only	read only
Default	1	1	1	1	X	X	X	X
Description	Not used				Determined by externally applied logic level			

Register 1: Output port registers

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, not the actual pin value.

'Not used' bits can be programmed with either logic 0 or logic 1.

Table 4. Register 1: Output Port Register Bit Description

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1
Description	Not used				Reflects outgoing logic levels of pins defined as outputs by Register 3			

Register 2: Polarity Inversion registers

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

'Not used' bits can be programmed with either logic 0 or logic 1.

Table 5. Register 2: Polarity Inversion register bit description

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Description	Not used				Inverts polarity of Input port register data: 0 = Input port register data retained (default value); 1 = Input port register data inverted			

Register 3: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared (written with '0'), the

corresponding port pin is enabled as an output. Note that there is a high-value resistor tied to V_{DD} at each pin. At reset, the ports of the devices are inputs with a pull-up to V_{DD}.

'Not used' bits can be programmed with either logic 0 or logic 1.

Table 6. Register 3: Configuration Register bit description

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1
Description	Not used				Configures the directions of the I/O pins: 0 = corresponding port pin enabled as an output; 1 = corresponding port pin configured as input (default value)			

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT29536A is a 4-bit GPIO expander with interruption and weak pull-up resistors for I²C-bus applications. The power supplier voltage range is from 1.65 V to 5.5 V, allowing the TPT29536A to interconnect with 1.8-V microcontrollers.

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All input/output pins have internal weak pull-up resistors to remove external components.

Typical Application

The following figure shows an application in which the TPT29536A can be used to control multiple subsystems and read inputs from buttons.

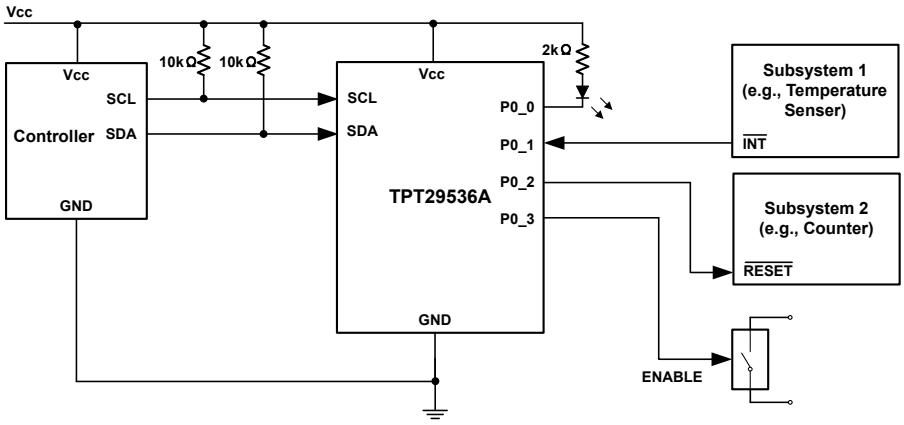


Figure 9. Typical Application Reference Circuit

Layout

Layout Guideline

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they have to turn corners. Figure 10 shows progressively better techniques for rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

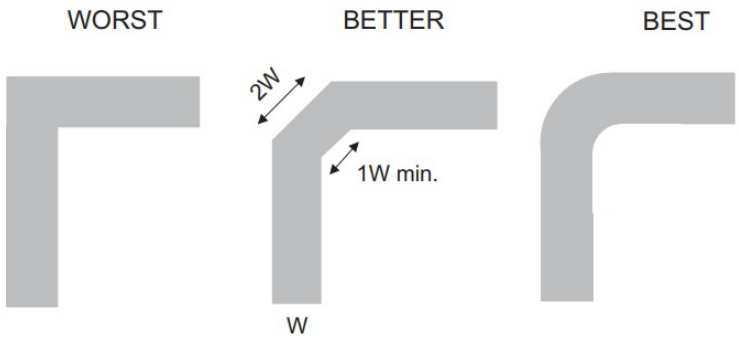


Figure 10. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Layout Example

Figure 11 illustrates an example of a PCB layout with the TPT29536A. Some key considerations are as follows:

- Decouple the VDD pin with a 0.1-μF capacitor, and place it as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the VDD supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

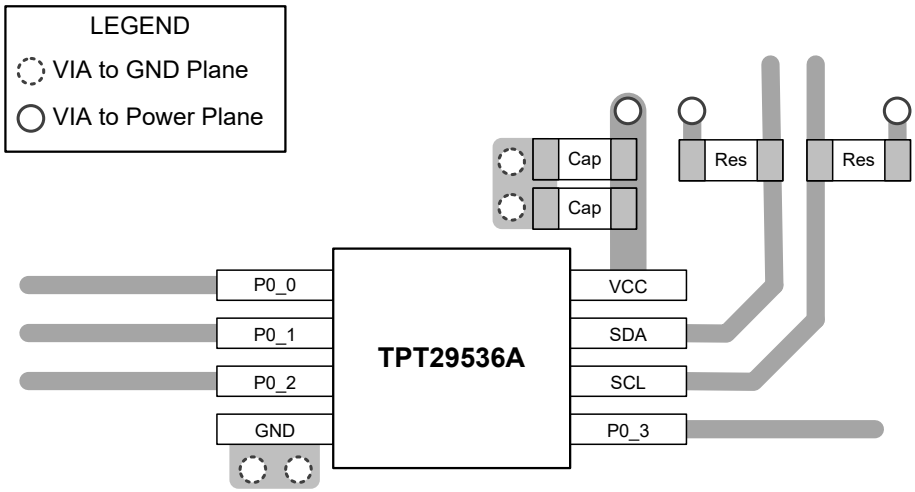
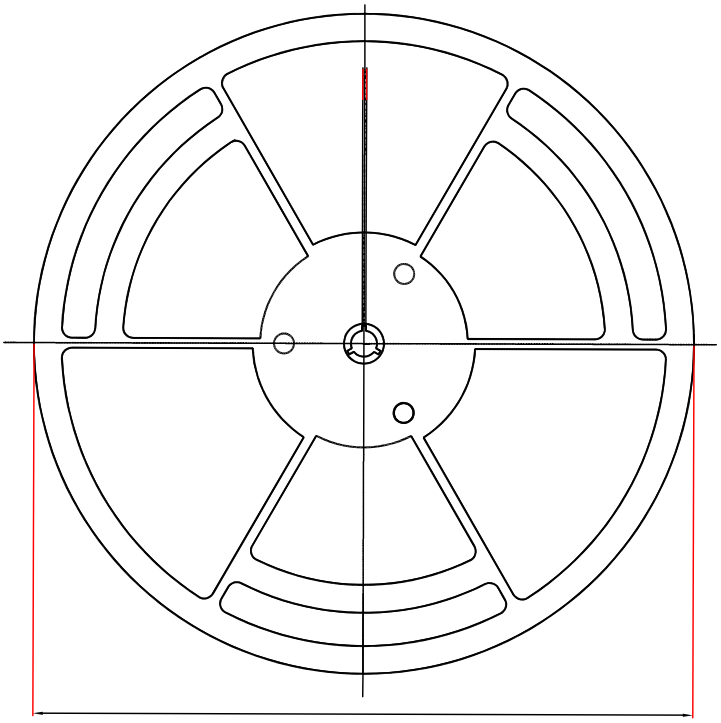
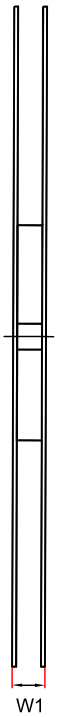
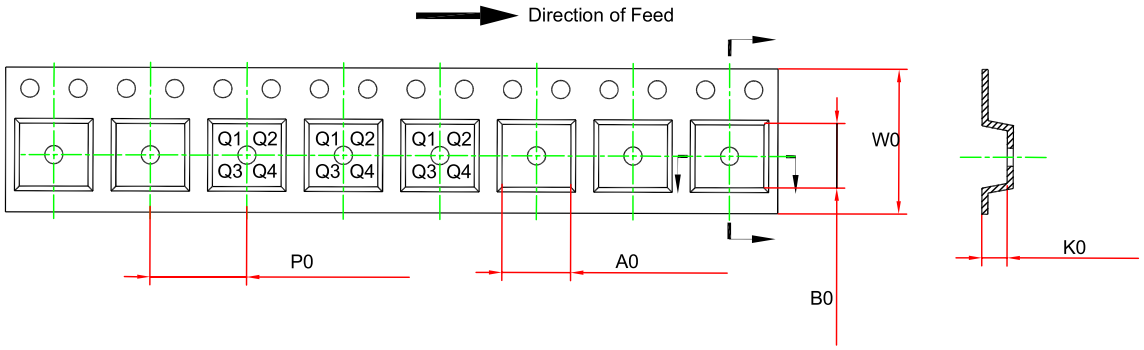


Figure 11. TPT29536A Layout Example

Tape and Reel Information





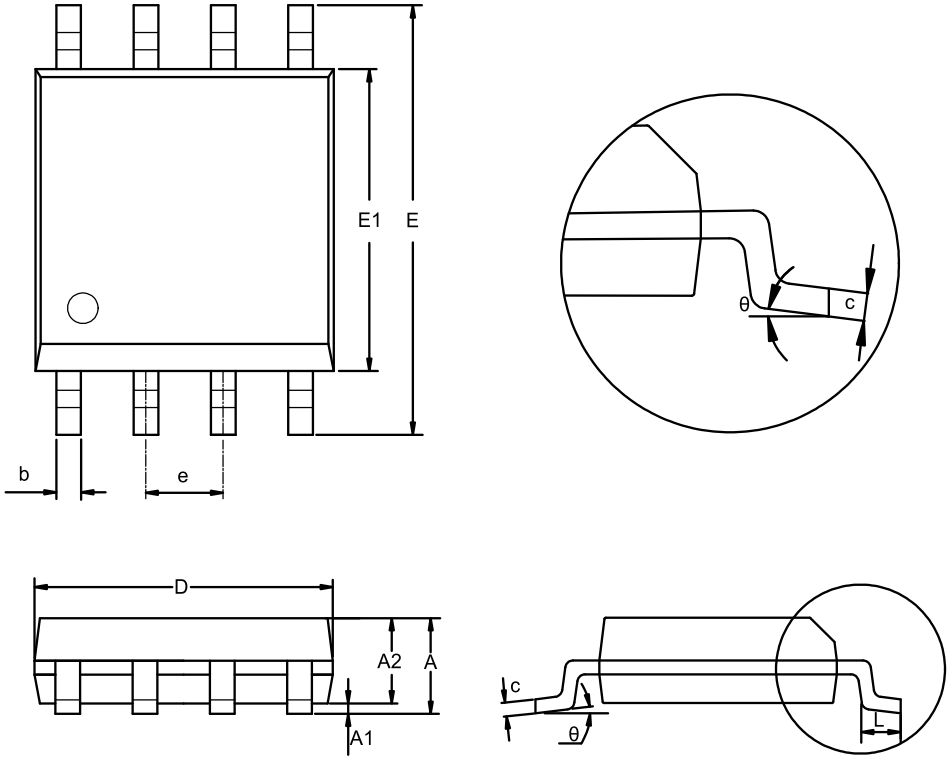


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPT29536A-VS1R	MSOP8	330.0	5.3	1.3	12.0	17.6	3.4	8.0	Q1

Package Outline Dimensions

MSOP8

Package Outline Dimensions VS1(MSOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29536A-VS1R	−40 to 125°C	MSOP8	9536A	MSL1	3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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