# I²C to 16-bit GPIO Expander with Interrupt

## Features

- I²C-Bus to 16-bit GPIO Expander
- Operating Supply Voltage from 1.65 V to 5.5 V
- Low Standby Current
- 400-kHz Fast-mode I²C-Bus
- 5-V Tolerant I/O Ports
- No Internal Pull-up Resistor
- Open-Drain Active Low Interrupt Output ($\overline{INT}$)
- Configurable Slave Address with 3 Address Pins
- Internal Power-on Reset
- Power-up with all Channels Configured as Inputs
- ESD Protection Exceeds JESD 22
  - ±2000-V Human Body Model
  - ±1500-V Charged Device Model

## Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers

## Description

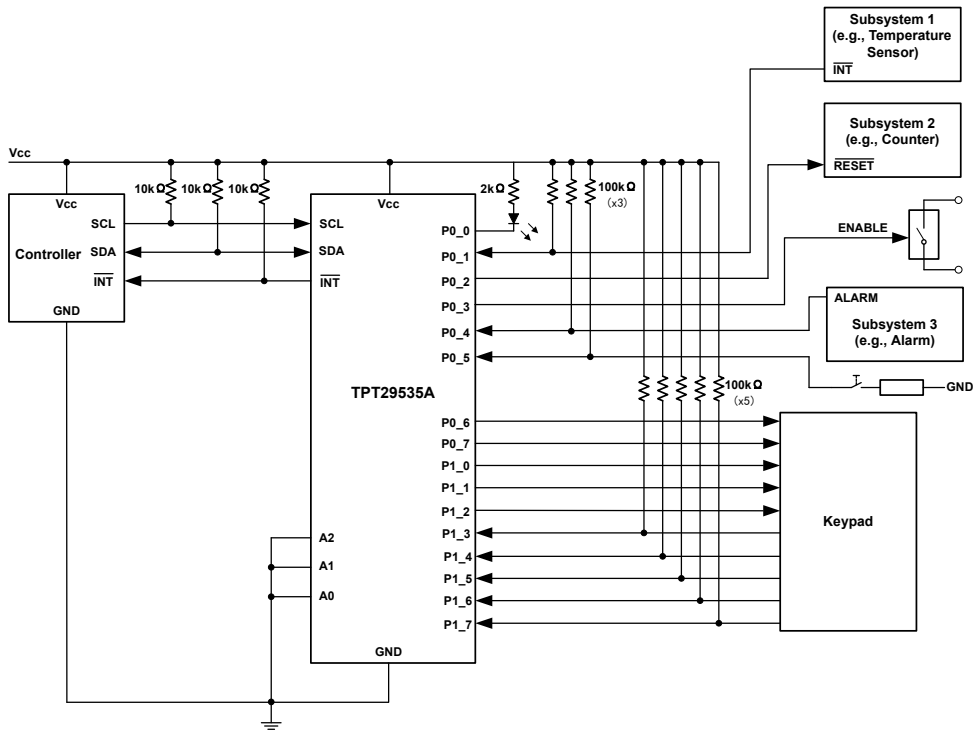
The TPT29535A is a 16-bit GPIO expander with interrupt for I²C-Bus applications. The power supply voltage ranges from 1.65 V to 5.5 V, allowing the TPT29535A to interconnect with 1.8-V microcontrollers.

The TPT29535A provides 16-bit Input/output (I/O) ports. The open-drain interrupt ($\overline{INT}$) output is asserted when any input state changes from its related register state. The device is used to indicate to the system master that an input state has changed. The $\overline{INT}$ can be connected to the interrupt input of a microcontroller. The power-on reset sets the registers to their default values and initializes the device state machine.

All input/output pins do not have internal pull-up resistors; thus the device can reduce power consumption when communicating with external I/Os. Three hardware pins (A0, A1, A2) select the configured I²C-Bus address and allow up to eight devices to share the same I²C-Bus.

The TPT29535A is available in TSSOP24 and QFN4X4-24 packages, and is characterized from −40°C to +125°C.

## Typical Application Circuit



# Table of Contents

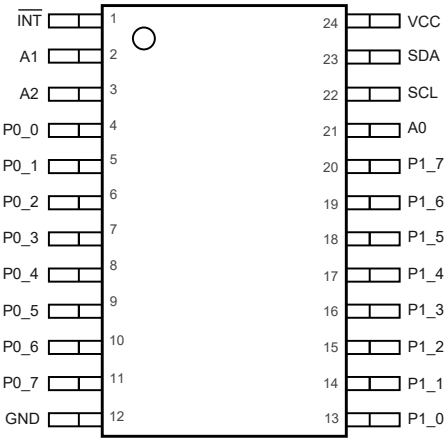
**Features** ..... 1
**Applications** ..... 1
**Description** ..... 1
**Typical Application Circuit** ..... 1
**Revision History** ..... 3
**Pin Configuration and Functions** ..... 4
**Specifications** ..... 6
Absolute Maximum Ratings (1) ..... 6
ESD, Electrostatic Discharge Protection ..... 6
Recommended Operating Conditions ..... 7
Thermal Information ..... 7
Electrical Characteristics ..... 8
I²C Interface Timing Requirements ..... 10
Switching Characteristics ..... 11
Typical Performance Characteristics ..... 12
Parameter Measurement Waveforms ..... 15
**Detailed Description** ..... 17
Overview ..... 17
Functional Block Diagram ..... 17
Feature Description ..... 17
Device Address ..... 18
Registers Map ..... 18
Bus Transactions ..... 21
**Application and Implementation** ..... 23
Application Information ..... 23
Typical Application ..... 23
I²C-Bus Pull-up Resistance ..... 24
**Layout** ..... 25
Layout Guideline ..... 25
Layout Example ..... 25
**Tape and Reel Information** ..... 27
**Package Outline Dimensions** ..... 28
TSSOP24 ..... 28
QFN4X4-24 ..... 29
**Order Information** ..... 30
**IMPORTANT NOTICE AND DISCLAIMER** ..... 31

## Revision History

| Date | Revision | Notes |
|---|---|---|
| 2026-05-20 | Rev.A.0 | Released version. |

## Pin Configuration and Functions

TPT29535A
TSSOP24 Package
Top View




TPT29535A
QFN4X4-24 Package
Top View

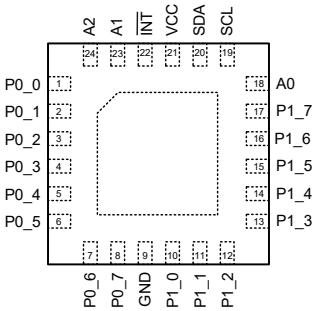



**Table 1. Pin Functions: TPT29535A**

| Pin | | Name | I/O | Description |
|---|---|---|---|---|
| TSSOP24 | QFN4X4-24 | | | |
| 21 | 18 | A0 | Input | Address input 0. Connect directly to $V_{CC}$ or ground |
| 2 | 23 | A1 | Input | Address input 1. Connect directly to $V_{CC}$ or ground |
| 3 | 24 | A2 | Input | Address input 2. Connect directly to $V_{CC}$ or ground |
| 12 | 9 | GND | GND | Ground |
| 1 | 22 | $\overline{INT}$ | Output | Interrupt output. Connect to $V_{CC}$ through a pull-up resistor |
| 4 | 1 | P0_0 | I/O | P-port I/O. Push-pull design structure. At power on, P0_0 is configured as an input |
| 5 | 2 | P0_1 | I/O | P-port I/O. Push-pull design structure. At power on, P0_1 is configured as an input |
| 6 | 3 | P0_2 | I/O | P-port I/O. Push-pull design structure. At power on, P0_2 is configured as an input |
| 7 | 4 | P0_3 | I/O | P-port I/O. Push-pull design structure. At power on, P0_3 is configured as an input |
| 8 | 5 | P0_4 | I/O | P-port I/O. Push-pull design structure. At power on, P0_4 is configured as an input |
| 9 | 6 | P0_5 | I/O | P-port I/O. Push-pull design structure. At power on, P0_5 is configured as an input |
| 10 | 7 | P0_6 | I/O | P-port I/O. Push-pull design structure. At power on, P0_6 is configured as an input |

| Pin | | Name | I/O | Description |
|---|---|---|---|---|
| TSSOP24 | QFN4X4-24 | | | |
| 11 | 8 | P0_7 | I/O | P-port I/O. Push-pull design structure. At power on, P0_7 is configured as an input |
| 13 | 10 | P1_0 | I/O | P-port I/O. Push-pull design structure. At power on, P1_0 is configured as an input |
| 14 | 11 | P1_1 | I/O | P-port I/O. Push-pull design structure. At power on, P1_1 is configured as an input |
| 15 | 12 | P1_2 | I/O | P-port I/O. Push-pull design structure. At power on, P1_2 is configured as an input |
| 16 | 13 | P1_3 | I/O | P-port I/O. Push-pull design structure. At power on, P1_3 is configured as an input |
| 17 | 14 | P1_4 | I/O | P-port I/O. Push-pull design structure. At power on, P1_4 is configured as an input |
| 18 | 15 | P1_5 | I/O | P-port I/O. Push-pull design structure. At power on, P1_5 is configured as an input |
| 19 | 16 | P1_6 | I/O | P-port I/O. Push-pull design structure. At power on, P1_6 is configured as an input |
| 20 | 17 | P1_7 | I/O | P-port I/O. Push-pull design structure. At power on, P1_7 is configured as an input |
| 22 | 19 | SCL | Input | Serial clock bus. Connect to $V_{CC}$ through a pull-up resistor |
| 23 | 20 | SDA | Input | Serial data bus. Connect to $V_{CC}$ through a pull-up resistor |
| 24 | 21 | VCC | Supply | Supply voltage |
| | | E-pad | - | Thermal pad. Should connect to GND on board |

# Specifications

## Absolute Maximum Ratings (1)

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.5 | 6.0 | V |
| $V_I$ | Input Voltage | −0.5 | 6.0 | V |
| $I_{IK}$ | Input Clamp Current, $V_I$ < 0 | −20 | | mA |
| $I_{OK}$ | Output Clamp Current, $V_O$ < 0 | −20 | | mA |
| $I_{IOK}$ | Input-Output Clamp Current, $V_O$ < 0 or $V_O$ > $V_{CC}$ | −20 | 20 | mA |
| $I_{OL}$ | Continuous Output Low Current, $V_O$ = 0 to $V_{CC}$ | | 50 | mA |
| $I_{OH}$ | Continuous Output High Current, $V_O$ = 0 to $V_{CC}$ | −50 | | mA |
| $I_{CC}$ | Continuous Current through GND | −250 | | mA |
| | Continuous Current through $V_{CC}$ | | 160 | mA |
| $T_J$ | Maximum Junction Temperature | | 150 | °C |
| $T_{STG}$ | Storage Temperature | −65 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

## ESD, Electrostatic Discharge Protection

| Parameter | | Condition | Minimum Level | Unit |
|---|---|---|---|---|
| HBM | Human Body Model ESD | ANSI/ESDA/JEDEC JS-001 (1) | ±2 | kV |
| CDM | Charged Device Model ESD | ANSI/ESDA/JEDEC JS-002 (2) | ±1.5 | kV |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

| Parameter | | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 1.65 | 5.5 | V |
| $V_{IH}$ | High-Level Input Voltage | SCL, SDA | 0.7 × $V_{CC}$ | 5.5 | V |
| | | A2 ~ A0, P0_7 ~ P0_0, P1_7 ~ P1_0 | 0.7 × $V_{CC}$ | 5.5 | V |
| $V_{IL}$ | Low-Level Input Voltage | SCL, SDA | −0.5 | 0.3 × $V_{CC}$ | V |
| | | A2 ~ A0, P0_7 ~ P0_0, P1_7 ~ P1_0 | −0.5 | 0.3 × $V_{CC}$ | V |
| $I_{OH}$ | High-Level Output Current | P0_7 ~ P0_0, P1_7 ~ P1_0 | −10 | | mA |
| $I_{OL}$ | Low-Level Output Current | P0_7 ~ P0_0, P1_7 ~ P1_0 | | 25 | mA |
| | | $\overline{INT}$, SDA | | 6 | mA |
| $T_A$ | Operating Temperature Range | $V_{CC}$ = 1.65 V ~ 3.6 V | −40 | 125 | ℃ |
| | | $V_{CC}$ = 4.5 V ~ 5.5 V | −40 | 105 | ℃ |

## Thermal Information

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| TSSOP24 | 68 | 21 | °C/W |
| QFN4X4-24 | 60 | 25 | °C/W |

## Electrical Characteristics

All test conditions: $V_{CC}$ = 1.65 V to 3.6 V, $T_A$ = −40℃ to +125℃; $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = −40℃ to +105℃ unless otherwise noted.

| Parameter | | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input Diode Clamp Voltage | $I_I$ = −18 mA; $V_{CC}$ = 1.65 V to 5.5 V | | −1.2 | | | V |
| $V_{POR}$ | Power-on Reset Voltage, $V_{CC}$ Rising | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 mA | | | 1.25 | 1.5 | V |
| | Power-on Reset Voltage, $V_{CC}$ Falling | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 mA | | 0.7 | 1.2 | | V |
| $I_{OL}$ | Low-level Output Current, SDA | $V_{OL}$ = 0.4 V; $V_{CC}$ = 1.65 V to 5.5 V | | 3 | | | mA |
| | Low-level Output Current, $\overline{INT}$ | $V_{OL}$ = 0.4 V; $V_{CC}$ = 1.65 V to 5.5 V | | 3 | | | mA |
| $V_{OL}$ | Low-level Output Voltage, P port | $I_{OL}$ = 8 mA; $V_{CC}$ = 1.65 V | | | | 0.45 | V |
| | | $I_{OL}$ = 8 mA; $V_{CC}$ = 2.3 V | | | | 0.25 | V |
| | | $I_{OL}$ = 8 mA; $V_{CC}$ = 3.0 V | | | | 0.25 | V |
| | | $I_{OL}$ = 8 mA; $V_{CC}$ = 4.5 V | | | | 0.2 | V |
| | Low-level Output Voltage, P port | $I_{OL}$ = 10 mA; $V_{CC}$ = 1.65 V | | | | 0.6 | V |
| | | $I_{OL}$ = 10 mA; $V_{CC}$ = 2.3 V | | | | 0.3 | V |
| | | $I_{OL}$ = 10 mA; $V_{CC}$ = 3.0 V | | | | 0.25 | V |
| | | $I_{OL}$ = 10 mA; $V_{CC}$ = 4.5 V | | | | 0.2 | V |
| $V_{OH}$ | High-level Output Voltage, P port | $I_{OH}$ = −8 mA; $V_{CC}$ = 1.65 V | | 1.2 | | | V |
| | | $I_{OH}$ = −8 mA; $V_{CC}$ = 2.3 V | | 1.8 | | | V |
| | | $I_{OH}$ = −8 mA; $V_{CC}$ = 3.0 V | | 2.6 | | | V |
| | | $I_{OH}$ = −8 mA; $V_{CC}$ = 4.75 V | | 4.1 | | | V |
| | High-level Output Voltage, P port | $I_{OH}$ = −10 mA; $V_{CC}$ = 1.65 V | | 1.0 | | | V |
| | | $I_{OH}$ = −10 mA; $V_{CC}$ = 2.3 V | | 1.7 | | | V |
| | | $I_{OH}$ = −10 mA; $V_{CC}$ = 3.0 V | | 2.5 | | | V |
| | | $I_{OH}$ = −10 mA; $V_{CC}$ = 4.75 V | | 4.0 | | | V |
| $I_I$ | Input Current: A0, A1, A2 | $V_I$ = $V_{CC}$ or GND, $V_{CC}$ = 1.65 V to 5.5 V | | −1 | | 1 | μA |
| | Input Current: SCL, SDA | $V_I$ = $V_{CC}$ or GND, $V_{CC}$ = 1.65 V to 5.5 V | | −1 | | 1 | μA |
| $I_{IH}$ | High-level Input Current: P port | $V_I$ = $V_{CC}$; $V_{CC}$ = 1.65 V to 5.5 V | | | | 1 | μA |
| $I_{IL}$ | Low-level Input Current: P Port | $V_I$ = GND; $V_{CC}$ = 1.65 V to 5.5 V | | −1 | | | μA |
| $I_{CC}$ | Supply Current | Active mode, $I_O$ = 0 mA; I/O = inputs; $f_{SCL}$ = 400 kHz | $V_{CC}$ = 5.5 V | | 22.7 | 40 | μA |
| | | | $V_{CC}$ = 3.6 V | | 12.1 | 30 | μA |
| | | | $V_{CC}$ = 2.7 V | | 8.2 | 19 | μA |
| | | | $V_{CC}$ = 1.95 V | | 5.6 | 11 | μA |

| Parameter | | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | Standby Mode, input low, $I_O$ = 0 mA; I/O = inputs; $f_{SCL}$ = 0 kHz | $V_{CC}$ = 5.5 V | | 0.73 | 8.7 | μA |
| | | | $V_{CC}$ = 3.6 V | | 0.43 | 4 | μA |
| | | | $V_{CC}$ = 2.7 V | | 0.29 | 3 | μA |
| | | | $V_{CC}$ = 1.95 V | | 0.18 | 2.2 | μA |
| | | Standby Mode, input high, $I_O$ = 0 mA; I/O = inputs; $f_{SCL}$ = 0 kHz | $V_{CC}$ = 5.5 V | | 0.73 | 3.9 | μA |
| | | | $V_{CC}$ = 3.6 V | | 0.42 | 2.2 | μA |
| | | | $V_{CC}$ = 2.7 V | | 0.29 | 1.8 | μA |
| | | | $V_{CC}$ = 1.95 V | | 0.18 | 1.5 | μA |
| $C_i$ | Input Capacitance: SCL | $V_I$ = $V_{CC}$ or GND; $V_{CC}$ = 1.65 V to 5.5 V (1) | | | 3 | | pF |
| $C_{io}$ | Input/Output Capacitance: SDA | $V_{I/O}$ = $V_{CC}$ or GND; $V_{CC}$ = 1.65 V to 5.5 V (1) | | | 3 | | pF |
| | Input/Output Capacitance: P ports | $V_{I/O}$ = $V_{CC}$ or GND; $V_{CC}$ = 1.65 V to 5.5 V (1) | | | 5 | | pF |

(1) Parameters are provided by lab bench tests and design simulation.

## I²C Interface Timing Requirements

Over recommended operating free-air temperature range, unless otherwise noted. (1)

| Description | | Conditions | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{scl}$ | I²C Clock Frequency | | 0 | 100 | 0 | 400 | kHz |
| $t_{sch}$ | I²C Clock High Time | | 4 | | 0.6 | | μs |
| $t_{scl}$ | I²C Clock Low Time | | 4.7 | | 1.3 | | μs |
| $t_{sp}$ | I²C Spike Time | | | 50 | | 50 | ns |
| $t_{sds}$ | I²C Serial-data Setup Time | | 250 | | 100 | | ns |
| $t_{sdh}$ | I²C Serial-data Hold Time | | 0 | | 0 | | ns |
| $t_{icr}$ | I²C Input Rise Time | | | 1000 | 20 | 300 | ns |
| $t_{icf}$ | I²C Input Fall Time | | | 300 | 20 × ($V_{CC}$ / 5.5 V) | 300 | ns |
| $t_{ocf}$ | I²C Output Fall Time | 10-pF to 400-pF bus | | 300 | 20 × ($V_{CC}$ / 5.5 V) | 300 | ns |
| $t_{buf}$ | I²C Bus Free Time Between Stop and Start | | 4.7 | | 1.3 | | μs |
| $t_{sts}$ | I²C Start or Repeated Start Condition Setup | | 4.7 | | 0.6 | | μs |
| $t_{sth}$ | I²C Start or Repeated Start Condition Hold | | 4 | | 0.6 | | μs |
| $t_{sps}$ | I²C Stop Condition Setup | | 4 | | 0.6 | | μs |
| $t_{vd(data)}$ | Valid Data Time | SCL low to SDA output valid | | 3.5 | | 0.9 | μs |
| $t_{vd(ack)}$ | Valid Data Time of ACK Condition | ACK signal from SCL low to SDA (out) low | | 3.5 | | 0.9 | μs |
| $C_b$ | I²C Bus Capacitive Load (2) | | | 400 | | 400 | pF |

(1) All timing requirements should refer to the I²C standard, and parameters in the table are tested by the lab bench.
(2) $C_b$ is the total capacitance of one bus line in pF.

## Switching Characteristics

Over the recommended operating free-air temperature range, $C_L \leq 100$ pF, unless otherwise noted.

| Description | | From (Input) | To (Output) | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{iv}$ | Interrupt Valid Time | P port | $\overline{INT}$ | | 4 | | 4 | μs |
| $t_{ir}$ | Interrupt Reset Delay Time | SCL | $\overline{INT}$ | | 4 | | 4 | μs |
| $t_{pv}$ | Output Data Valid; $V_{CC}$ = 2.3 V to 5.5 V | SCL | P port | | 400 | | 400 | ns |
| | Output Data Valid; $V_{CC}$ = 1.65 V to 2.3 V | | | | 400 | | 400 | ns |
| $t_{ps}$ | Input Data Setup Time | P port | SCL | 150 | | 150 | | ns |
| $t_{ph}$ | Input Data Hold Time | P port | SCL | 1 | | 1 | | μs |

## Typical Performance Characteristics

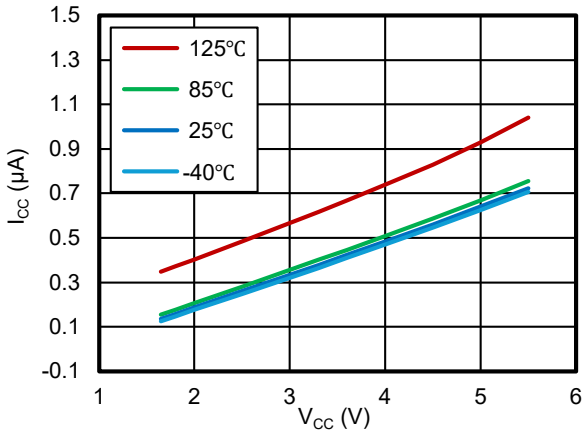



Figure 1. Standby Supply Current vs. Supply Voltage

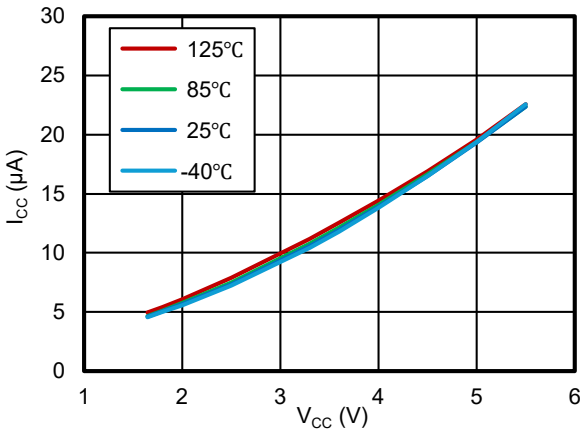



Figure 2. Active Supply Current vs. Supply Voltage

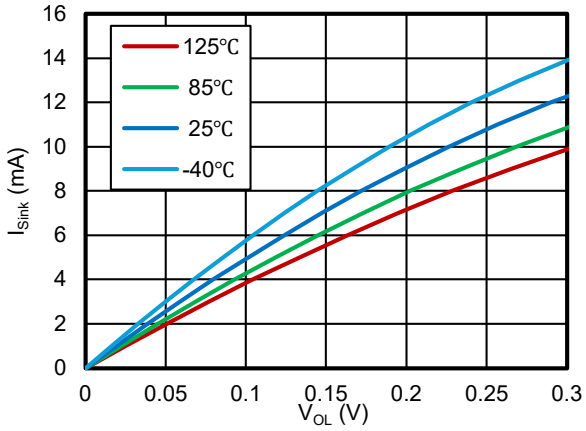



Figure 3. I/O Sink Current vs. $V_{OL}$ ($V_{CCP}$ = 1.65 V)

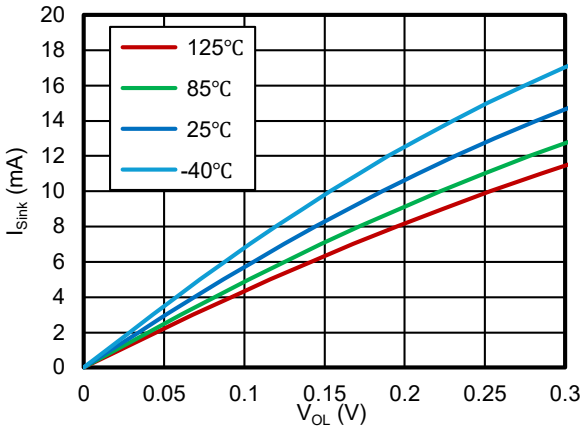



Figure 4. I/O Sink Current vs. $V_{OL}$ ($V_{CCP}$ = 1.8 V)

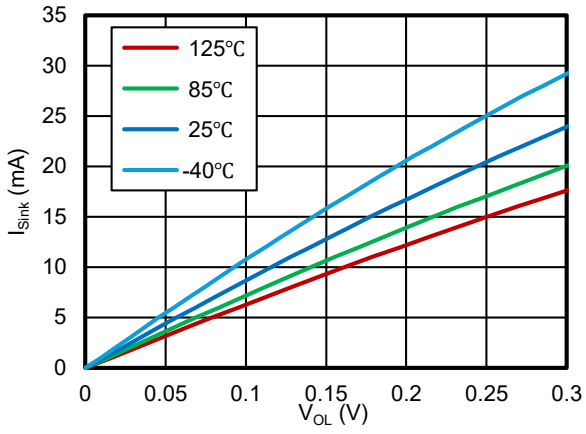



Figure 5. I/O Sink Current vs. $V_{OL}$ ($V_{CCP}$ = 2.5 V)

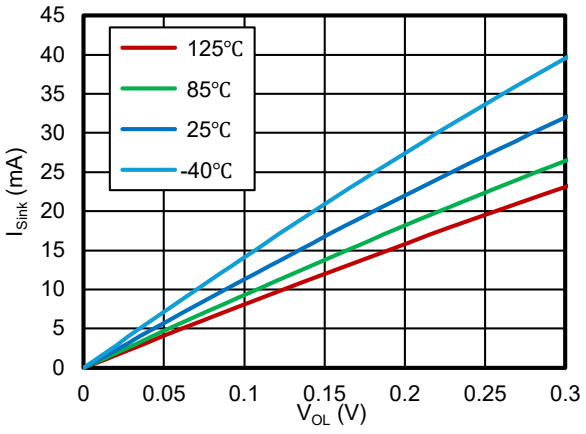



Figure 6. I/O Sink Current vs. $V_{OL}$ ($V_{CCP}$ = 3.3 V)

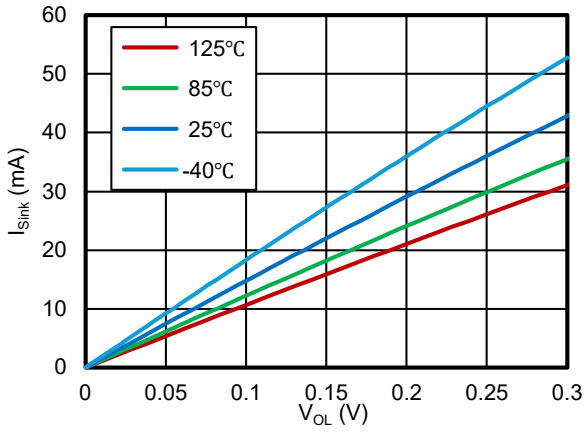



Figure 7. I/O Sink Current vs. $V_{OL}$ ($V_{CCP}$ = 5 V)

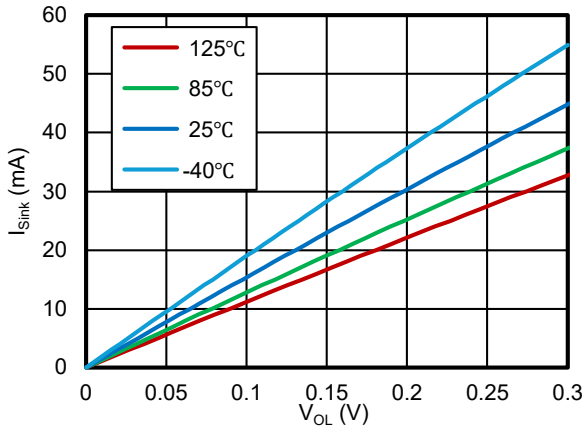



Figure 8. I/O Sink Current vs. $V_{OL}$ ($V_{CCP}$ = 5.5 V)

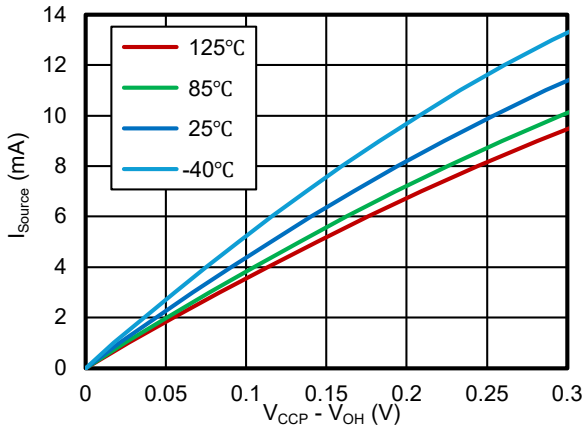



Figure 9. I/O Source Current vs. $V_{OH}$ ($V_{CCP}$ = 1.65 V)

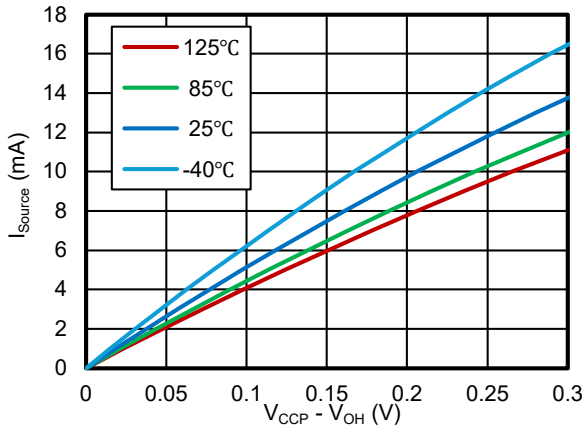



Figure 10. I/O Source Current vs. $V_{OH}$ ($V_{CCP}$ = 1.8 V)

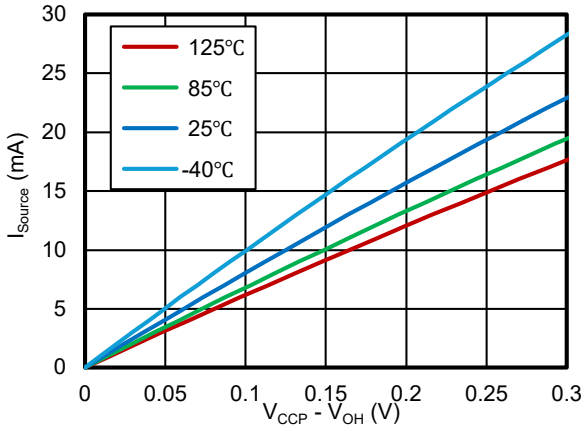



Figure 11. I/O Source Current vs. $V_{OH}$ ($V_{CCP}$ = 2.5 V)

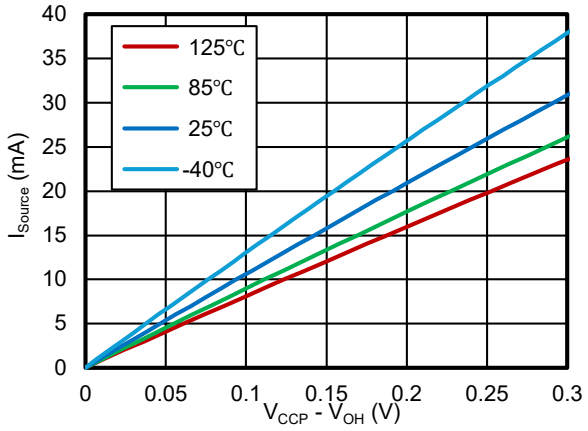



Figure 12. I/O Source Current vs. $V_{OH}$ ($V_{CCP}$ = 3.3 V)

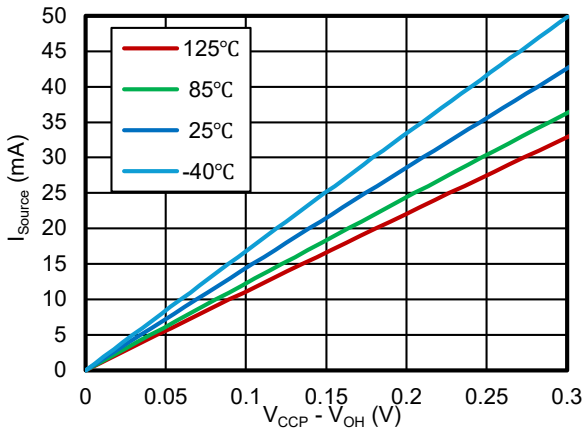



Figure 13. I/O Source Current vs. $V_{OH}$ ($V_{CCP}$ = 5 V)

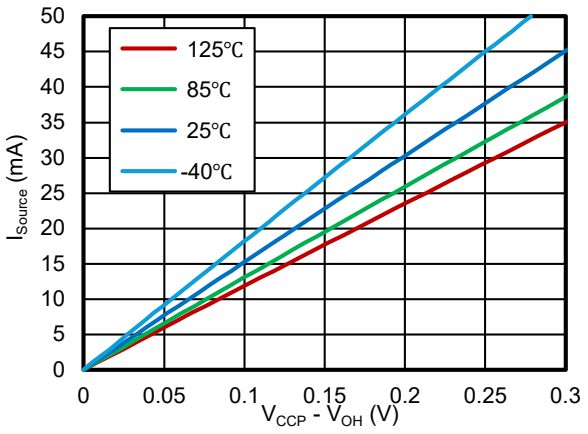



Figure 14. I/O Source Current vs. $V_{OH}$ ($V_{CCP}$ = 5.5 V)

## Parameter Measurement Waveforms

### I²C Interface Load Circuit and Waveforms

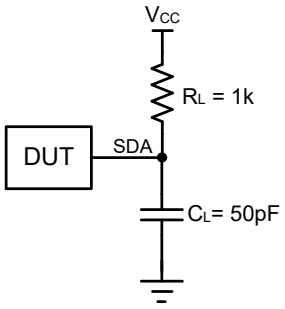



**Figure 15. SDA Load Configuration**

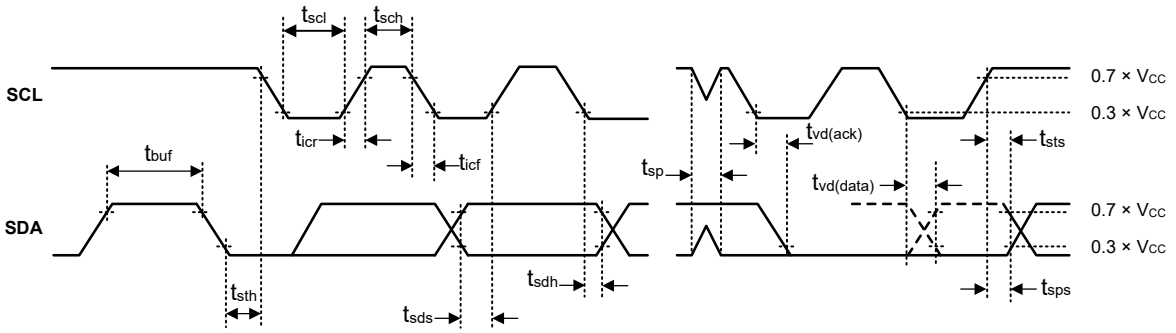



**Figure 16. Definition of Timing on the I²C-Bus**

### Interrupt Load Circuit and Waveforms

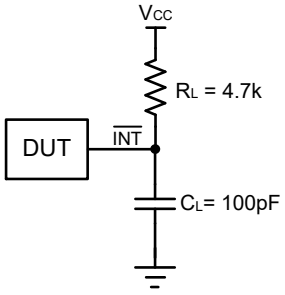



**Figure 17. Interrupt Load Configuration**

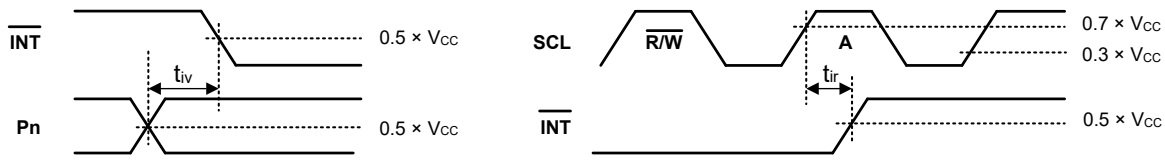



**Figure 18. Definition of Interrupt Timing**

**P-Port Load Circuit and Waveforms**

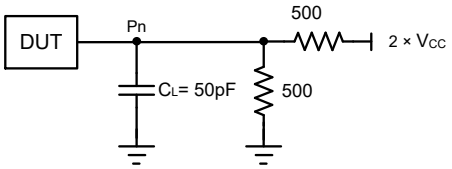



**Figure 19. P-Port Load Configuration**

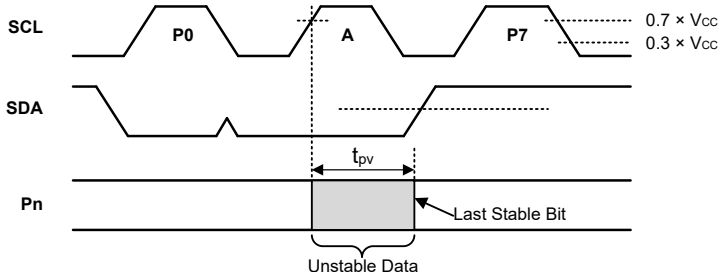



**Figure 20. Definition of Write Mode Timing**

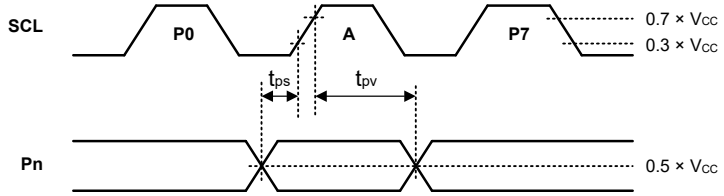



**Figure 21. Definition of Read Mode Timing**

# Detailed Description

## Overview

The TPT29535A is a 16-bit GPIO expander with interrupt for I²C-bus applications. The power supply voltage ranges from 1.65 V to 5.5 V, allowing the TPT29535A to interconnect with 1.8-V microcontrollers.

The TPT29535A contains two pairs of 8-bit registers: Configuration (input or output mode selection), Input Port, Output Port, and Polarity Inversion registers. At power-on, the I/Os are configured as inputs by default. The system controller can configure the I/Os as either inputs or outputs by writing to the I/O configuration register bits. Data for each input or output is held in the corresponding Input or Output register. The polarity of the Input Port register can be inverted via the Polarity Inversion register. All registers are readable by the system controller.

The open-drain interrupt ($\overline{INT}$) output is asserted when any input state changes from its related register state. The device is used to indicate to the system controller that an input state has changed. The $\overline{INT}$ can be connected to the interrupt input of a microcontroller. By asserting an interrupt signal on this line, the remote I/O can notify the microcontroller of incoming data on its ports without the need for I²C-Bus communication. Thus, the TPT29535A can remain a simple slave device. The power-on reset sets the registers to their default values and initializes the device state machine.

All input/output pins do not have internal pull-up resistors; thus the device can reduce power consumption when communicating with external I/Os. Three hardware pins (A0, A1, A2) select the configured I²C-Bus address and allow up to eight devices to share the same I²C-Bus.

## Functional Block Diagram

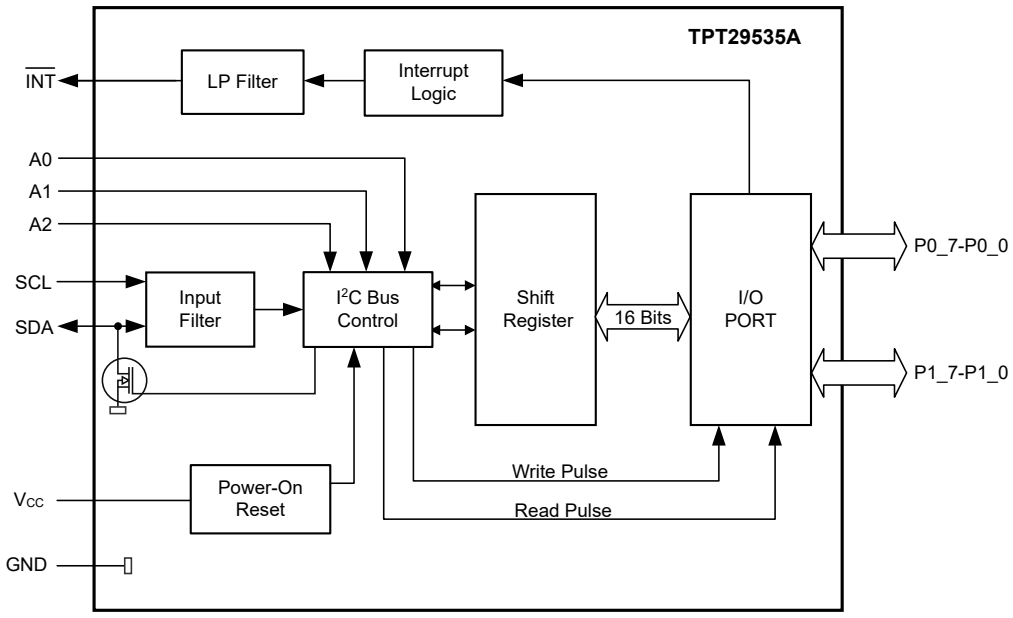



**Figure 22. Functional Block Diagram**

## Feature Description

#### 5-V Tolerant I/O Ports

The TPT29535A supports the I/O voltage from 1.8 V to 5 V, which allows the TPT29535A to connect to various devices with I/O communication. To minimize the current consumption, it is recommended that the input signal meet the $V_{IH}$ and $V_{IL}$ spec

in the Electrical Characteristics table. Unused ports must not be left floating, and should be connected to $V_{CC}$ or GND via a resistor.

**Power-on Reset**

When power (from 0 V) is applied to the $V_{CC}$ pin of the TPT29535A, an internal Power-On Reset (POR) remains in reset condition until $V_{CC}$ reaches $V_{POR}$. At that point, the reset condition is released, and the TPT29535A registers and state machine are set to their default states. After that, $V_{CC}$ must be lowered to $V_{PORF}$ to reset the device, and then brought back up to the operating voltage to complete a power-on reset cycle.

**Interrupt ($\overline{INT}$) Output**

In the input mode, an interrupt is generated by any rising or falling edge of the port inputs. After time $t_{iv}$, the output signal $\overline{INT}$ is valid. When data on the port is changed to the original setting, or data is read from the port that generated the interrupt, it resets the interrupt circuit. The reset operation will be performed in read mode, at the acknowledge (ACK) bit after the SCL rising edge. Note that the $\overline{INT}$ is reset at the ACK just before the byte of changed data is sent. Interrupts that occur during the ACK clock pulse can be lost because the interrupt is reset during this pulse. Each change of the I/O after resetting is detected and generates the $\overline{INT}$ output.

The pin configured as an output cannot trigger an interrupt. Changing an I/O from output to input may cause a false interrupt if the pin state does not match the setting of the Input Port register.

The $\overline{INT}$ output has an open-drain structure and requires a pull-up resistor to $V_{CC}$. The $\overline{INT}$ should be connected to the voltage source of the device that requires the interrupt information.

## Device Address

Following a START condition, the bus master must output the address of the slave it is accessing. Three hardware pins (A0, A1, A2) select the configured I²C-Bus address and allow up to eight devices to share the same I²C-Bus. To conserve power, address pins (A0, A1, A2) must be pulled HIGH or LOW. The address of the TPT29535A is shown below.

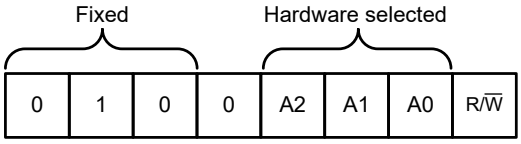



**Figure 23. Slave Device Address**

## Registers Map

**Command Byte**

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

**Table 2. Command Byte Description**

| Command | Register |
|---|---|
| 0 | Input port 0 |
| 1 | Input port 1 |

| | |
|---|---|
| 2 | Output port 0 |
| 3 | Output port 1 |
| 4 | Polarity Inversion port 0 |
| 5 | Polarity Inversion port 1 |
| 6 | Configuration port 0 |
| 7 | Configuration port 1 |

**Register 0 and 1: Input port registers**

This register is an input-only port, which means the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output, and writes to this register have no effect.

The default value 'X' is determined by the external logic level.

**Table 3. Input Port 0 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | I0.7 | I0.6 | I0.5 | I0.4 | I0.3 | I0.2 | I0.1 | I0.0 |
| Default | X | X | X | X | X | X | X | X |

**Table 4. Input Port 1 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | I1.7 | I1.6 | I1.5 | I1.4 | I1.3 | I1.2 | I1.1 | I1.0 |
| Default | X | X | X | X | X | X | X | X |

**Register 2 and 3: Output port registers**

This register is an output-only port, which means the outcoming logic levels of the pins are defined as outputs by Register 6 (Configuration port 0) and 7 (Configuration port 1). Bit values in this register have no effect on pins defined as inputs. In fact, the value reading from this register is in the flip-flop controlling the output selection, not the actual pin value.

**Table 5. Output Port 0 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | O0.7 | O0.6 | O0.5 | O0.4 | O0.3 | O0.2 | O0.1 | O0.0 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Table 6. Output Port 1 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | O1.7 | O1.6 | O1.5 | O1.4 | O1.3 | O1.2 | O1.1 | O1.0 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Register 4 and 5: Polarity Inversion registers**

This register allows the user to invert the polarity of the input port register data. If a bit in this register is set (written with '1'), the input port data polarity is inverted. If a bit in this register is cleared (written with '0'), the input port data polarity is retained.

**Table 7. Polarity Inversion Port 0 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | N0.7 | N0.6 | N0.5 | N0.4 | N0.3 | N0.2 | N0.1 | N0.0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8. Polarity Inversion Port 1 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | N1.7 | N1.6 | N1.5 | N1.4 | N1.3 | N1.2 | N1.1 | N1.0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Register 6 and 7: Configuration registers**

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with a high impedance. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. After a reset, all ports are defaulted to inputs.

**Table 9. Configuration Port 0 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | C0.7 | C0.6 | C0.5 | C0.4 | C0.3 | C0.2 | C0.1 | C0.0 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Table 10. Configuration Port 1 Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | C1.7 | C1.6 | C1.5 | C1.4 | C1.3 | C1.2 | C1.1 | C1.0 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## Bus Transactions

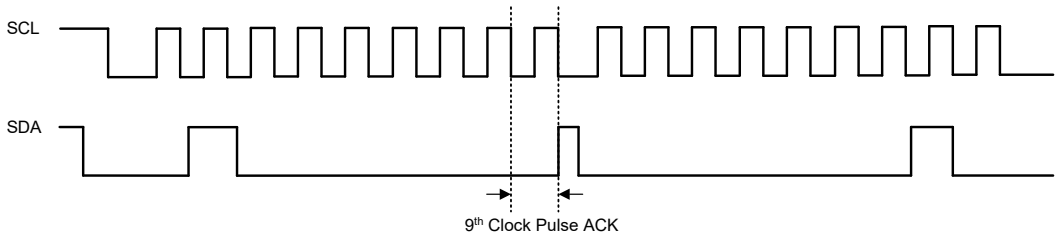



**Figure 24. I²C-Bus Waveform**

### Writing to Port Registers

The data is transmitted to the TPT29535A by sending the device address with the least significant bit set to logic '0'. The command byte is sent after the address and determines which register will receive the subsequent data.

The 8 registers of the TPT29535A can be divided into 4 register pairs, which are the input port, output port, polarity inversion port, and configuration port, respectively. After sending data to one register, the next data byte will be sent to another register in the same pair. For example, if the first byte is sent to output port 1 (register 3), then the next byte will be stored in output port 0 (register 2). There is no limitation on the number of data bytes sent in a single write transmission. Therefore, each 8-bit register can be updated independently of the others.

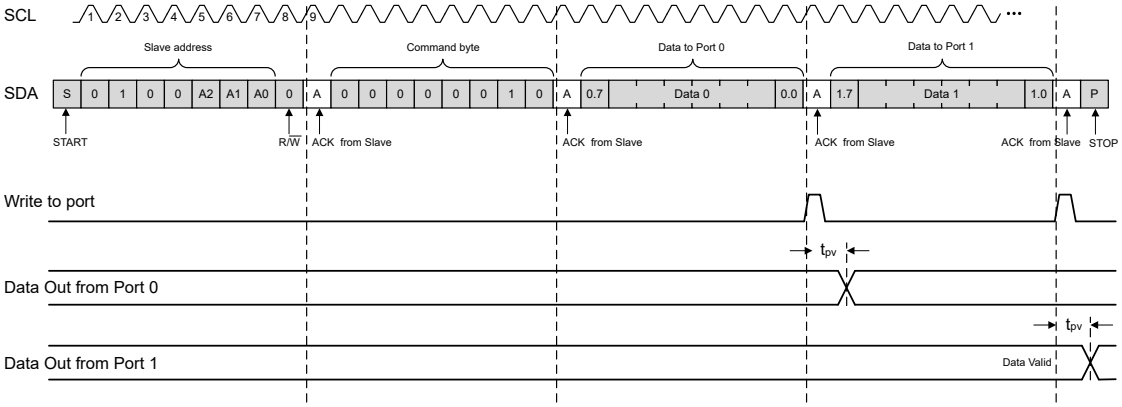



**Figure 25. Write to Output Port Registers**

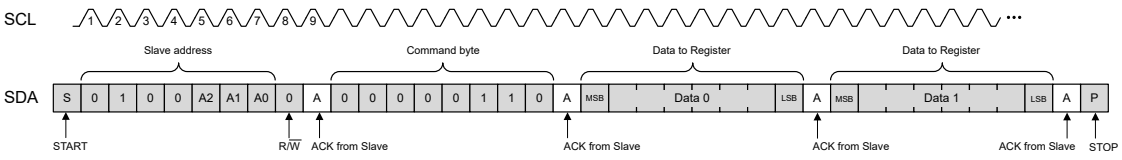



**Figure 26. Write to Configuration Registers**

### Reading Port Registers

To read data, the master device must first send the TPT29535A address with the least significant bit set to logic '0'. The command byte is sent following the address, determining which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to logic '1'. The TPT29535A will then transmit the data from the register defined by the command byte. Data is clocked into the register on the rising edge of the acknowledge clock pulse.

After reading the first byte, the master can continue to read data from the other register in the same pair by sending an ACK to the slave. For example, if the first byte is input port 1 (register 1), then the next byte read is input port 0 (register 0). There is no limit on the number of data bytes that can be received in one read transmission. For the last byte received, the master device must send a NACK, followed by sending a STOP condition.

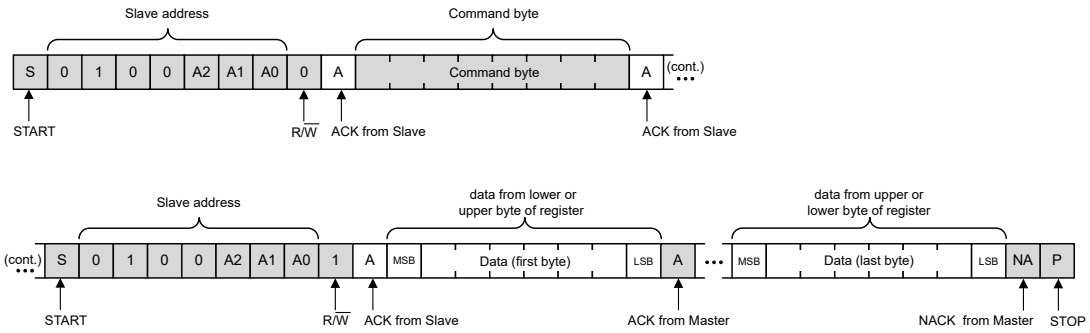



**Figure 27. Read Port Registers**

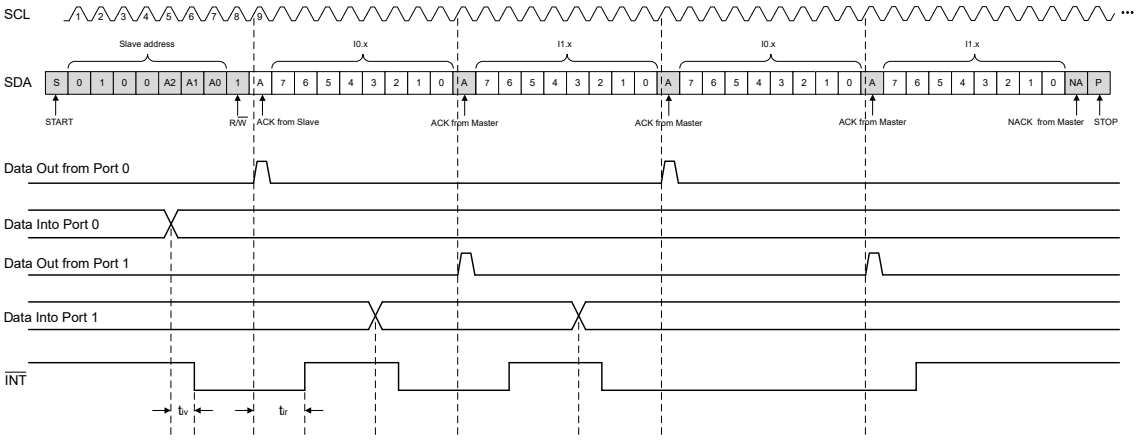



**Figure 28. Read Input Port Register, Scenario 1**

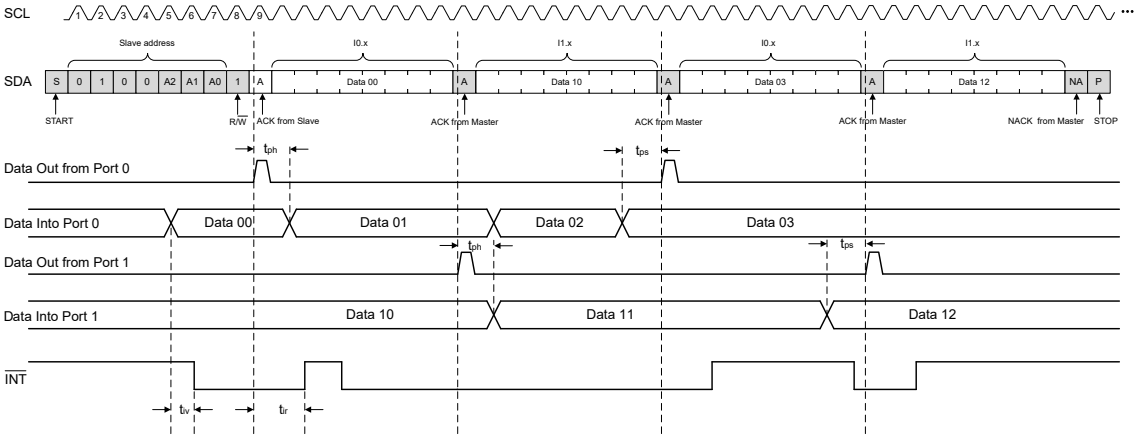



**Figure 29. Read Input Port Register, Scenario 2**

# Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## Application Information

The TPT29535A features 16-bit configurable I/O ports. The interrupt $\overline{INT}$ can be connected to the interrupt input of a microcontroller, and then the interrupt $\overline{INT}$ output will respond to any input state change.

## Typical Application

The following figure shows an application in which the TPT29535A can be used to control multiple subsystems and read inputs from buttons.

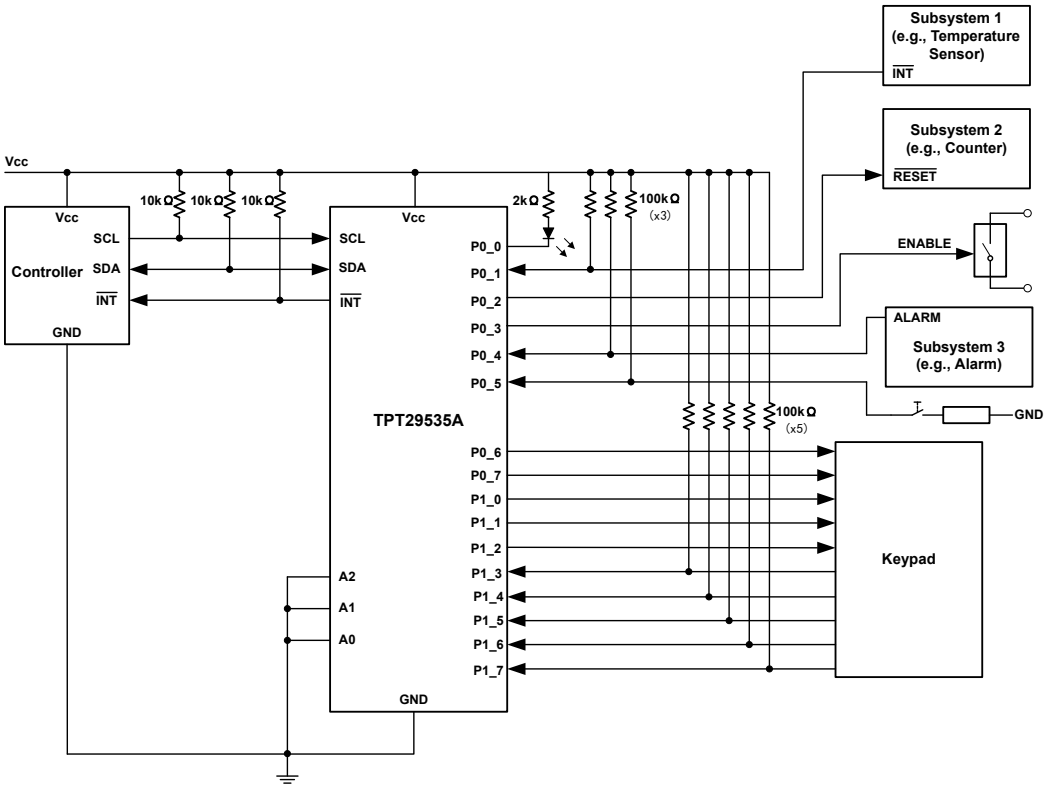



**Figure 30. Typical Application Reference Circuit**

## I²C-Bus Pull-up Resistance

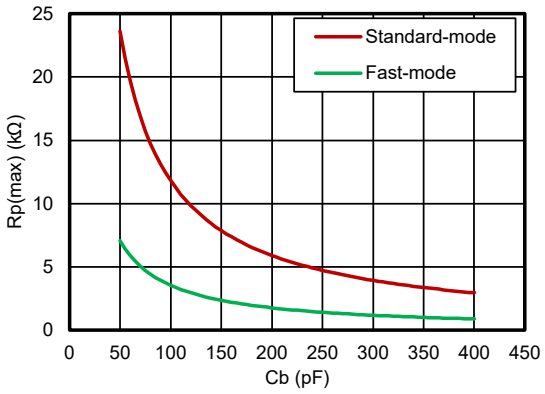
The SDA and SCL pull-up resistors are selected as follows.

The minimum pull-up resistance is a function of $V_{CC}$, $V_{OL(max)}$, and $I_{OL}$.

$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

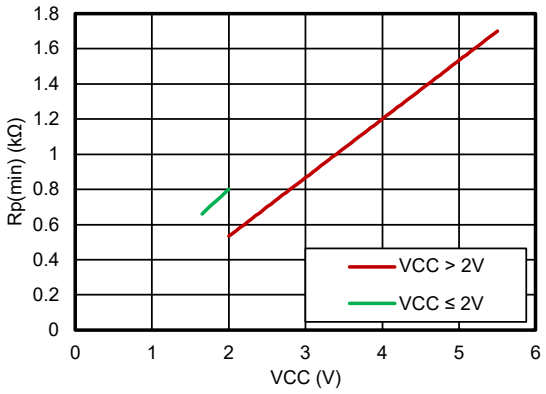
The maximum pull-up resistance is a function of $t_r$ and $C_b$. The parameter $t_r$ is the maximum rise time of the I²C-Bus, specified as 300 ns for Fast-mode and 1000 ns for Standard-mode. $C_b$ is the total capacitance on the bus.

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$




Standard-mode ($f_{scl}$ = 100 kHz, $t_r$ = 1 µs)
Fast-mode ($f_{scl}$ = 400 kHz, $t_r$ = 300 ns)

**Figure 31. Maximum Pull-up Resistance ($R_{p(max)}$) vs. Bus Capacitance ($C_b$)**




$V_{OL}$ = 0.4 V, $I_{OL}$ = 3 mA when $V_{CC}$ > 2 V
$V_{OL}$ = 0.2*$V_{CC}$, $I_{OL}$ = 2 mA when $V_{CC}$ ≤ 2 V

**Figure 32. Minimum Pull-up Resistance ($R_{p(min)}$) vs. Pull-up Reference Voltage ($V_{CC}$)**

# Layout

## Layout Guideline

For PCB layout of the TPT29535A, common board-level design practices must be followed. I²C buses generally do not require impedance matching or differential routing, as these are concerns typically associated with high-speed interfaces. Nevertheless, the fast falling edges inherent to the I²C open-drain architecture demand particular attention. These fast transitions contain significant high-frequency harmonic content and are susceptible to reflection at impedance discontinuities such as vias, connectors, and stubs, manifesting as ringing or non-monotonic edges on the signal lines. For applications with long trace lengths or notable impedance mismatches, it is recommended to place series damping resistors on the bus lines. These resistors effectively reduce the slew rate of the falling edge and absorb reflected energy from the far end.

In PCB routing, right-angle bends should be avoided. When a trace must change direction, 45° bends or curved arcs are recommended, with curved arcs being the preferred approach as they maintain constant trace width, minimizing unwanted impedance variations. Upon leaving the vicinity of the IC, signal traces should be fanned out with adequate spacing to minimize crosstalk. Additionally, wider trace widths should be used for power and ground nets to accommodate higher current levels. Bypass and decoupling capacitors are commonly employed to stabilize the voltage on the $V_{CC}$ pin. A larger capacitor provides supplementary power during brief supply droops, while a smaller capacitor filters high-frequency ripple. These capacitors must be placed as close to the device as possible.

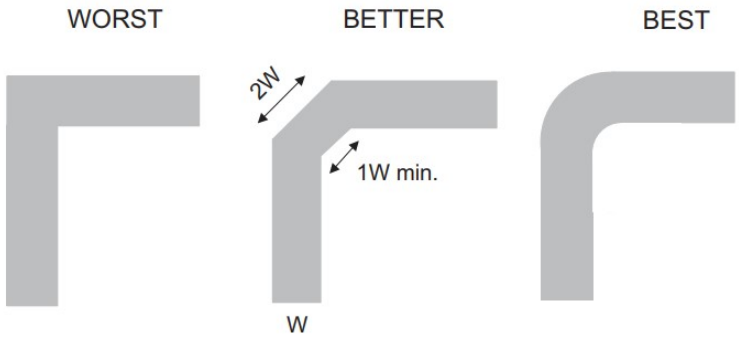



**Figure 33. Trace Example**

On a 2-layer PCB, signal routing is typically placed on the top layer with power and ground planes on the bottom layer. For boards with higher routing density, a 4-layer stack-up is recommended, where signals are generally routed on the top and bottom layers, with one internal layer dedicated to ground and the other to power. In designs employing solid or split power and ground planes, vias should be placed immediately adjacent to the surface-mount component pads that require connection to $V_{CC}$ or GND, and electrically connected to the internal plane or the opposite side of the board. Vias are also used when signal traces must transition to the opposite board layer; however, such vias should be minimized to reduce impedance discontinuities. Where vias are unavoidable, the clearance around them should be increased to minimize parasitic capacitance. Care should also be taken when designing test points, as through-hole pins are not recommended for high-frequency signal paths.

## Layout Example

Figure 34 illustrates an example of a PCB layout with the TPT29535A. Some key considerations are as follows:

- Decouple the $V_{CC}$ pin with a 0.1-μF capacitor, and place it as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the $V_{CC}$ supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.

- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

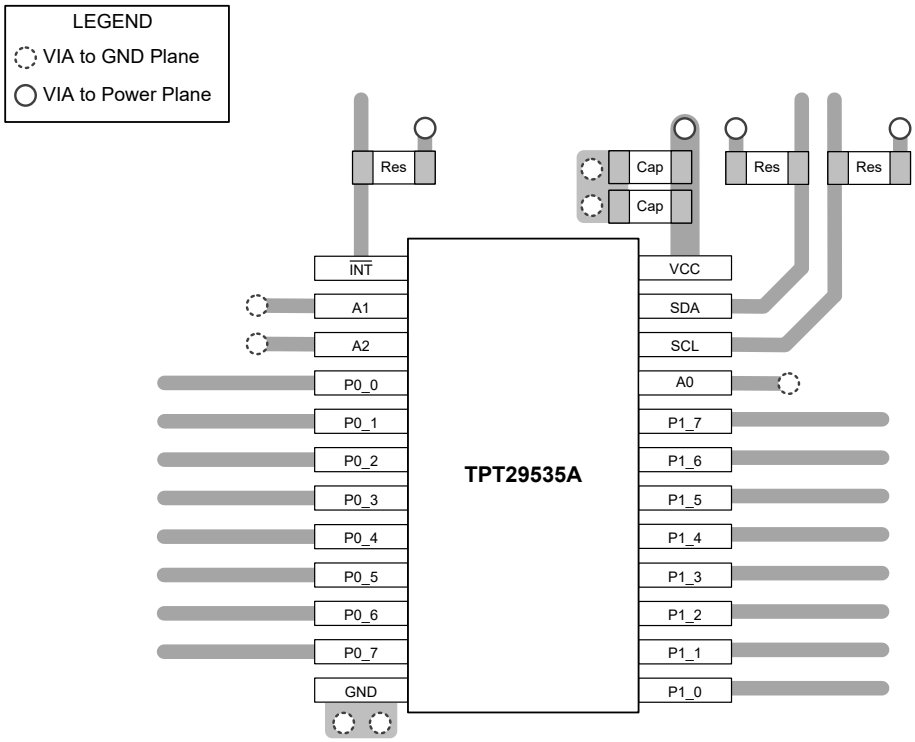
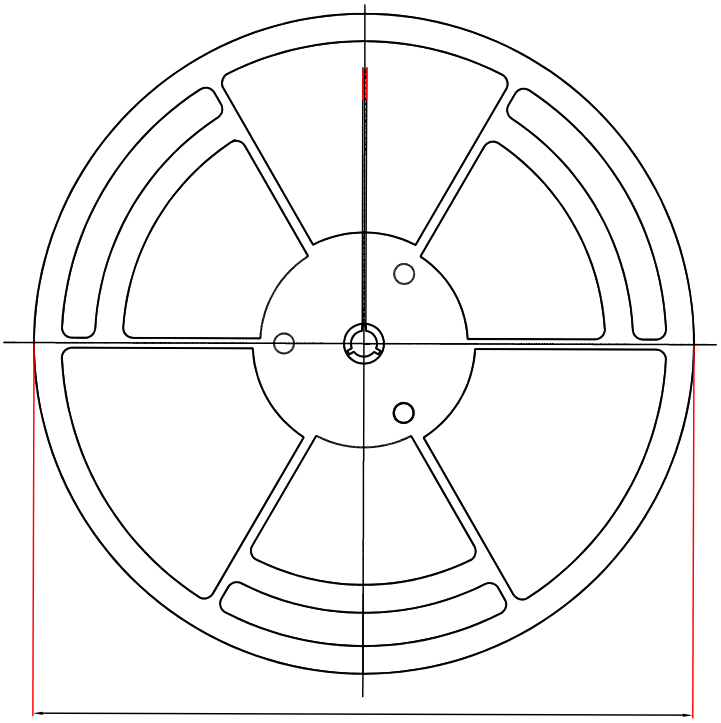
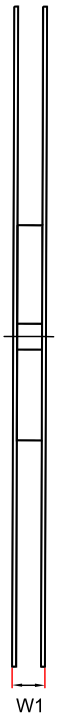
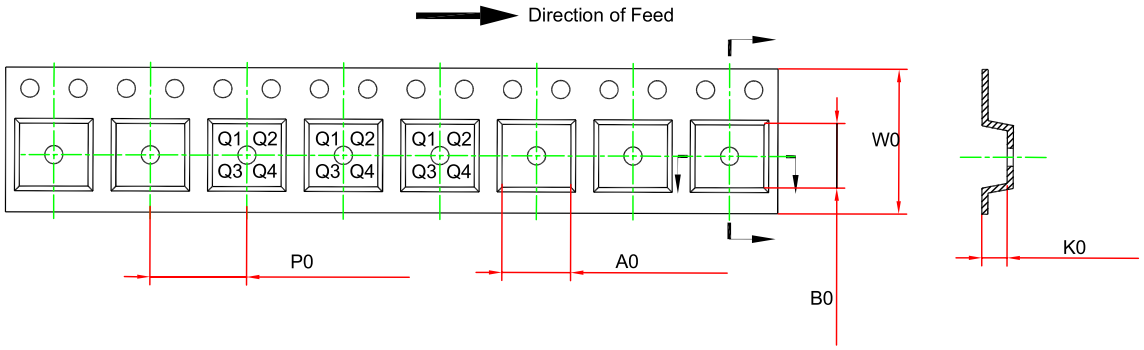



**Figure 34. TPT29535A Layout Example**

## Tape and Reel Information



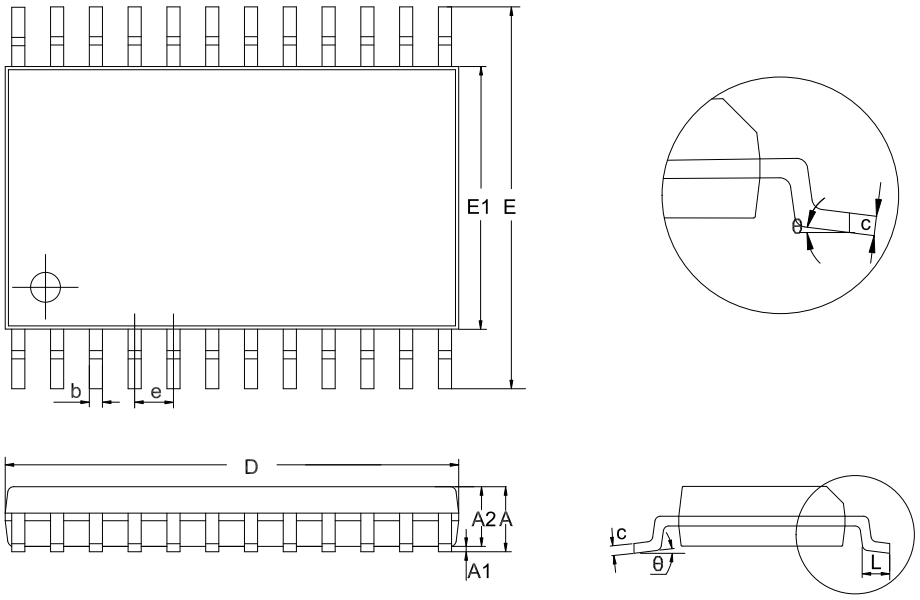




| Order Number | Package | D1 (mm) | W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | W0 (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|
| TPT29535A-TS5R | TSSOP24 | 330 | 21.6 | 6.8 | 8.3 | 1.6 | 8 | 16 | Q1 |
| TPT29535A-FE2R | QFN4X4-24 | 330 | 17.6 | 4.3 | 4.3 | 1.1 | 8 | 12 | Q2 |

## Package Outline Dimensions

### TSSOP24

Package Outline Dimensions TS5(TSSOP-24-A)



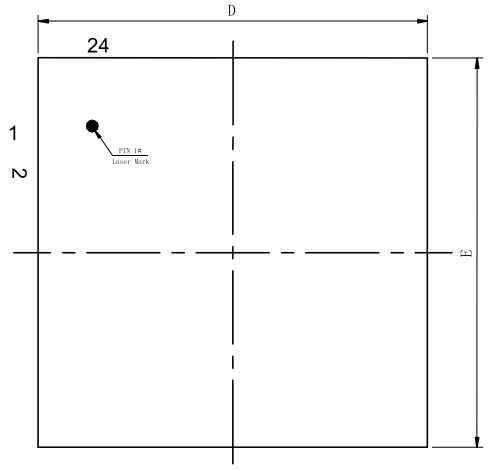

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.900 | 1.200 | 0.035 | 0.047 |
| A1 | 0.050 | 0.150 | 0.002 | 0.006 |
| A2 | 0.800 | 1.050 | 0.031 | 0.041 |
| b | 0.190 | 0.300 | 0.007 | 0.012 |
| c | 0.090 | 0.200 | 0.004 | 0.008 |
| D | 7.700 | 7.900 | 0.303 | 0.311 |
| E | 6.200 | 6.600 | 0.244 | 0.260 |
| E1 | 4.300 | 4.500 | 0.169 | 0.177 |
| e | 0.650 BSC | | 0.026 BSC | |
| L | 0.450 | 0.750 | 0.018 | 0.030 |
| θ | 0 | 8° | 0 | 8° |

NOTES

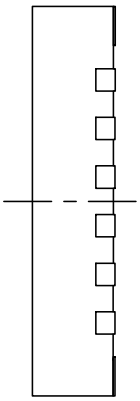
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

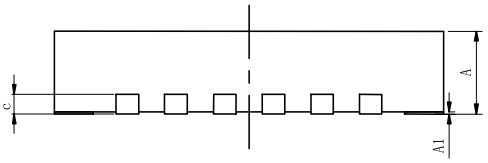
## QFN4X4-24

### Package Outline Dimensions QF8(QFN4X4-24-B)

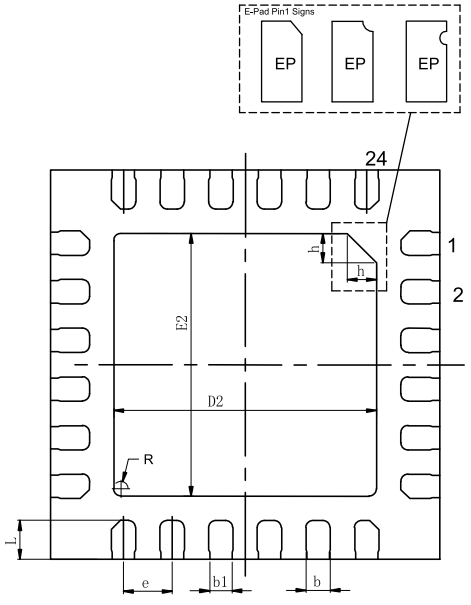



TOP VIEW






SIDE VIEW




BOTTOM VIEW

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.800 | 0.900 | 0.031 | 0.035 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| b1 | 0.160 REF | | 0.006 REF | |
| c | 0.180 | 0.250 | 0.007 | 0.010 |
| D | 3.900 | 4.100 | 0.154 | 0.161 |
| E | 3.900 | 4.100 | 0.154 | 0.161 |
| e | 0.500 BSC | | 0.020 BSC | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |
| D2 | 2.150 | 2.350 | 0.085 | 0.093 |
| E2 | 2.150 | 2.350 | 0.085 | 0.093 |
| h | 0.300 | 0.400 | 0.008 | 0.016 |

## Order Information

| Order Number | Operating Temperature Range | Package | Marking Information | MSL | Transport Media, Quantity | Eco Plan |
|---|---|---|---|---|---|---|
| TPT29535A-TS5R | −40℃ to +125℃ | TSSOP24 | 9535A | MSL3 | Tape and Reel, 4000 | Green |
| TPT29535A-FE2R | −40℃ to +125℃ | QFN4×4-24 | 29535 | MSL3 | Tape and Reel, 3000 | Green |

**Green**: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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