Features

- Bidirectional Translator of I²C Applications and SMBus Compatible
- Support Fast-mode Plus, up to 1Mbps data rate
- High-impedance SCL1, SDA1, SCL2 and SDA2 pins for EN = LOW
- 1 V pre-charge on All SDA and SCL Lines prevents corruption during live board insertion
- Operating Power Supply Range of 2.35 V to 5.5 V
- Low I_{CC} Chip Disable of < 1 µA
- Powered-Off High-Impedance I²C Pins
- Built-in ΔV/Δt rise time accelerator
- ACK error protection to avoid direction switching error
- ESD Protection:
  - 7 kV Human-Body Model
  - 1.5 kV Charged-Device Model

Applications

- Servers/Storages
- Enterprise Switching
- Telecom switching equipment and Base stations
- Industrial automation equipment

Description

The TPT29511B device is a dual bidirectional I²C and SMBus Hot-swap buffer with an enable (EN) input, and work from 2.3 V to 5.5 V V_{CC}, which supports IO cards live insertion and removal from backplane. Control circuit prevents the backplane-side I²C lines (in) from the other card-side I²C lines (out) until a stop command or bus idle condition occurs on the backplane without bus contention on the card. When the connection is made, the TPT29511B provides bidirectional buffering, keeping the backplane and card capacitances isolated.

The TPT29511B rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements (ΔV/Δt > 1.25 V/us). when the pulse width of the rise edge acceleration is greater than 300 ns, the ACK error protection is triggered to prevent the direction switching error.

The TPT29511B incorporates a digital ENABLE input pin, which enables the device when asserted HIGH and forces the device into a low current mode when asserted LOW, and an open-drain READY output pin, which indicates that the backplane and card sides are connected together (HIGH) or not (LOW).

TPT29511B is available in MSOP8 and SOP8 package, and is characterized from −40°C to +125°C.

Functional Block Diagram

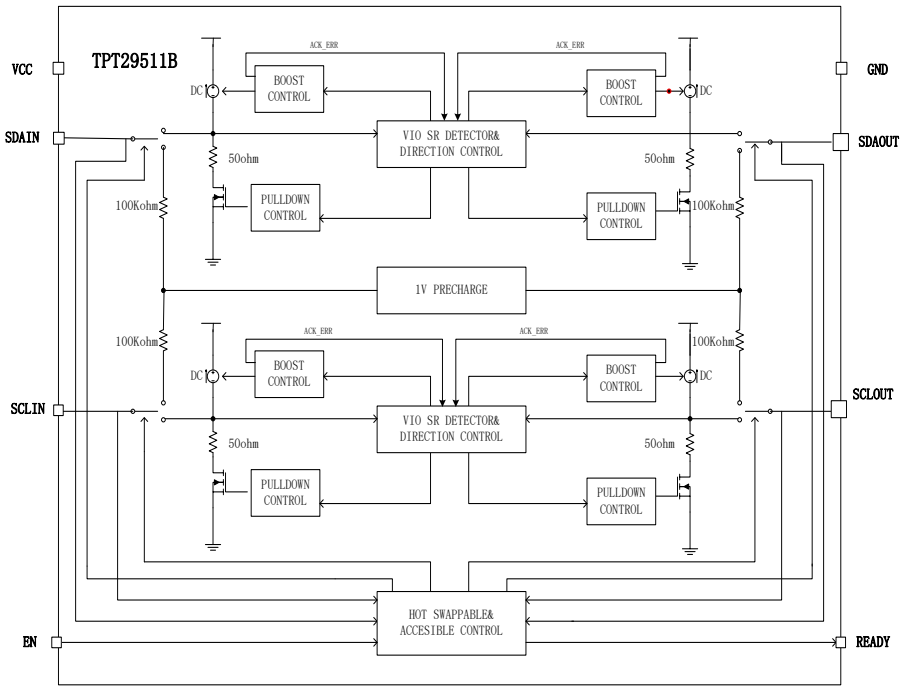


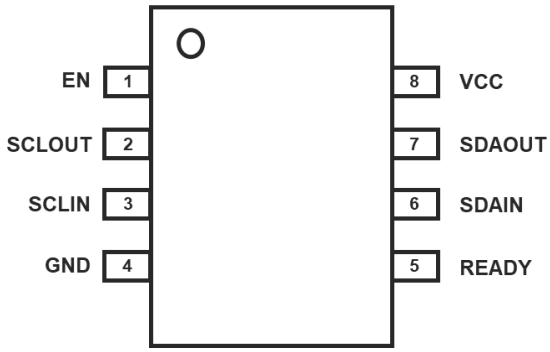
Table of Contents

Revision History

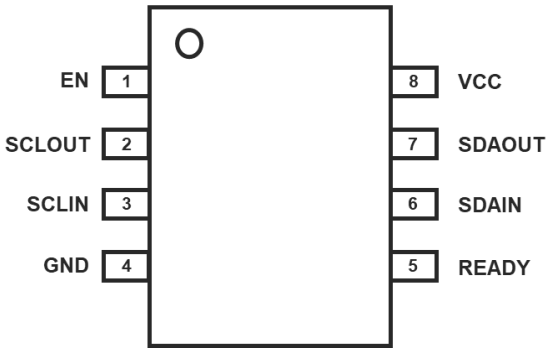
Date	Revision	Notes
2021-01-05	Rev.Pre.0	Initial Version
2022-01-05	Rev.A0	Released version
2022-02-09	Rev.A1	Added SOP8 package
2023-06-13	Rev.A2.1	Updated the tape reel information

Pin Configuration and Functions

TPT29511B-SO1R
SOP8



TPT29511B-VS1R
MSOP8



Pin Functions

Pin		I/O	Description
No.	Name		
1	EN	I	Active-high chip enable pin. If EN is low, the device is in a low current mode.
2	SCLOUT	I/O	Serial clock output to and from the SCL bus on the card
3	SCLIN	I/O	Serial clock input to and from the SCL bus on the backplane
4	GND	–	Ground.
5	READY	O	Open-drain output which pulls LOW when SDAIN and SCLIN are disconnected from SDAOUT and SCLOUT, and goes HIGH when the two sides are connected
6	SDAIN	I/O	Serial data input to and from the SDA bus on the backplane
7	SDAOUT	I/O	Serial data output to and from the SDA bus on the card
8	VCC	–	Power supply

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{CC}	Power supply	−0.5	+7	V
IO PIN	SDAIN, SCLIN, SDAOUT, SCLOUT, EN, READY	−0.5	+7	V
I_{IK}	Input clamp current		−50	mA
I_{OK}	Output clamp current		−50	mA
I_O	Continuous output current		±50	mA
I_{CC}	Continuous current through VCC or GND		±100	mA
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		300	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001(1)	7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002(2)	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter			Min	Max	Unit
V_{CC}	Supply voltage		2.3	5.5	V
V_I	Input voltage range	EN input	0	5.5	V
V_{IO}	Input/output voltage range	SDAIN, SCLIN, SDAOUT, SCLOUT	0	5.5	V
V_O	Output voltage range	READY	0	5.5	V
T_A	Ambient temperature		-40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
8-Pin MSOP	205	44	°C/W
8-Pin SOIC	160	40	°C/W

Electrical Characteristics

All test conditions: V_{CC} = 3.3 V, T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
I_{CC}	Supply current	V_{CC} = 5.5 V SDAIN, SCLIN = 0 V SDAOUT, SCLOUT = 10k R_{PU}		3.7	6	mA
I_{SD}	Supply current in shutdown mode through the VCC pin	EN = 0 V, SDAIN, SCLIN, SDAOUT, SCLOUT = 0 V or V_{CC}, READY pin = Hi-Z EN pulled low after bus connection event (disable pre-charge)		0.7	3	μA
UVLO(1)	Under voltage lockout (rising)	EN = V_{CC} READY = 10 kΩ to V_{CC}		2.15		V
	Under voltage lockout (falling)			2		
DC electrical characteristics						
V_{PRE}	Pre-charge voltage	SDA, SCL = Hi-Z	0.8	1	1.2	V
I_{PU}	RTA pull-up current (1)	Position transition on SDA, SCL $V_{SDA/SCL}$ > 0.8 V, Slew rate = 1.25 V/μs. V_{CC} = 3.3 V		8		mA
I_{LI}	Input pin leakage	SDA/SCL pins = 90% V_{CC}, EN = V_{CC}, SDA/SCL pins = 10% V_{CC}, EN = GND	−1		1	μA
V_{OS}	Input-output offset voltage (SCLIN to SCLOUT, SCLOUT to SCLIN and SDAIN to SDAOUT, SDAOUT to SDAIN)	R_{PU} for SDA/SCL = 10 kΩ		105	175	mV
I_{I_RDY}	Ready pin leakage	EN = V_{CC}, READY = V_{CC}, Bus connected	−1		1	μA
V_{IH}	High-level input voltage	EN	0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	EN	0		0.3 × V_{CC}	V
V_{OL_IO}	Low-level output voltage	SDAIN, SCLIN, SDAOUT, SCLOUT, I_{OL} = 3 mA, V_{IN} = 0.1 V		0.25	0.4	V
V_{OL_READY}	Low-level output voltage	Power on, READY = L, I_{OL} = 3 mA	0		0.4	V
		Power off, R_{PU} = 10kΩ to 3.3 V		0.6	0.9	V
$C_{IN(EN)}$	EN input capacitance (1)	V_{EN} = 0 V or V_{CC}, f = 400 kHz		4		pF
$C_{IO(READY)}$	READY output capacitance (1)	V_{READY} = 0 V or V_{CC}, f = 400 kHz		6		pF
$C_{IO(SDA/SCL)}$	SDA/SCL pin capacitance (1)	V_{PIN} = 0 V or V_{CC}, f = 400 kHz		8.8		pF

(1) Test data based on bench test and design simulation.

AC Electrical Characteristics

All test conditions: V_{CC} = 3.3 V, T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up switching						
t_{EN}	Time from V_{POR} to digital being ready	V_{CC} transition from 0 V to V_{CC}, Time from V_{POR} to earliest stop bit recognized	50	103	150	µs
t_{IDLE}	Bus idle time to READY active	SDA, SCL = 10 kΩ to V_{CC} EN = V_{CC} Measured at 0.5 × V_{CC}	50	100	150	µs
$t_{DISABLE}$	Time from EN high to low to READY low	SDA, SCL = 10 kΩ to V_{CC} READY = 10 kΩ to V_{CC} Measured at 0.5 × V_{CC}		30	200	ns
t_{STOP}	SDAIN to READY delay after stop condition	SDA, SCL = 10 kΩ to V_{CC} READY = 10 kΩ to V_{CC} Measured at 0.5 × V_{CC}		1.2	2	µs
t_{READY}	SCLOUT/SDAOUT to READY	SDA, SCL = 10 kΩ to V_{CC} READY = 10 kΩ to V_{CC} Measured at 0.5 × V_{CC}		1.2	2	µs
t_{PLH}	Low to high propagation delay (1)	R_{PU} for SDA/SCL = 10 kΩ C_L = 100 pF per pin Measured at 0.5 × V_{CC}		0	– (1)	ns
t_{PHL}	High to low propagation delay	R_{PU} for SDA/SCL = 10 kΩ C_L = 100 pF per pin Measured at 0.5 × V_{CC}		77	150	ns

(1) t_{PLH} typ data based on bench test and design simulation, the max value depends on the input source and cannot test in the FT.

AC Electrical Characteristics (Continued)

All test conditions: V_{CC} = 3.3 V, T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
Timing characteristics (reference to I²C 400 kHz) (1)					
f_{SCL_MAX}	Maximum SCL clock frequency	400			kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
$t_{HD;STA}$	Hold time for a repeated START condition	0.6			µs
$t_{SU;STA}$	Set-up time for a repeated START condition	0.6			µs
$t_{SU;STO}$	Set-up time for a STOP condition	0.6			µs
$t_{HD;DAT}$	Data hold time	0			ns
$t_{SU;DAT}$	Data set-up time	100			ns
t_{LOW}	LOW period of the SCL clock	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	0.6			µs
t_F	Fall time of both SDA and SCL signals (2)	20+ 0.1*Cb		150	ns
t_R	Rise time of both SDA and SCL signals (2)	20 +0.1*Cb		150	ns

(1) Reference to I²C standard @400 kHz, NOT tested in production.

(2) Cb is total capacitance of one bus line in pF.

Typical Performance Characteristics

All test conditions: V_{IN} = 5 V, T_A = +25°C, unless otherwise noted.

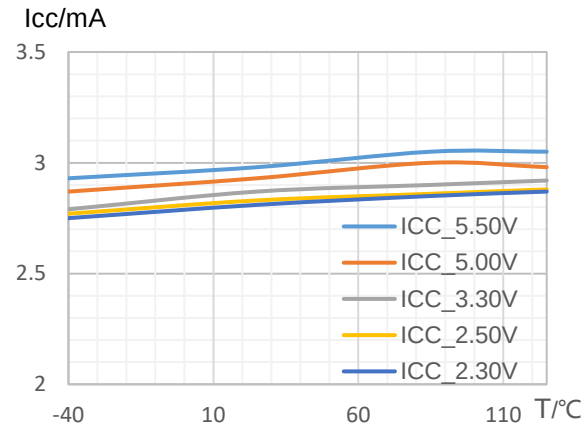


Figure 1. I_{CC} versus temperature

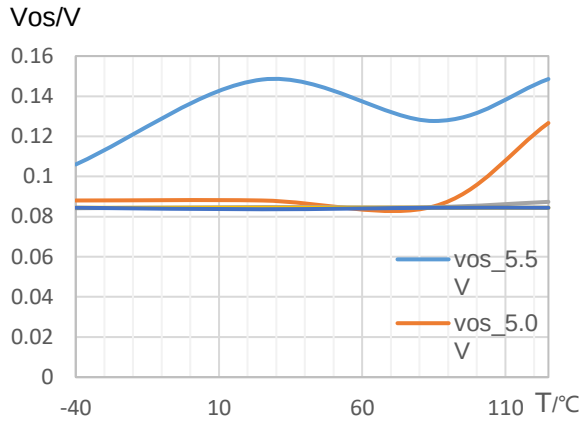


Figure 2. Vos versus temperature

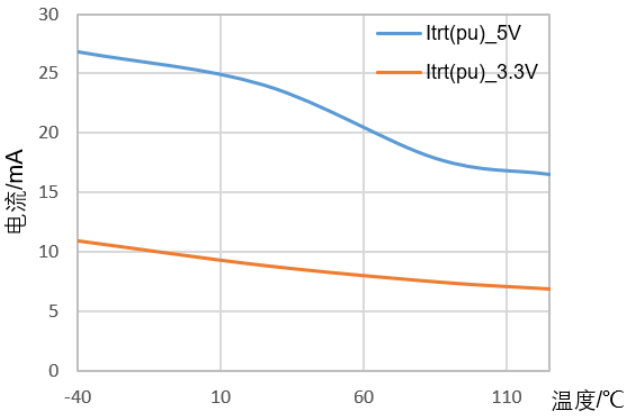


Figure 3. Itrt(pu) versus temperature

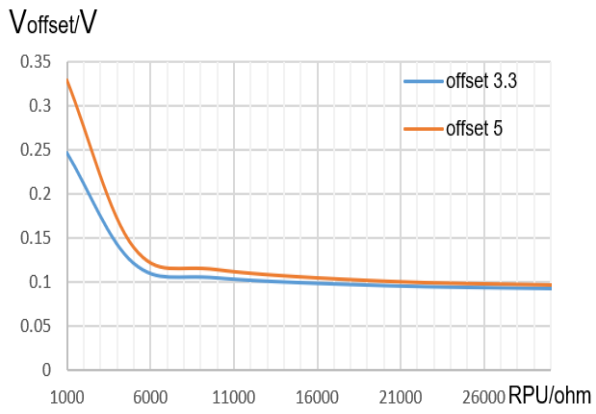


Figure 4. Vos versus Rpu

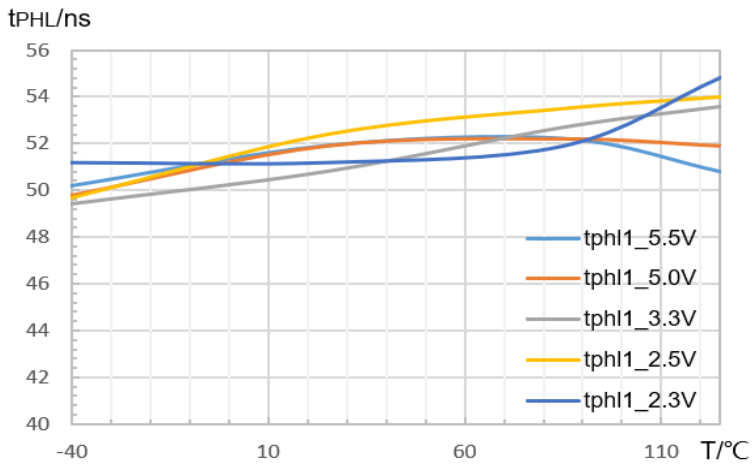
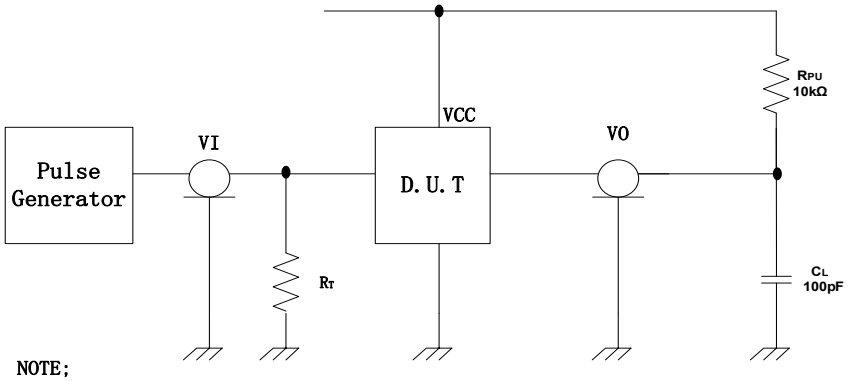


Figure 5. t_{PHL} versus temperature

Test Circuitry



NOTE;
R_{PU} is pull up resistor, C_L is load capacitance(includes jig and probe capacitance).
R_T is terminations resistance(equal to the output impedance Z_O of the pulse generators.)

Figure 6 Test Circuitry of TPT29511

Test Timing Diagrams

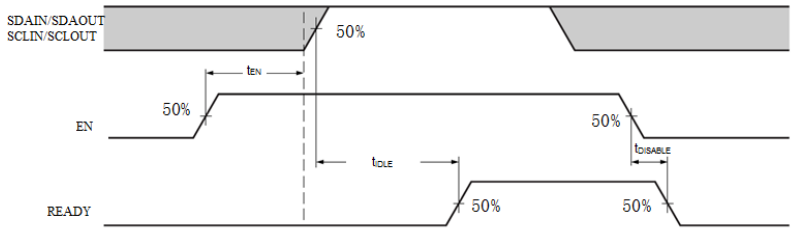


Figure 7 Timing for t_{EN}, t_{IDLE}, $t_{DISABLE}$

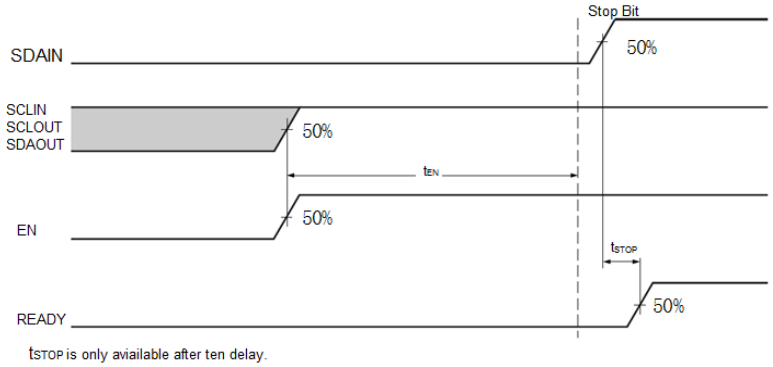


Figure 8 Timing for t_{STOP}

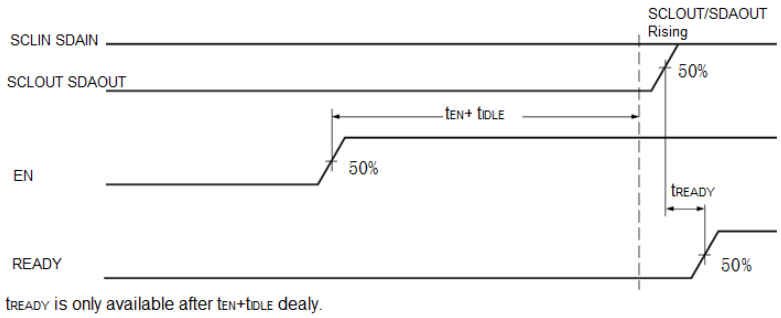


Figure 9 Timing for t_{READY}

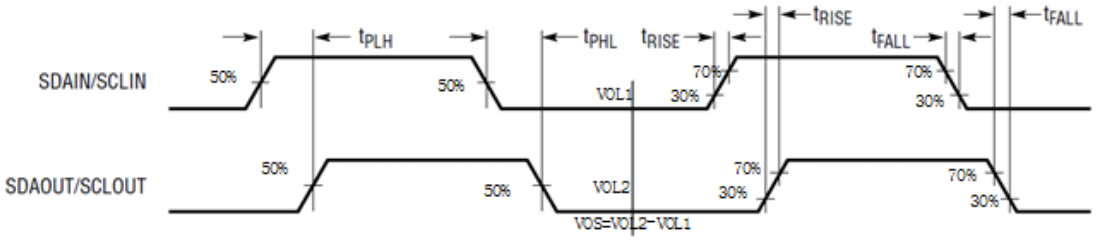


Figure 10 Timing for t_{PHL}, t_{PLH}, t_R, t_F, V_{OS}

Detailed Description

Overview

The TPT29511B device is a dual bidirectional I²C and SMBus Hot-swap buffer with an enable (EN) input, and work from 2.3 V to 5.5 V V_{CC}, which supports IO cards live insertion and removal from backplane. Control circuit prevents the backplane-side I²C lines (in) from the other card-side I²C lines (out) until a stop command or bus idle condition occurs on the backplane without bus contention on the card. When the connection is made, the TPT29511B provides bidirectional buffering, keeping the backplane and card capacitances isolated.

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The TPT29511B incorporates a digital ENABLE input pin, which enables the device when asserted HIGH and forces the device into a low current mode when asserted LOW, and an open-drain READY output pin, which indicates that the backplane and card sides are connected together (HIGH) or not (LOW).

Functional Block Diagram

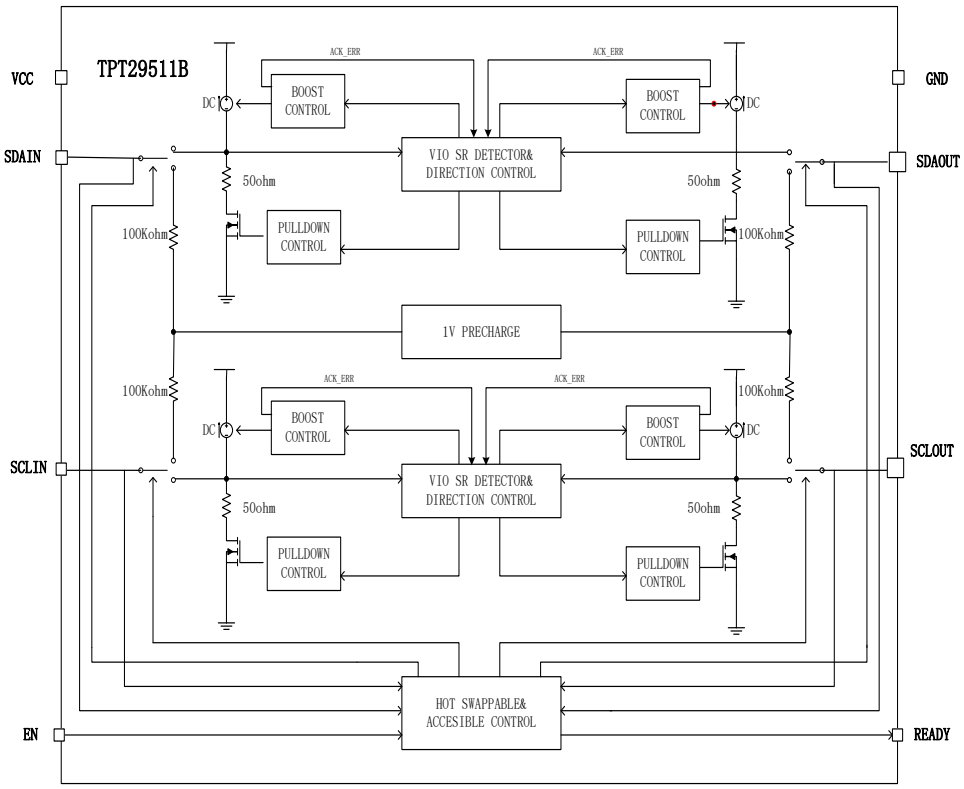


Figure 11. Functional Block Diagram

Feature Description

Enable (EN)

The device is active mode as pin EN is high voltage level. If EN is low, the device is in a low current mode.

Under-voltage Lockout (UVLO)

The device uses an under-voltage lockout circuit to keep the device in shutdown mode until the supply voltage is higher than the UVLO threshold.

Over Voltage Protection (OVP)

The device uses an over-voltage protection circuit to prevent the device from damage when the supply voltage is higher than OVP threshold.

READY

The output pin will goes HIGH to indicate that SDAIN and SCLIN are connected from SDAOUT and SCLOUT. And pull LOW when the two sides are disconnected. The pin is driven by an open-drain pull-down capable of sinking 6 mA while holding 0.4 V on the pin. A 10 kΩ resistor is suggested connecting to VCC to provide the pull-up status.

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT29511B device is a dual bidirectional I2C and SMBus Hot-swap buffer, which supports IO cards live insertion and removal from backplane, such as the application in Servers/Storages and Enterprise Switching.

Typical Application

错误!未找到引用源。 shows the typical application schematic.

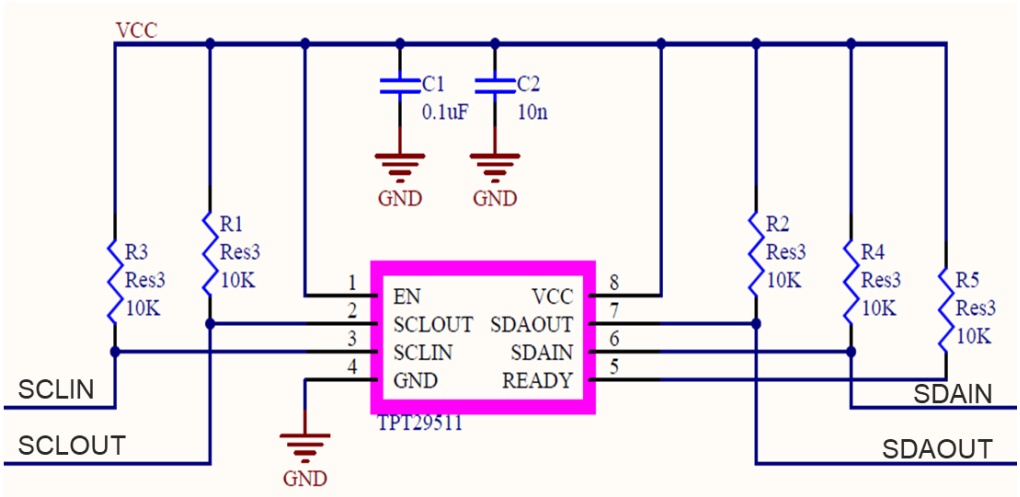
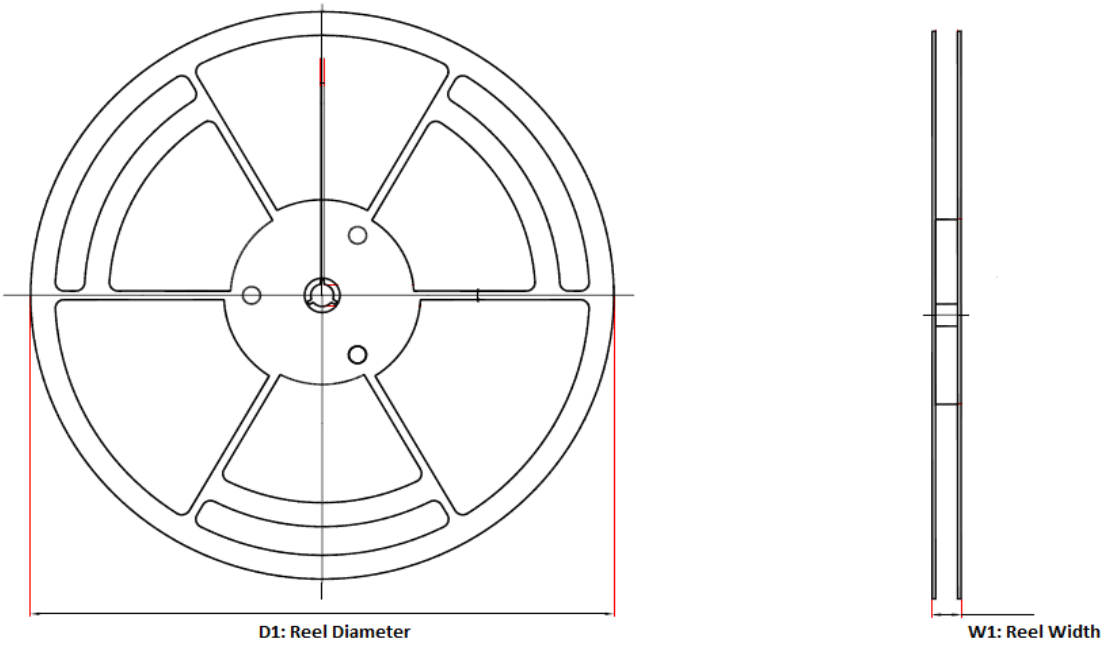


Figure 13. Reference Circuitry of TPT29511

Tape and Reel Information

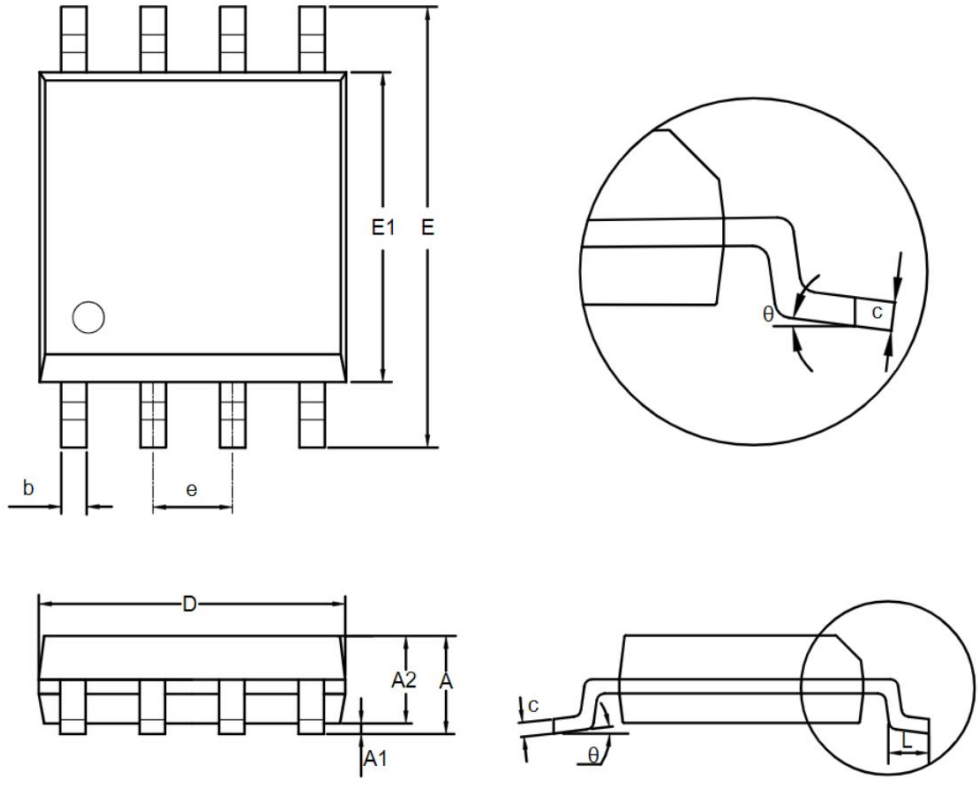


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPT29511B-VS1R	8-Pin MSOP	330.0	5.2	1.5	12.0	17.6	3.3	8.0	Q1
TPT29511B-SO1R	8-Pin SOP	330.0	6.5	2.0	12.0	17.6	5.4	8.0	Q1

Package Outline Dimensions

VS1R (MSOP8)

Package Outline Dimensions VS1(MSOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

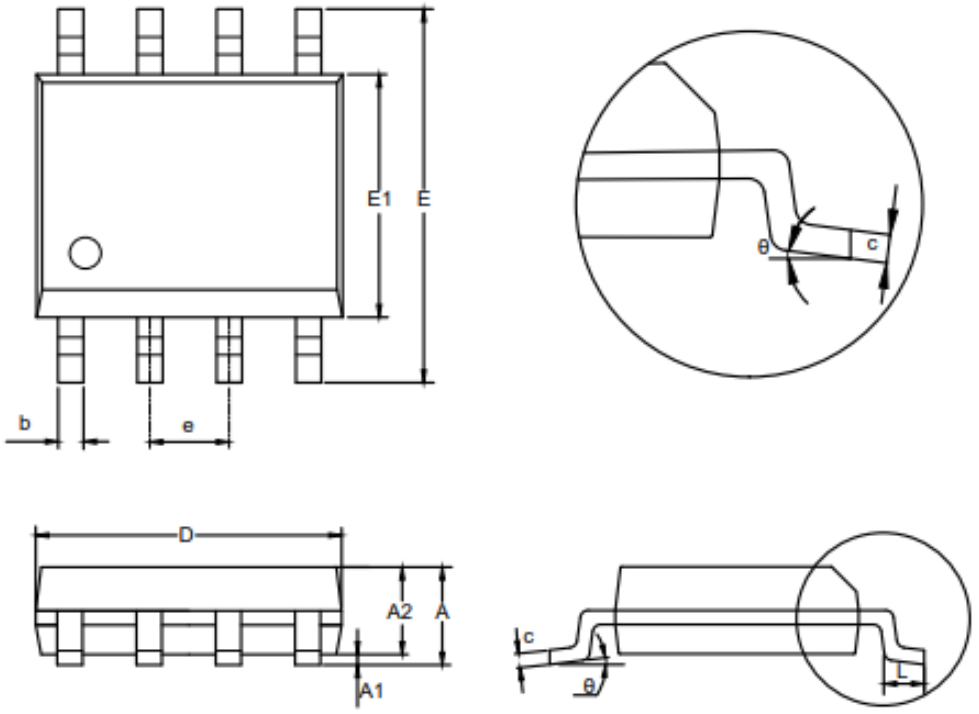
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Package Outline Dimensions

SO1R (SOP8)

Package Outline Dimensions SO1(SOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29511B-VS1R	−40 to 125°C	8-Pin MSOP	9511B	MSL3	Tape and Reel, 3000	Green
TPT29511B-SO1R	−40 to 125°C	8-Pin SOP	9511B	MSL3	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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