

Features

- I²C-Bus to 8-bit GPIO Expander
- Operating Supply Voltage from 1.65 V to 5.5 V
- Allows Bidirectional Voltage-level Translation and GPIO Expansion Between 1.8-V, 2.5-V, 3.3-V, and 5-V I²C-bus and P-ports
- Low Standby Current
- 400-kHz Fast-Mode I²C-bus
- 5-V Tolerant I/Os
- Open-Drain Active Low Interrupt Output ($\overline{\text{INT}}$)
- One Address Pin Allowing up to 2 Different Addresses
- Internal Power-on Reset
- Active-Low Reset Input ($\overline{\text{RESET}}$)
- Power-up with all Channels Configured as Inputs
- ESD Protection Exceeds JESD 22
 - 4000-V Human Body Model
 - 1500-V Charged-Device Model

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers

Description

The TPT29508 is an 8-bit GPIO expander with interruption for I²C-bus applications. It operates from a supply voltage range of 1.65 V to 5.5 V on both the I²C-bus side (V_{CCI}) and the P-port side (V_{CCP}), which allows bidirectional voltage-level translation and GPIO expansion between 1.8-V, 2.5-V, 3.3-V, and 5-V I²C-bus and P-ports.

The TPT29508 features a set of 8-bit Configuration, Input, Output, and Polarity Inversion registers. The open-drain interrupt ($\overline{\text{INT}}$) output is changeable when any input state changes from its related register state. $\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. A power-on reset initializes all registers to their default values and resets the device state machine. The TPT29508 also has a hardware $\overline{\text{RESET}}$ pin to reset the device to its default state.

All input/output pins do not have internal pull-up resistors, which helps reduce power consumption when communicating with external I/Os. One hardware pin (ADDR) selects the I²C-bus address and allows up to two devices to share the same I²C-bus.

The TPT29508 is available in the QFN1.8X2.6-16 package, and is characterized from -40°C to +105°C.

Typical Application Circuit

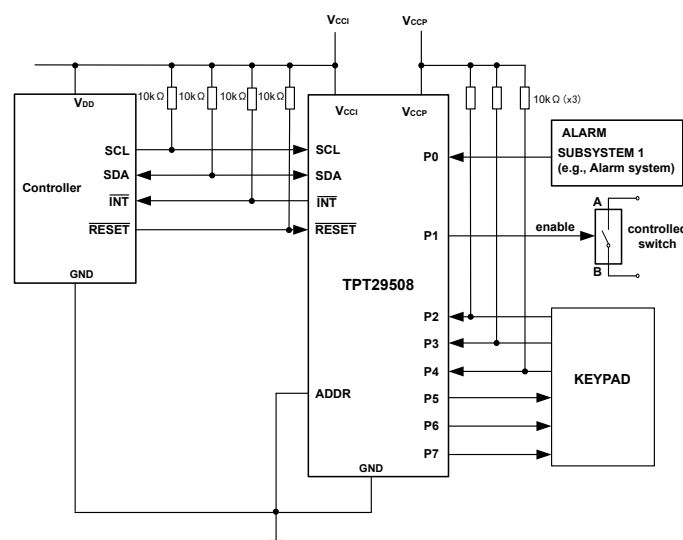


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Revision History

Date	Revision	Notes
2026-01-30	Rev.A.0	Released version.

Pin Configuration and Functions

QFN1.8X2.6-16 Package

Top View

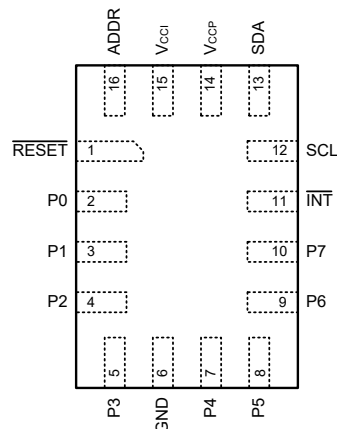


Table 1. Pin Functions: TPT29508

Pin	Name	I/O	Description
1	$\overline{\text{RESET}}$	I	Reset input, active LOW. Connect to V_{CCI} through a pull-up resistor if not used.
2	P0	I/O	P-port I/O. Push-pull design structure. At power on, P0 is configured as an input.
3	P1	I/O	P-port I/O. Push-pull design structure. At power on, P1 is configured as an input.
4	P2	I/O	P-port I/O. Push-pull design structure. At power on, P2 is configured as an input.
5	P3	I/O	P-port I/O. Push-pull design structure. At power on, P3 is configured as an input.
6	GND	GND	Ground.
7	P4	I/O	P-port I/O. Push-pull design structure. At power on, P4 is configured as an input.
8	P5	I/O	P-port I/O. Push-pull design structure. At power on, P5 is configured as an input.
9	P6	I/O	P-port I/O. Push-pull design structure. At power on, P6 is configured as an input.
10	P7	I/O	P-port I/O. Push-pull design structure. At power on, P7 is configured as an input.
11	$\overline{\text{INT}}$	O	Interrupt output. Connect to V_{CCI} through a pull-up resistor.
12	SCL	I	Serial clock bus. Connect to V_{CCI} through a pull-up resistor.
13	SDA	I/O	Serial data bus. Connect to V_{CCI} through a pull-up resistor.
14	V_{CCP}	Supply	Supply voltage for P-ports.
15	V_{CCI}	Supply	Supply voltage of I ² C-bus. Connect directly to the V_{CC} of the external I ² C controller. Provides voltage level translation.
16	ADDR	I	Address input. Connect directly to V_{CCP} or ground

I²C to 8-bit GPIO Expander with Voltage-level Translation
Specifications
Absolute Maximum Ratings ⁽¹⁾

Parameter		Min	Max	Unit
V _{CCI}	Supply Voltage for I ² C Pins	-0.5	6.5	V
V _{CC1}	Supply Voltage for P-ports	-0.5	6.5	V
V _I	Input Voltage	-0.5	6.5	V
V _O	Output Voltage	-0.5	6.5	V
I _{IK}	Input Clamp Current, ADDR, $\overline{\text{RESET}}$, SCL, V _I < 0	-20		mA
I _{OK}	Output Clamp Current, $\overline{\text{INT}}$, V _O < 0	-20		mA
I _{IOK}	Input/Output Clamp Current, P-port, V _O < 0 or V _O > V _{CCP}	-20	20	mA
	Input/Output Clamp Current, SDA, V _O < 0 or V _O > V _{CC1}	-20	20	mA
I _{OL}	Continuous Output Low Current, P-port, V _O = 0 to V _{CCP}		50	mA
	Continuous Output Low Current, SDA, $\overline{\text{INT}}$, V _O = 0 to V _{CC1}		25	mA
I _{OH}	Continuous Output High Current, P-port, V _O = 0 to V _{CCP}		50	mA
I _{CC}	Continuous Current through GND		250	mA
	Continuous Current through V _{CCP}		160	mA
	Continuous Current through V _{CC1}		10	mA
T _J	Maximum Junction Temperature		150	°C
T _{stg}	Storage Temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

I²C to 8-bit GPIO Expander with Voltage-level Translation
Recommended Operating Conditions

Over-operating free-air temperature range (unless otherwise noted).

Parameter			Min	Max	Unit
V _{CCI}	Supply Voltage for I ² C Pins		1.65	5.5	V
V _{CC}	Supply Voltage for P-ports		1.65	5.5	V
V _{IH}	High-level Input Voltage	SCL, SDA	0.7 × V _{CCI}	V _{CCI}	V
		$\overline{\text{RESET}}$	0.7 × V _{CCI}	5.5	V
		ADDR, P7 ~ P0	0.7 × V _{CCP}	5.5	V
V _{IL}	Low-level Input Voltage	SCL, SDA, $\overline{\text{RESET}}$	-0.5	0.3 × V _{CCI}	V
		ADDR, P7 ~ P0	-0.5	0.3 × V _{CCP}	V
I _{OH}	High-level Output Current	P7 ~ P0		10	mA
I _{OL}	Low-level Output Current	P7 ~ P0		25	mA
		$\overline{\text{INT}}$, SDA		6	mA
T _A	Operating Temperature Range	V _{CC} = 1.65 ~ 3.6 V	-40	125	°C
		V _{CC} = 4.5 ~ 5.5 V	-40	105	°C

Thermal Information

Package Type	θ _{JA}	θ _{JC}	Unit
QFN1.8X2.6-16	110.8	65.1	°C/W

I²C to 8-bit GPIO Expander with Voltage-level Translation
Electrical Characteristics

 All test conditions: $V_{CC1} = 1.65\text{ V} \sim 5.5\text{ V}$, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit	
V_{IK}	Input Diode Clamp Voltage	$I_I = -18\text{ mA}$, $V_{CCP} = 1.65\text{ V to }5.5\text{ V}$	-1.2			V	
V_{POR}	Power-on Reset Voltage, V_{CCP} Rising	$V_I = V_{CCP}$ or GND; $I_O = 0\text{ mA}$		1.25	1.5	V	
	Power-on Reset Voltage, V_{CCP} Falling	$V_I = V_{CCP}$ or GND; $I_O = 0\text{ mA}$	0.7	1.2		V	
V_{OH}	High-level Output Voltage, P-port	$I_{OH} = -8\text{ mA}$; $V_{CCP} = 1.65\text{ V}$	1.2			V	
		$I_{OH} = -8\text{ mA}$; $V_{CCP} = 2.3\text{ V}$	1.8			V	
		$I_{OH} = -8\text{ mA}$; $V_{CCP} = 3.0\text{ V}$	2.6			V	
		$I_{OH} = -8\text{ mA}$; $V_{CCP} = 4.5\text{ V}$	4.1			V	
	High-level Output Voltage, P-port	$I_{OH} = -10\text{ mA}$; $V_{CCP} = 1.65\text{ V}$	1.1			V	
		$I_{OH} = -10\text{ mA}$; $V_{CCP} = 2.3\text{ V}$	1.7			V	
		$I_{OH} = -10\text{ mA}$; $V_{CCP} = 3.0\text{ V}$	2.5			V	
		$I_{OH} = -10\text{ mA}$; $V_{CCP} = 4.5\text{ V}$	4.0			V	
V_{OL}	Low-level Output Voltage, P-port	$I_{OL} = 8\text{ mA}$; $V_{CCP} = 1.65\text{ V}$			0.45	V	
		$I_{OL} = 8\text{ mA}$; $V_{CCP} = 2.3\text{ V}$			0.25	V	
		$I_{OL} = 8\text{ mA}$; $V_{CCP} = 3.0\text{ V}$			0.25	V	
		$I_{OL} = 8\text{ mA}$; $V_{CCP} = 4.5\text{ V}$			0.2	V	
	Low-level Output Voltage, P-port	$I_{OL} = 10\text{ mA}$; $V_{CCP} = 1.65\text{ V}$			0.6	V	
		$I_{OL} = 10\text{ mA}$; $V_{CCP} = 2.3\text{ V}$			0.3	V	
		$I_{OL} = 10\text{ mA}$; $V_{CCP} = 3.0\text{ V}$			0.25	V	
		$I_{OL} = 10\text{ mA}$; $V_{CCP} = 4.5\text{ V}$			0.2	V	
I_{OL}	Low-level Output Current, SDA	$V_{OL} = 0.4\text{ V}$; $V_{CC1} = 1.65\text{ V to }5.5\text{ V}$	3			mA	
	Low-level Output Current, $\overline{\text{INT}}$	$V_{OL} = 0.4\text{ V}$; $V_{CC1} = 1.65\text{ V to }5.5\text{ V}$	3			mA	
I_I	Input Current: SCL, SDA, $\overline{\text{RESET}}$	$V_{CC1} = 1.65\text{ V to }5.5\text{ V}$, $V_I = V_{CC1}$ or GND	-1		1	μA	
	Input Current: ADDR	$V_{CCP} = 1.65\text{ V to }5.5\text{ V}$, $V_I = V_{CCP}$ or GND	-1		1	μA	
I_{IH}	High-level Input Current: P-port	$V_I = V_{CCP}$; $V_{CCP} = 1.65\text{ V to }5.5\text{ V}$	-1		1	μA	
I_{IL}	Low-level Input Current: P-port	$V_I = \text{GND}$; $V_{CCP} = 1.65\text{ V to }5.5\text{ V}$	-1		1	μA	
I_{CC} ($I_{CC1} + I_{CCP}$)	Supply Current	Active mode, V_I on SDA and $\overline{\text{RESET}} = V_{CC1}$ or GND, V_I on P-port and ADDR = V_{CCP} or	$V_{CCP} = 5.5\text{ V}$		23.2	33	μA
		$V_{CCP} = 3.6\text{ V}$		12.3	15	μA	
		$V_{CCP} = 2.3\text{ V}$		6.8	11	μA	

I²C to 8-bit GPIO Expander with Voltage-level Translation

Parameter		Conditions	Min	Typ	Max	Unit	
		GND, I _O = 0 ; I/O = inputs; f _{SCL} = 400 kHz	V _{CCP} = 1.65 V		4.7	8	μA
		Standby Mode, V _I on SCL, SDA and $\overline{\text{RESET}}$ = V _{CCI} or GND, V _I on P-port and ADDR = V _{CCP} or GND, I _O = 0; I/O = inputs; f _{SCL} = 0 Hz	V _{CCP} = 5.5 V		1.5	7	μA
			V _{CCP} = 3.6 V		0.9	3.2	μA
			V _{CCP} = 2.3 V		0.5	1.7	μA
			V _{CCP} = 1.65 V		0.3	1.7	μA
ΔI _{CCI}	Additional Current in Standby Mode	SCL, SDA and $\overline{\text{RESET}}$, One input at V _{CCI} – 0.6 V, Other inputs at V _{CCI} or GND	V _{CCP} = 1.65 V to 5.5 V			7	μA
ΔI _{CCP}		P-port and ADDR, One input at V _{CCP} – 0.6 V, Other inputs at V _{CCP} or GND	V _{CCP} = 1.65 V to 5.5 V			7	μA
C _i	Input Capacitance (1)	SCL, V _I = V _{CCI} or GND; V _{CCP} = 1.65 V to 5.5 V		3			pF
C _{io}	Input/Output Capacitance (1)	SDA, V _{I/O} = V _{CCI} or GND; V _{CCP} = 1.65 V to 5.5 V		3			pF
		P-port, V _{I/O} = V _{CCP} or GND; V _{CCP} = 1.65 V to 5.5 V		5			pF

(1) Parameters are provided by lab bench tests and design simulation.

I²C to 8-bit GPIO Expander with Voltage-level Translation
I²C Interface Timing Requirements

Over recommended operating free-air temperature range, unless otherwise noted. ⁽¹⁾

Parameter		Conditions	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
f _{scl}	I ² C Clock Frequency		0	100	0	400	kHz
t _{sch}	I ² C Clock High Time		4		0.6		μs
t _{scl}	I ² C Clock Low Time		4.7		1.3		μs
t _{sp}	I ² C Spike Time			50		50	ns
t _{sds}	I ² C Serial-data Setup Time		250		100		ns
t _{sdh}	I ² C Serial-data Hold Time		0		0		ns
t _{icr}	I ² C Input Rise Time			1000	20	300	ns
t _{icf}	I ² C Input Fall Time			300	20 + 0.1 C _b	300	ns
t _{ocf}	I ² C Output Fall Time	10-pF to 400-pF bus		300	20 + 0.1 C _b	300	ns
t _{buf}	I ² C Bus Free Time Between Stop and Start		4.7		1.3		μs
t _{sts}	I ² C Start or Repeated Start Condition Setup		4.7		0.6		μs
t _{sth}	I ² C Start or Repeated Start Condition Hold		4		0.6		μs
t _{sps}	I ² C Stop Condition Setup		4		0.6		μs
t _{vd(data)}	Valid Data Time	SCL low to SDA output valid		3.45		0.9	μs
t _{vd(ack)}	Valid Data Time of ACK Condition	ACK signal from SCL low to SDA (out) low		3.45		0.9	μs
C _b	I ² C Bus Capacitive Load ⁽²⁾			400		400	pF

(1) All timing requirements should refer to the I²C standard, and parameters in the table are tested by the lab bench.

(2) C_b is the total capacitance of one bus line in pF.

Reset Timing Requirements

Over recommended operating free-air temperature range, unless otherwise noted.

Parameter		Conditions	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
t _W	Reset Pulse Duration		30		30		ns
t _{REC}	Reset Recovery Time		0		0		ns
t _{RESET}	Time to Reset	V _{CCP} = 3.6 V to 5.5 V	400		400		ns
		V _{CCP} = 2.3 V to 3.6 V	400		400		ns
		V _{CCP} = 1.65 V to 2.3 V	550		550		ns

(1) Parameters are provided by lab bench tests and design simulation.

Switching Characteristics

Over recommended operating free-air temperature range, C_L ≤ 100 pF, unless otherwise noted.

Parameter		From (Input)	To (Output)	Standard Mode		Fast Mode		Unit
				Min	Max	Min	Max	
t _{iv}	Interrupt Valid Time	P-port	$\overline{\text{INT}}$		4		4	μs
t _{ir}	Interrupt Reset Delay Time	SCL	$\overline{\text{INT}}$		4		4	μs
t _{pv}	Output Data Valid, V _{CCP} = 2.3 V to 5.5 V	SCL	P-port		250		250	ns
	Output Data Valid, V _{CCP} = 1.65V to 2.3V				300		300	ns
t _{ps}	Input Data Setup Time	P-port	SCL	150		150		ns
t _{ph}	Input Data Hold Time	P-port	SCL	1		1		μs

(1) Parameters are provided by lab bench tests and design simulation.

Typical Performance Characteristics

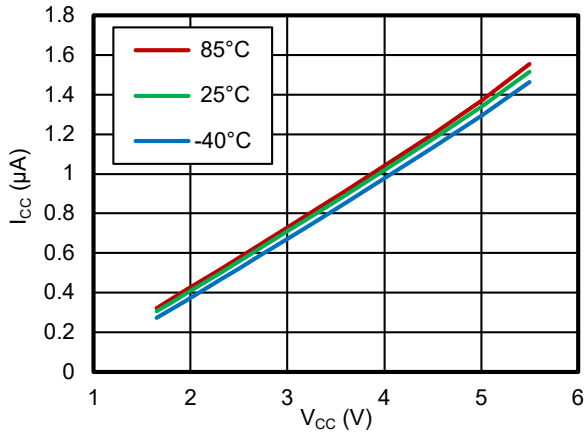


Figure 1. Standby Supply Current vs. Supply Voltage

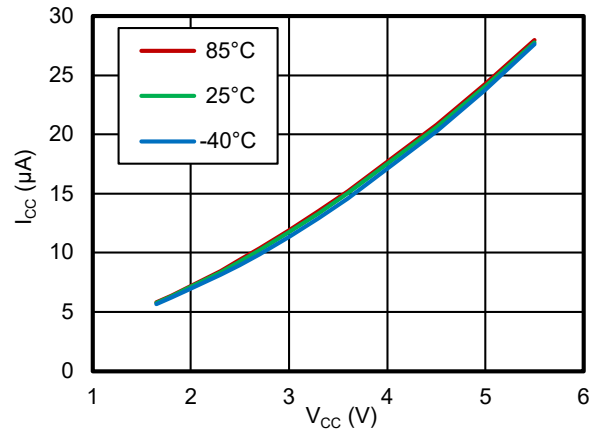


Figure 2. Supply Current vs. Supply Voltage

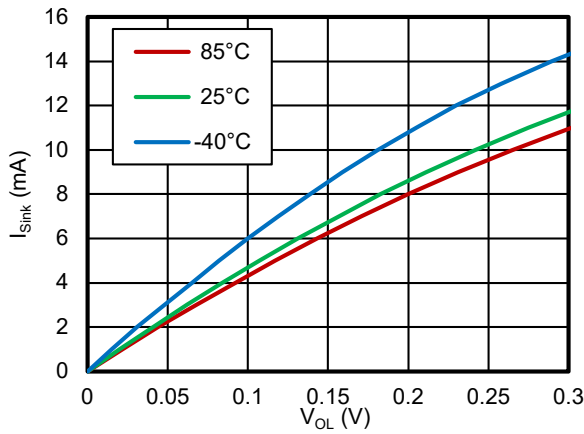


Figure 3. I/O Sink Current vs. VOL (V_{CCP} = 1.65 V)

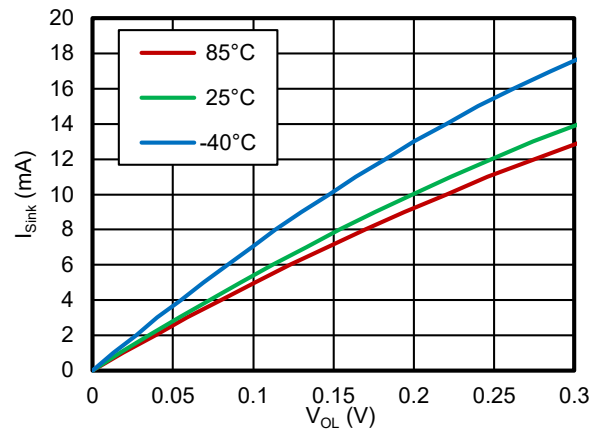


Figure 4. I/O Sink Current vs. VOL (V_{CCP} = 1.8 V)

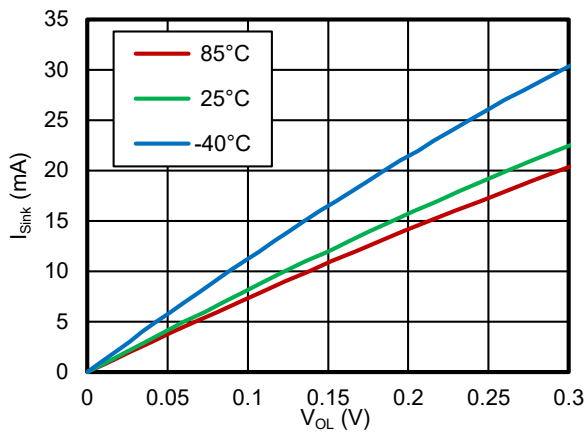


Figure 5. I/O Sink Current vs. VOL (V_{CCP} = 2.5 V)

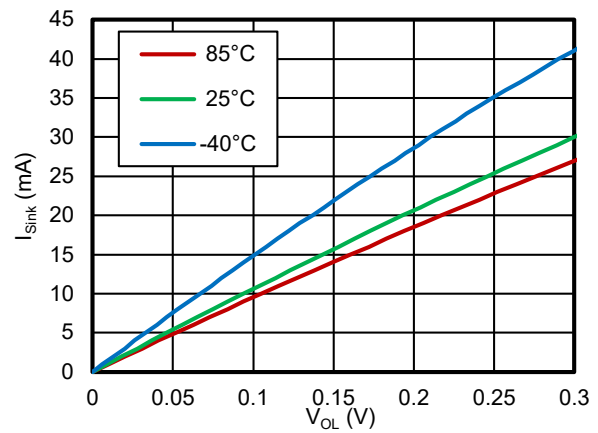


Figure 6. I/O Sink Current vs. VOL (V_{CCP} = 3.3 V)

I²C to 8-bit GPIO Expander with Voltage-level Translation

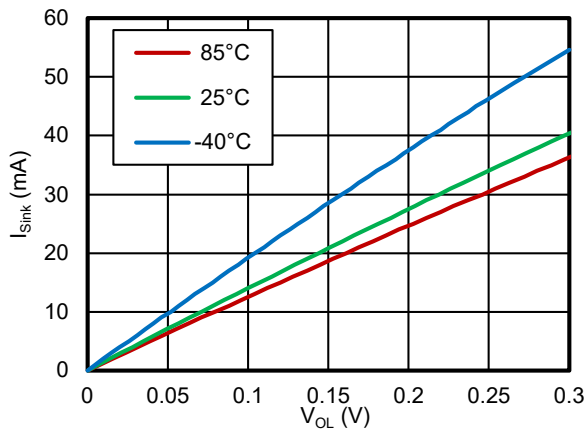


Figure 7. I/O Sink Current vs. V_{OL} (V_{CCP} = 5 V)

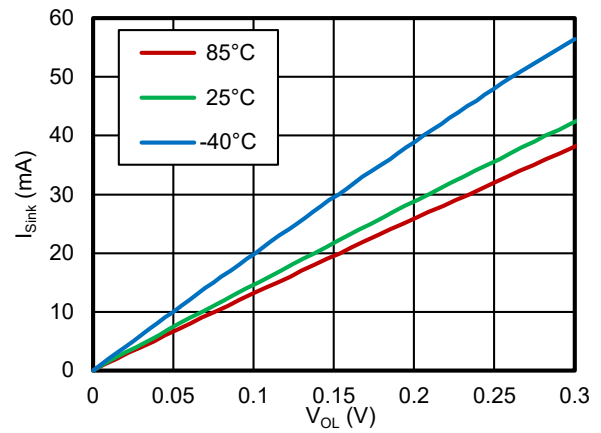


Figure 8. I/O Sink Current vs. V_{OL} (V_{CCP} = 5.5 V)

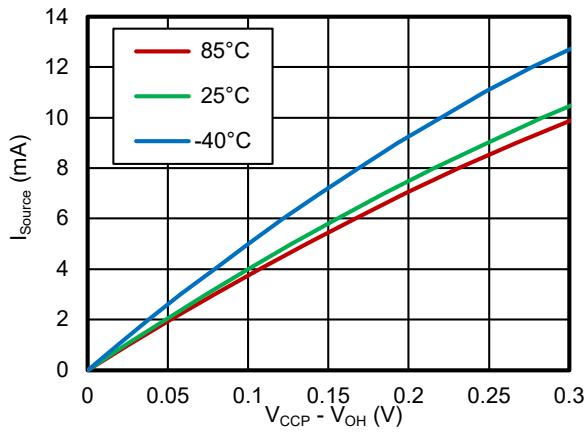


Figure 9. I/O Source Current vs. V_{OH} (V_{CCP} = 1.65 V)

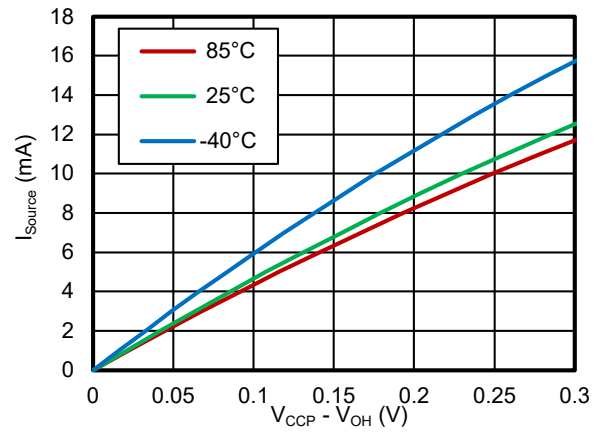


Figure 10. I/O Source Current vs. V_{OH} (V_{CCP} = 1.8 V)

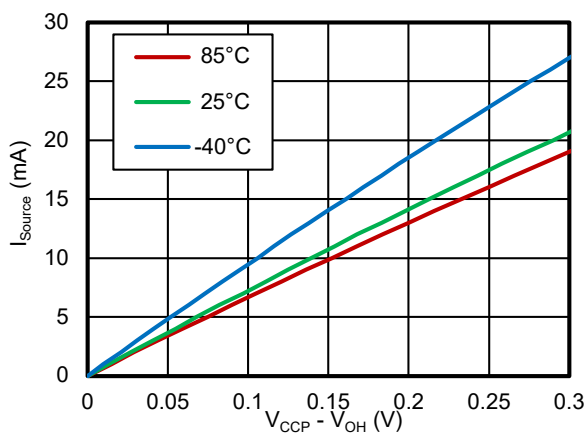


Figure 11. I/O Source Current vs. V_{OH} (V_{CCP} = 2.5 V)

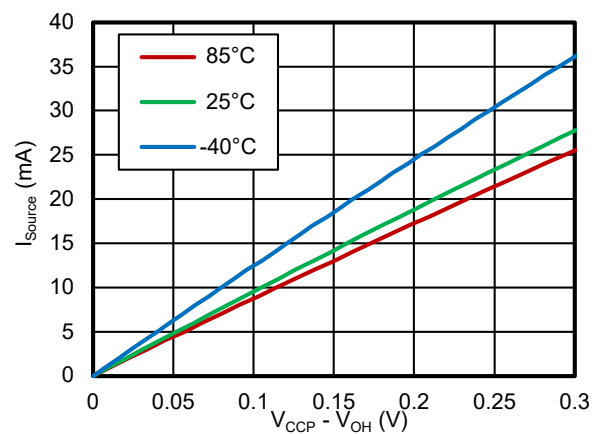


Figure 12. I/O Source Current vs. V_{OH} (V_{CCP} = 3.3 V)

I²C to 8-bit GPIO Expander with Voltage-level Translation

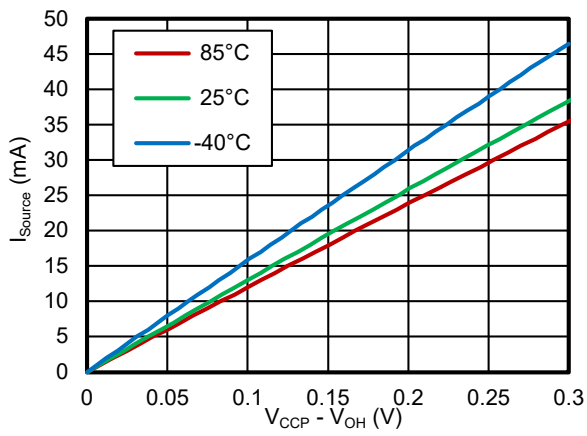


Figure 13. I/O Source Current vs. V_{OH} (V_{CCP} = 5 V)

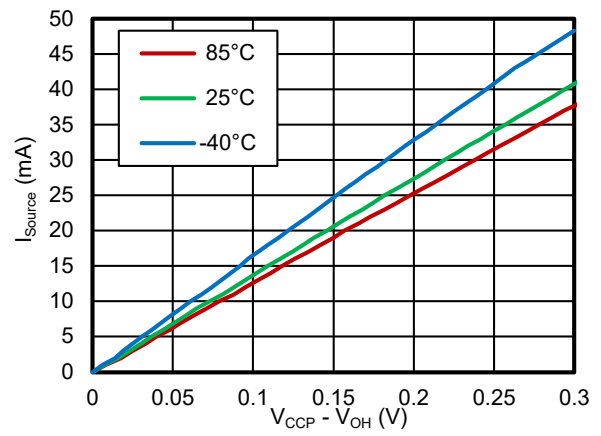


Figure 14. I/O Source Current vs. V_{OH} (V_{CCP} = 5.5 V)

Parameter Measurement Waveforms

I²C Interface Load Circuit and Waveforms

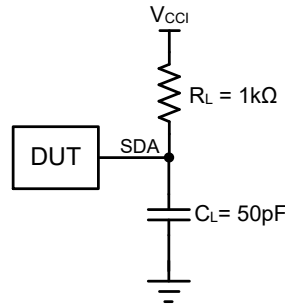


Figure 15. SDA Load Configuration

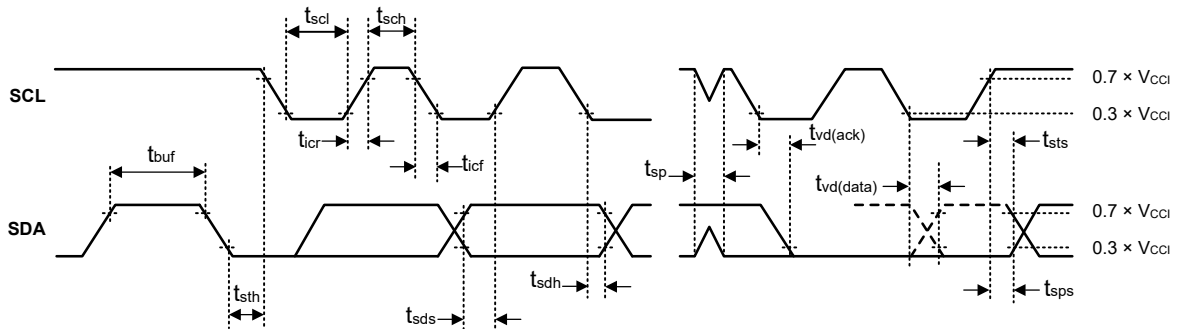


Figure 16. Definition of Timing on the I²C-bus

Interrupt Load Circuit and Waveforms

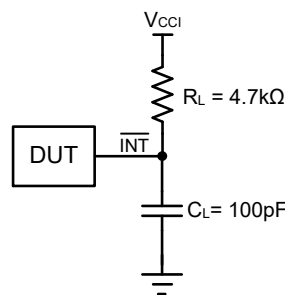


Figure 17. Interrupt Load Configuration

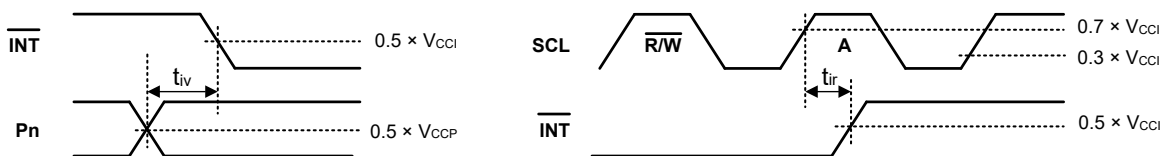


Figure 18. Definition of Interrupt Timing

I²C to 8-bit GPIO Expander with Voltage-level Translation

P-Port Load Circuit and Waveforms

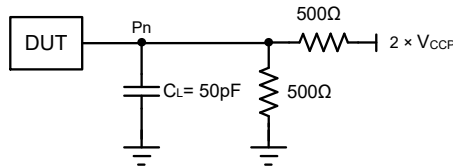


Figure 19. P-Port Load Configuration

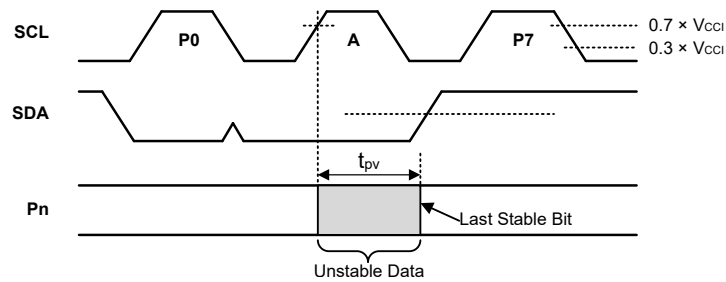


Figure 20. Definition of Write Mode Timing

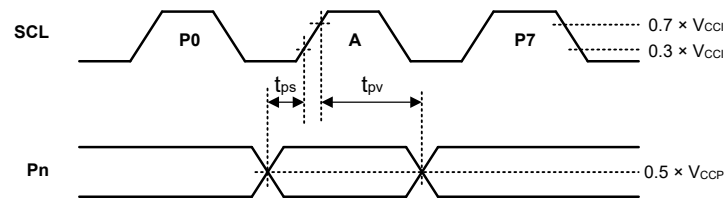


Figure 21. Definition of Read Mode Timing

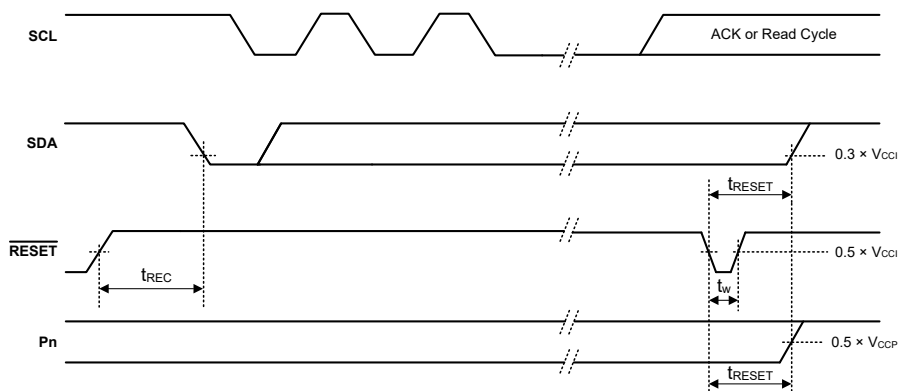


Figure 22. Definition of Reset Timing

Detailed Description

Overview

The TPT29508 is an 8-bit GPIO expander with interruption for I²C-bus applications. It operates from a supply voltage range of 1.65 V to 5.5 V on both the I²C-bus side (V_{CC1}) and the P-port side (V_{CCP}), which allows bidirectional voltage-level translation and GPIO expansion between 1.8-V, 2.5-V, 3.3-V, and 5-V I²C-bus and P-ports.

The TPT29508 features a set of 8-bit Configuration, Input, Output, and Polarity Inversion registers. The open-drain interrupt (\overline{INT}) output is changeable when any input state changes from its related register state. \overline{INT} can be connected to the interrupt input of a microcontroller. A power-on reset initializes all registers to their default values and resets the device state machine. The TPT29508 also has a hardware \overline{RESET} pin to reset the device to its default state.

All input/output pins do not have internal pull-up resistors, which helps reduce power consumption when communicating with external I/Os. One hardware pin (ADDR) selects the I²C-bus address and allows up to two devices to share the same I²C-bus.

Functional Block Diagram

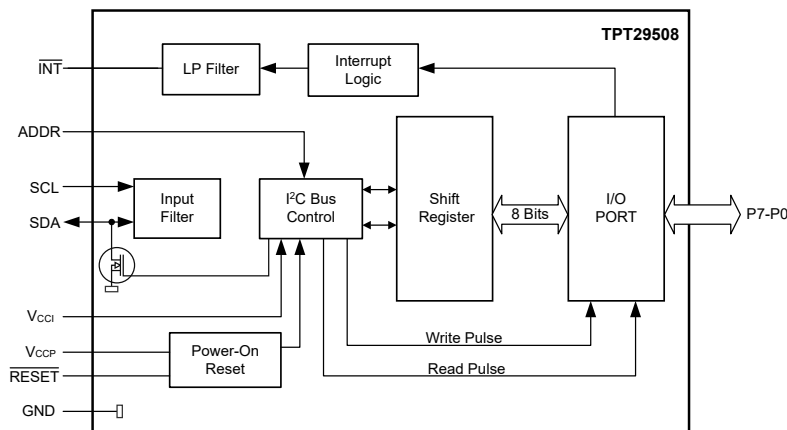


Figure 23. Functional Block Diagram

Feature Description

Voltage-level Translation

The TPT29508 allows bidirectional voltage-level translation and GPIO expansion between I²C-bus and P-ports.

Table 2. Voltage-level Translation

V_{CC1} (I ² C-bus)	V_{CCP} (P-port)
1.65 V to 5.5 V	1.65 V to 5.5 V

5-V Tolerant I/O Ports

The TPT29508 supports the I/O voltage from 1.8 V to 5 V and allows the TPT29508 to connect to kinds of devices with I/O communication. To minimize the current consumption, suggest the input signal should meet the V_{IH} and V_{IL} specs in the Electrical Characteristics table. Unused ports must not be left floating, and should be connected to V_{CCP} or GND via a resistor.

I²C to 8-bit GPIO Expander with Voltage-level Translation

Power-on Reset

When power (from 0 V) is connected to TPT29508 V_{CCP} , an internal Power-On Reset (POR) is in a reset condition until V_{CCP} has reached V_{POR} . At this point, the reset condition is released, and the TPT29508 registers and state machine are set up to their default states. After that, the V_{CCP} must be lowered V_{PORF} to reset the device and then back up to the operating voltage for a power-reset cycle.

Reset Input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ input can be asserted to initialize the system while keeping the V_{CCP} at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_w . The TPT29508 registers and state machine are changed to their default state once $\overline{\text{RESET}}$ is low. When $\overline{\text{RESET}}$ is high, the I/O levels at the P-port can be changed externally or through the controller. This input requires a pull-up resistor to V_{CCI} , if no active connection is used.

Interrupt Output ($\overline{\text{INT}}$)

In the input mode, an interrupt is generated by any rising or falling edge of the port inputs. After time t_{iv} , the output signal $\overline{\text{INT}}$ is valid. When data on the port is changed to the original setting, or data is read from the port that generated the interrupt, it resets the interrupt circuit. The reset operation should be in the read mode, and at the acknowledge (ACK) bit after the SCL rising edge. Note that the $\overline{\text{INT}}$ is reset at the ACK just before the byte of changed data is sent. Interrupts that occur during the ACK clock pulse can be lost since the resetting of the interrupt during this pulse. Each change of the I/O after resetting is detected and generates the $\overline{\text{INT}}$ output.

The pin configured as an output cannot trigger an interrupt. Changing an I/O from output to input may cause a false interrupt if the pin state does not match the setting of the Input Port register.

The $\overline{\text{INT}}$ output has an open-drain structure and requires a pull-up resistor to V_{CCP} or V_{CCI} , depending on the application. INT should be connected to the voltage source of the device that requires the interrupt information.

Register Map

Device Address

Following a START condition, the bus master must output the address of the slave it is accessing. The ADDR pin selects the I²C-bus address and allows up to two devices to share the same I²C bus. To conserve power, the ADDR pin must be pulled HIGH or LOW. The address of the TPT29508 is shown below.

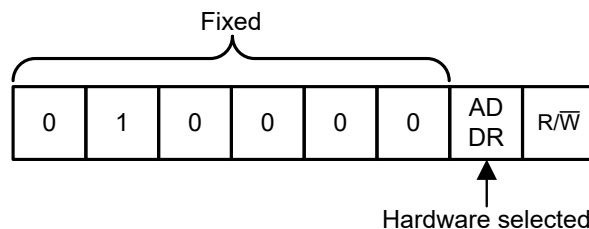


Figure 24. Slave Device Address

Control Register and Command Byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers is written or read.

I²C to 8-bit GPIO Expander with Voltage-level Translation
Table 3. Command Byte Description

Command Byte	Protocol	Register
0	Read byte	Input port
1	Read/write byte	Output port
2	Read/write byte	Polarity Inversion
3	Read/write byte	Configuration

Register 0: Input Port Registers

This register is an input-only port, which means the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 1, and writes to this register have no effect.

The default value 'X' is determined by the external logic level.

Table 4. Input Port Register

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Default	X	X	X	X	X	X	X	X

Register 1: Output Port Registers

This register configures the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. In fact, the value reading from this register is in the flip-flop controlling the output selection, not the actual pin value.

Table 5. Output Port Register

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	1	1	1	1	1	1	1	1

Register 2: Polarity Inversion Registers

This register allows the user to invert the polarity of the input port register data. If a bit in this register is set (written with '1'), the input port data polarity is inverted. If a bit in this register is cleared (written with '0'), the input port data polarity is retained.

Table 6. Polarity Inversion Register

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	0	0	0	0	0	0	0	0

Register 3: Configuration Registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with a high impedance. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. After a reset, the ports are defaulted to inputs.

I²C to 8-bit GPIO Expander with Voltage-level Translation**Table 7. Configuration Register**

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

Bus Transactions

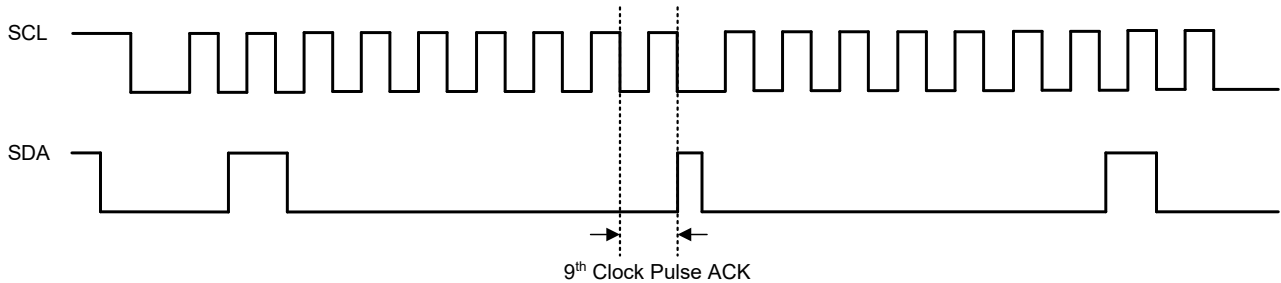


Figure 25. I²C BUS Waveform

Writing to the Port Registers

The data is transmitted to the TPT29508 by sending the device address with the least significant bit set to logic '0'. The command byte is sent after the address and determines which register will receive the subsequent data. There is no limitation on the number of data bytes sent in a single write transmission. The register address of the TPT29508 does not increment automatically.

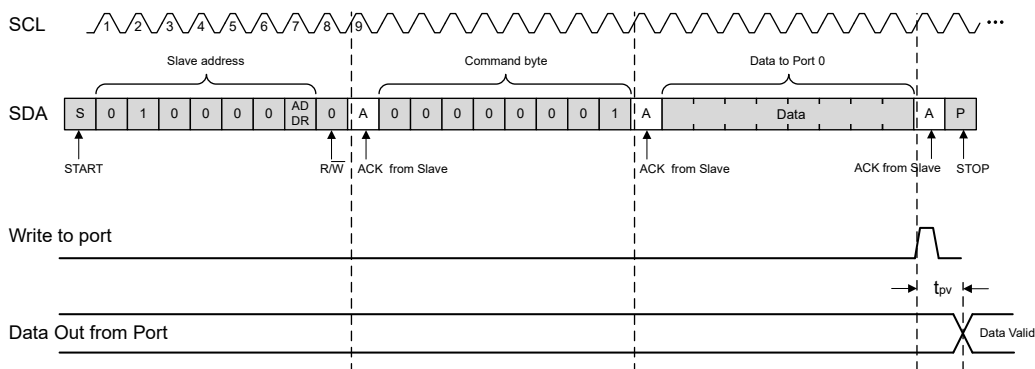


Figure 26. Write to Output Port Registers

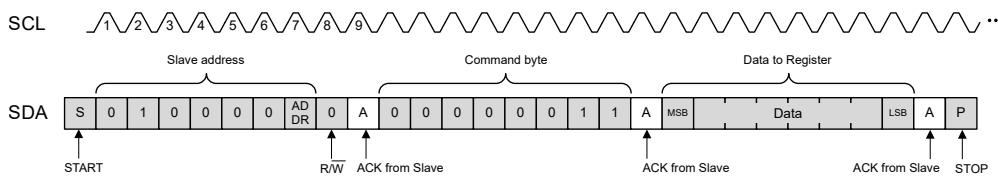


Figure 27. Write to Configuration Registers

Reading the Port Registers

Before reading data, the master device must first send the TPT29508 address with the least significant bit set to logic '0'. Then the command byte is sent following the address, determining which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to logic '1'. The TPT29508 will then send the data from the register defined by the command byte. Data is clocked into the register on the rising edge of the acknowledge clock pulse. There is no limitation on the number of data bytes received in a single read transmission. The register address of the

I²C to 8-bit GPIO Expander with Voltage-level Translation

TPT29508 does not increment automatically. For the last byte received, the master device must send a NACK, followed by sending a STOP condition.

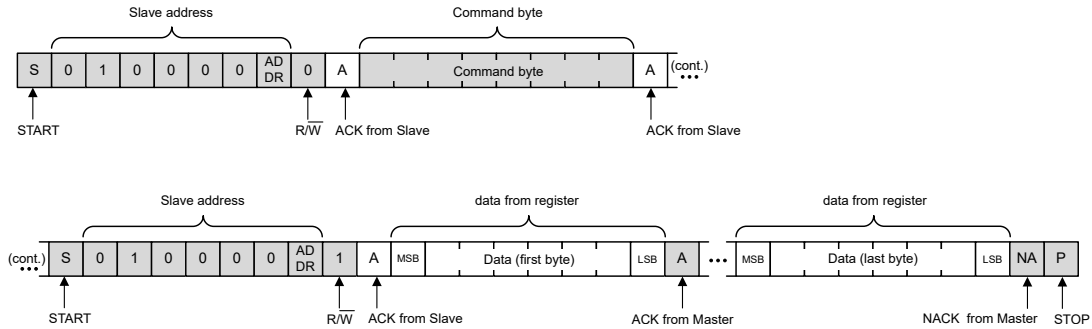


Figure 28. Read from Registers

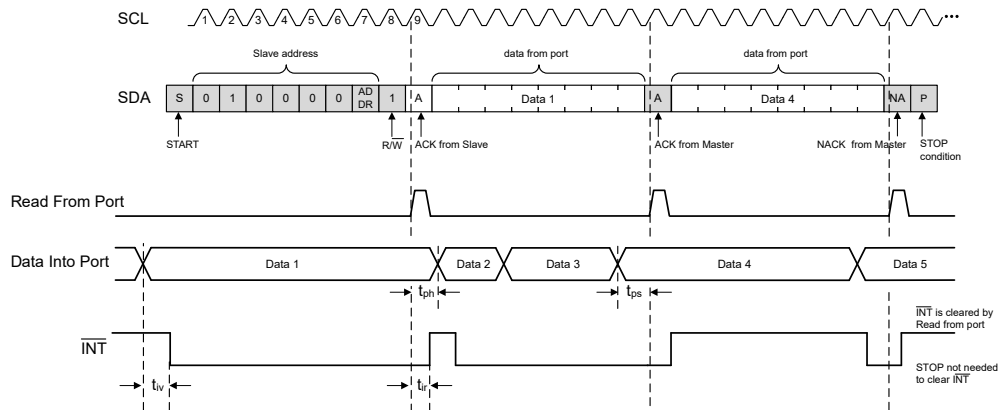


Figure 29. Read Input Port Register

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT29508 provides configurable I/O ports. Its interrupt ($\overline{\text{INT}}$) output can be connected to the interrupt input of a microcontroller, and can respond to any input state change. The TPT29508 allows bidirectional voltage-level translation and GPIO expansion between 1.8-V, 2.5-V, 3.3-V, and 5-V I²C-bus and P-ports.

Typical Application

The following figure shows an application in which the TPT29508 can be used to control multiple subsystems and read inputs from buttons.

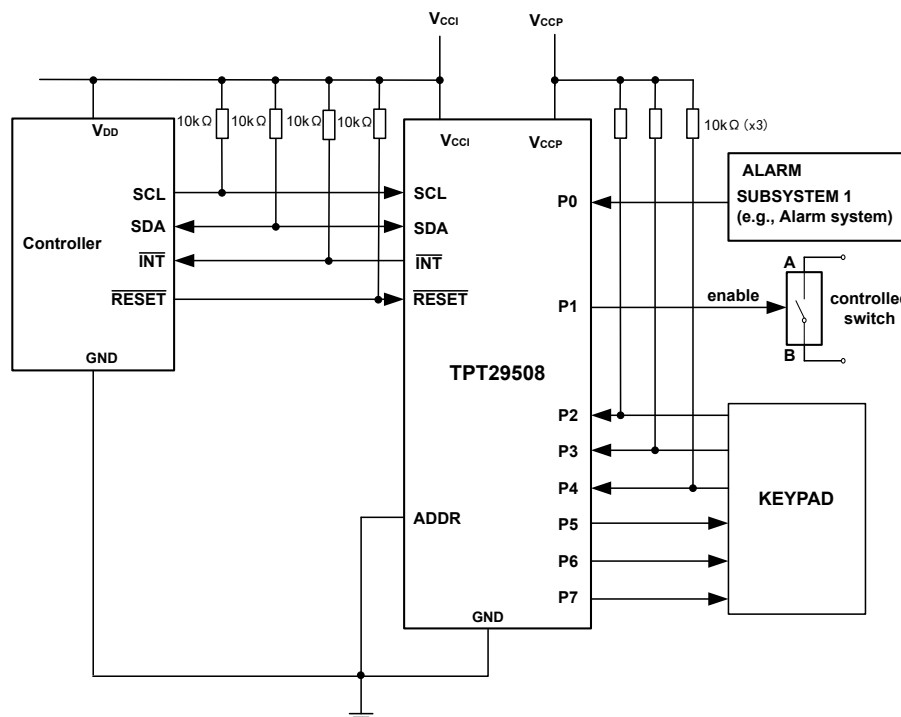


Figure 30. Typical Application Circuit

I²C-bus Pull-up Resistance

The SDA and SCL pull-up resistors are selected as follows.

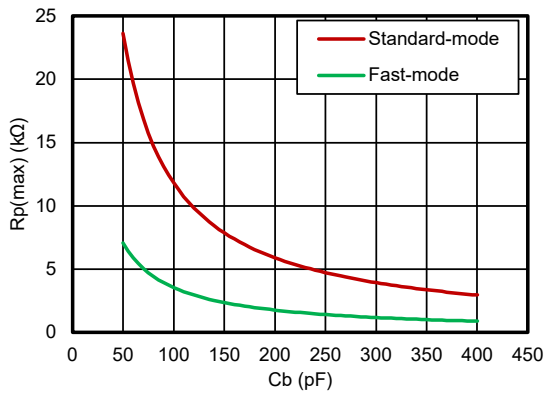
The minimum pull-up resistance is a function of V_{CC} , $V_{OL(max)}$, and I_{OL} .

I²C to 8-bit GPIO Expander with Voltage-level Translation

$$R_{p(\min)} = \frac{V_{CC} - V_{OL(\max)}}{I_{OL}} \tag{1}$$

The maximum pull-up resistance is a function of t_r and C_b . The parameter t_r is the maximum rise time of the I²C-bus, specified as 300 ns for Fast-mode and 1000 ns for Standard-mode. C_b is the total capacitance on the bus.

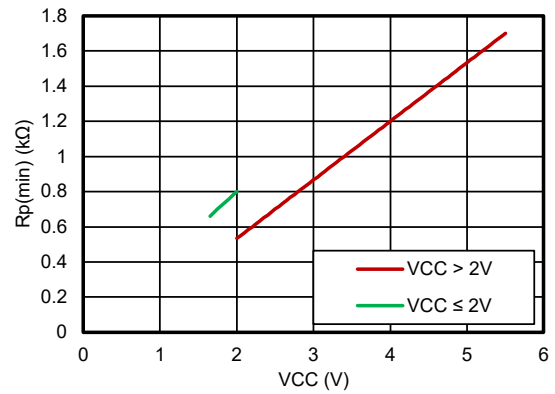
$$R_{p(\max)} = \frac{t_r}{0.8473 \times C_b} \tag{2}$$



Standard-mode ($f_{scl} = 100 \text{ kHz}$, $t_r = 1 \mu\text{s}$)

Fast-mode ($f_{scl} = 400 \text{ kHz}$, $t_r = 300 \text{ ns}$)

Figure 31. Maximum Pull-up Resistance ($R_{p(\max)}$) vs. Bus Capacitance (C_b)



$V_{OL} = 0.4 \text{ V}$, $I_{OL} = 3 \text{ mA}$ when $V_{CC} > 2 \text{ V}$

$V_{OL} = 0.2 \times V_{CC}$, $I_{OL} = 2 \text{ mA}$ when $V_{CC} \leq 2 \text{ V}$

Figure 32. Minimum Pull-up Resistance ($R_{p(\min)}$) vs. Pull-up Reference Voltage (V_{CC})

Layout

Layout Guideline

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance, and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they will have to turn corners. Figure 33 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

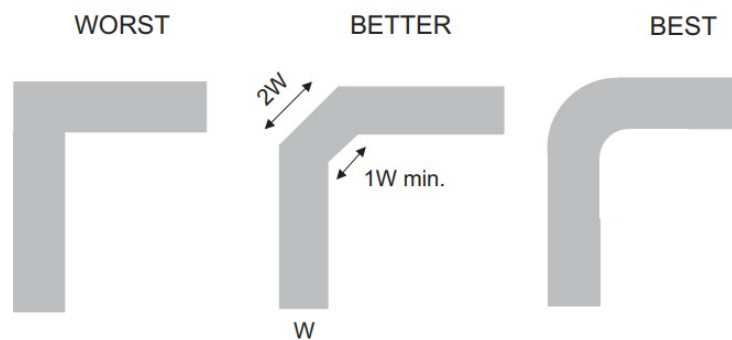


Figure 33. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Layout Example

Figure 34 illustrates an example of a PCB layout with the TPT29508. Some key considerations are as follows:

- Decouple the Supply (V_{CC1} and V_{CCP}) pin with a 0.1- μ F capacitor, and place it as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible and only make perpendicular crossings when necessary.

I²C to 8-bit GPIO Expander with Voltage-level Translation

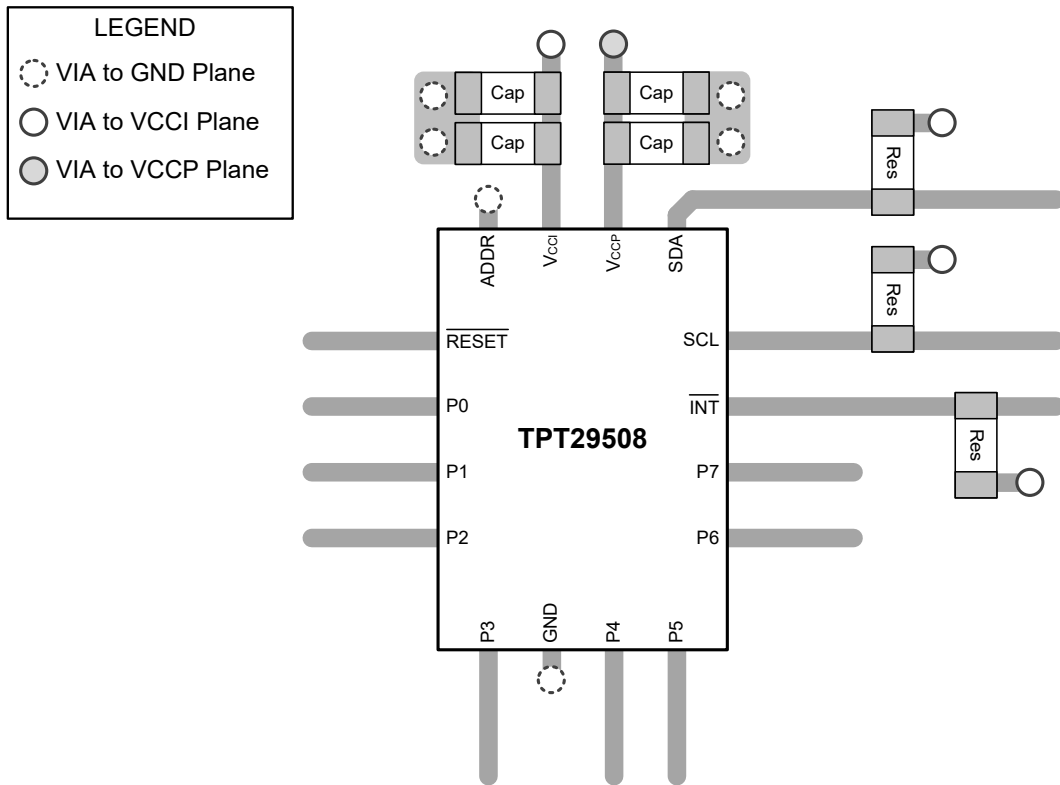
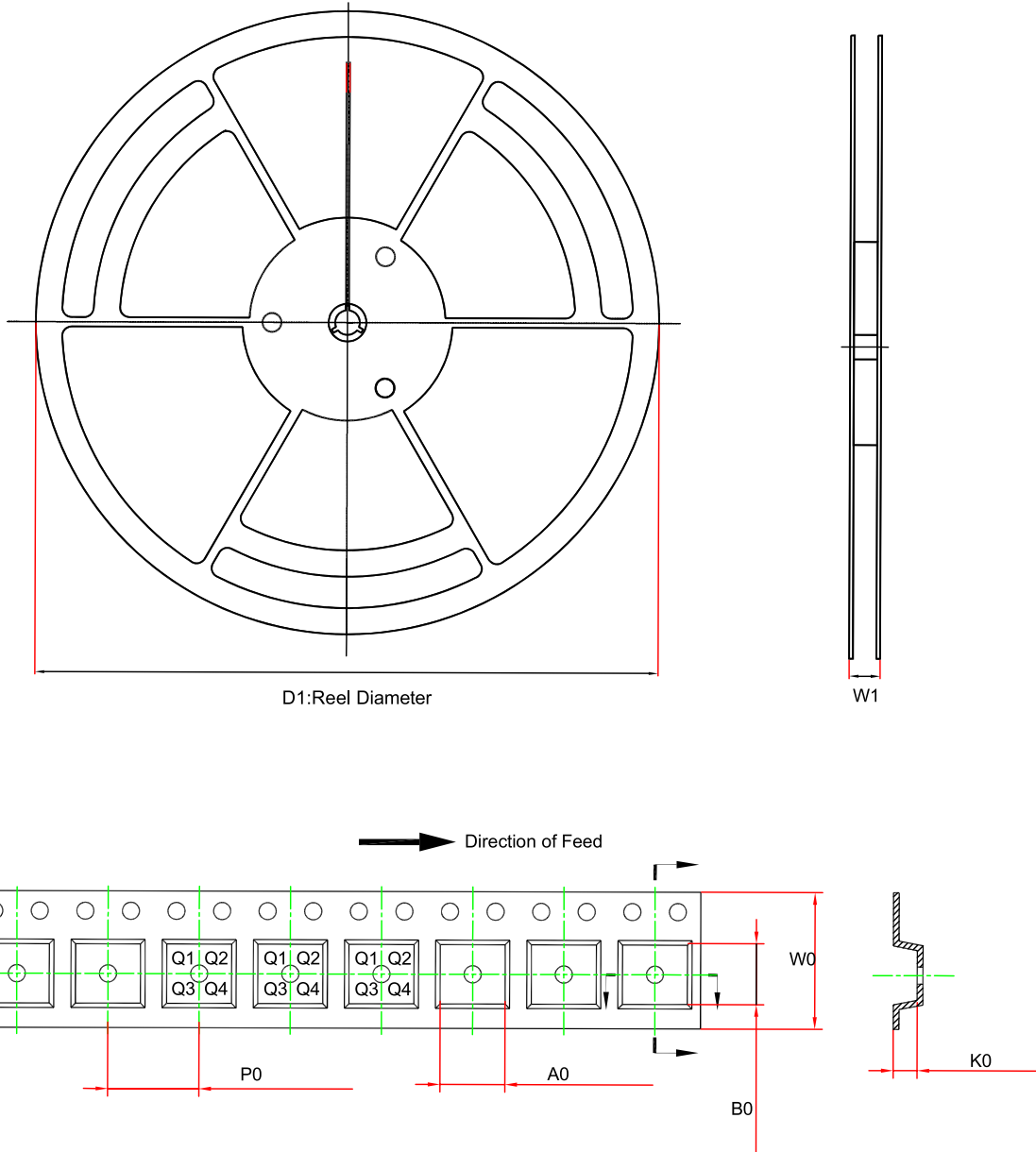


Figure 34. TPT29508 Layout Example

Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT29508-QN6R	QFN1.8X2.6-16	180	11.6	2	2.85	0.72	4	8	Q1

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29508-QN6R	-40 to 105°C	QFN1.8X2.6-16	508	MSL1	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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