

SD 3.0-SDR104 Compliant Memory Card Voltage-Level Translator

Features

- SD 3.0 Spec-Compliant Voltage Translation to Support SDR104 Mode
- Supports High Speed Clock, up to 208 MHz
- 1.2-V to 1.8-V Host Side Interface Voltage Support
- 100-mA Peak Current Regulator to Supply the Card-Side I/Os
- Low Power Consumption by Push-Pull Output Stage
- Automatic Enable and Disable Through V_{SD}
- Integrated Pull-up and Pull-down Resistors: No External Resistors Required
- Integrated EMI Filters Suppress Higher Harmonics of Digital I/Os
- Package: WLCSP20; Pitch 0.4 mm
- ESD Protection on Card Side
 - 8-kV IEC61000-4-2, Contact Mode
 - 15-kV IEC61000-4-2, Air-Discharge Mode

Description

The TPT24857 is an SD 3.0 spec-compliant memory card voltage-level translator with bidirectional control. It is designed to translate voltage between voltage 1.8 V to 3.0 V in the card side and 1.2 V to 1.8 V in the host side.

The device supports SD 3.0 SDR104 in high speed mode, and covers down to SDR50, DDR50, SDR25, SDR12 & SD 2.0 (50 MHz and 25 MHz) modes. The TPT24857 has an integrated voltage regulator to supply the card-side I/Os, and can support a 100-mA peak current with an auto-enable function. The device also has the EMI filters and support robust ESD protections: 10-kV IEC contact ESD.

The TPT24857 is available in WLCSP20 with the 0.4-mm pitch package, and is characterized from -40°C to +85°C.

Applications

- Smartphone
- Mobile Handset and Digital Camera
- Tablet PC/ Laptop
- SD, MMC or MicroSD Card Readers

Functional Block Diagram

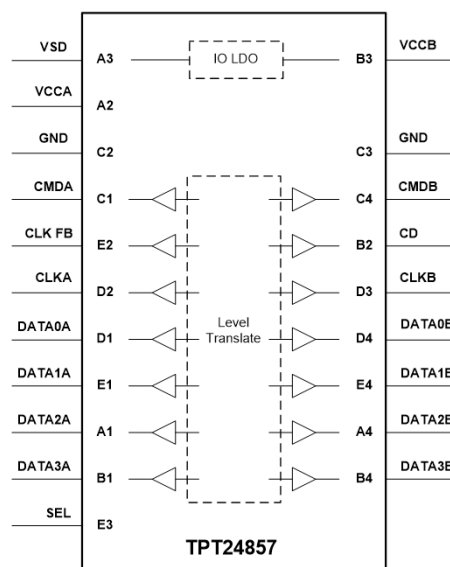


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SD 3.0-SDR104 Compliant Memory Card Voltage-Level Translator**Revision History**

Date	Revision	Notes
2020-01-02	Rev. Pre.0	Initial version.
2020-02-21	Rev. Pre.1	Updated the MSL level 1 and ICCA current.
2020-05-11	Rev. Pre.2	Updated the electrical parameter.
2020-06-24	Rev.A.0	Fixed the datasheet.
2020-09-11	Rev.A.1	Updated the host side and card side, and the min/max value of tr/tf.
2024-12-24	Rev.A.2	Updated to a new datasheet format. Updated the POD. Updated the Tape and Reel Information.

Pin Configuration and Functions

TPT24857-WS8R
WLCSP20

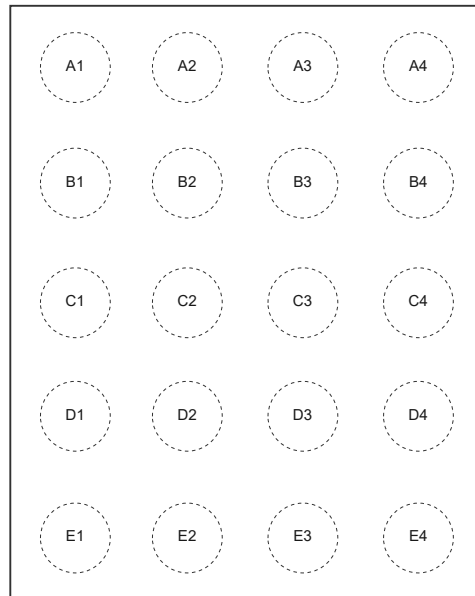


Table 1. Pin Functions

Pin No.	Name	I/O	Description
A1	DAT2A	I/O	Data 2 input or output on the host side.
A2	VCCA		Supply voltage from the host side.
A3	VSD		The supply voltage.
A4	DAT2B	I/O	Data 2 input or output on the memory card side.
B1	DAT3A	I/O	data 3 input or output on the host side.
B2	CD	O	Card detect switch biasing output.
B3	VCCB		Internal supply decoupling (VLDO).
B4	DAT3B	I/O	Data 3 input or output on the memory card side.
C1	CMDA	I/O	Command input or output on the host side.
C2	GND		Supply ground.
C3	GND		Supply ground.
C4	CMDB	I/O	Command input or output on the memory card side.
D1	DAT0A	I/O	Data 0 input or output on the host side.
D2	CLKA	I	Clock signal input on the host side.
D3	CLKB	O	Clock signal output on the memory card side.
D4	DAT0B	I/O	Data 0 input or output on the memory card side.

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Pin No.	Name	I/O	Description
E1	DAT1A	I/O	Data 1 input or output on the host side.
E2	CLK_FB	O	Clock feedback output on the host side.
E3	SEL	I	Card side I/O voltage level select.
E4	DAT1B	I/O	Data 1 input or output on the memory card side.

SD 3.0-SDR104 Compliant Memory Card Voltage-Level Translator**Specifications****Absolute Maximum Ratings**

Parameter		Min	Max	Unit
VCCA	Host Side Reference Voltage Range	-0.5	5.5	V
VSD, VCCB	Power Supply and Card Side Reference Bias Voltage Range	-0.5	5.5	V
V _I	Input Voltage Range ⁽²⁾	-0.5	5.5	V
P _{total}	Total Power Dissipation		1000	mW
	Peak Current in Card Side		100	mA
T _J	Maximum Operating Junction Temperature		85	°C
T _{STG}	Storage Temperature Range	-65	150	°C

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
IEC-ESD	IEC-61000-4-2, Contact Discharge	Side B Pin	8	kV
	IEC-61000-4-2, Air-Gap Discharge	Side B Pin	15	kV
HBM	HBM per ANSI/ESDA/JEDEC JS-001	All pins	7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1.5	kV
Latch Up	Latch up per JESD78	All Pin	600	mA

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V _{SD}	Supply Voltage	2.9		3.6	V
V _{CCA}	Host Side Voltage	1.1		2.0	V
V _I	Input Voltage in Host Side	-0.3		V _{CCA} + 0.3	V
	Input Voltage in Card Side	-0.3		V _{LDO} + 0.3	V
Cap	External Capacitance at Pin V _{CCB}		2.2		μF
	External Capacitance at Pin V _{SD}		0.1		μF
	External Capacitance at Pin V _{CCA}		0.1		μF
T _A	Operating Ambient Temperature	-40		85	°C

Integrated Resistors

All test conditions: T_A = 25°C.

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Table 2. Intergrated Resistors

Parameter		Min	Typ	Max	Unit
R _{pd}	VLDO Pull-Down Resistor to GND	70	100	130	Ω
	SEL Pull-Down Resistor to GND	210	350	550	kΩ
R _{pu}	Pull-up Resistor at Pins of Data-x and CMDx	20	33	40	kΩ
	Pull-up Resistor at CD Pin to V _{CCA}	70	100	130	kΩ
R _s	Series Resistor at Host Side, Tolerance ±30% ⁽¹⁾		22.5		Ω
	Series Resistor at Card Side, Tolerance ±30% ⁽¹⁾		15		Ω

(1) R_s is provided by design simulation.

Device Function Table

Table 3. SD Card Side Voltage Level Control Signal Truth Table

Input	Output		
SEL	V _{CCB}	Pins	Function
H	1.8 V	DAT0B to DAT3B, CLKB, CMDB	Low Supply Voltage Level (1.8 V _{typ})
L	Tracking V _{SD}	DAT0B to DAT3B, CLKB, CMDB	High Supply Voltage Level (Tracking V _{SD})

(1) H = HIGH; L = LOW; X = don't care.

(2) Host-side pins are not influenced by SEL.

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Electrical Characteristics

All test conditions: $V_{SD} = 3.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Automatic Enable Feature: V_{SD}						
V_{SDen}	Device Enable Voltage Level	$V_{CCA} \geq 1.0\text{ V}$, V_{SD} rising edge	2.25	2.45	2.65	V
$V_{SDdisable}$	Device Disable Voltage Level	$V_{CCA} \geq 1.0\text{ V}$, V_{SD} falling edge	2.2	2.4	2.6	V
ΔV_{SDen}	V_{SDen} Hysteresis Voltage		30		150	mV
Supply Voltage Regulator for Card-Side I/O PIN: V_{CCB}						
$V_{O(LDO)}$	Regulator/Switch Output Voltage	SEL = LOW; $3.0\text{ V} \leq V_{SD} \leq 3.6\text{ V}$; $I_O < 100\text{ mA}$	$V_{SD} - 0.2$	$V_{SD} - 0.1$	V_{SD}	V
		SEL = HIGH; $V_{SD} \geq 2.9\text{ V}$; $I_O < 100\text{ mA}$	1.7	1.8	1.95	V
$I_{O(LDO)}$	Regulator/Switch Output Current				100	mA
Host-Side Input Signals: CMDA and DAT0A to DAT3A, CLKA; $1.1\text{ V} \leq V_{CCA} \leq 2.0\text{ V}$						
V_{IH}	High-Level Input Voltage	$V_{CCA} = 1.1\text{ V}$ and $V_{CCA} = 2.0\text{ V}$	$0.75 \times V_{CCA}$		$V_{CCA} + 0.3$	V
V_{IL}	Low-Level Input Voltage	$V_{CCA} = 1.1\text{ V}$ and $V_{CCA} = 2.0\text{ V}$	-0.3		$0.25 \times V_{CCA}$	V
Host-Side Control Signals; $1.1\text{ V} \leq V_{CCA} \leq 2.0\text{ V}$						
SEL						
V_{IH}	High-Level Input Voltage	$V_{CCA} = 1.1\text{ V}$ and $V_{CCA} = 2.0\text{ V}$	$0.75 \times V_{CCA}$		$V_{CCA} + 0.3$	V
V_{IL}	Low-Level Input Voltage	$V_{CCA} = 1.1\text{ V}$ and $V_{CCA} = 2.0\text{ V}$	-0.3		$0.25 \times V_{CCA}$	V
Host-Side Output Signals: CLK_FB, CMDA and DAT0A to DAT3A; $1.1\text{ V} \leq V_{CCA} \leq 2.0\text{ V}$						
V_{OH}	High-Level Output Voltage	$I_O = 2\text{ mA}$; $V_I = V_{IH}$ (card side) for CLK_F	$0.8 \times V_{CCA}$			V
	High-Level Output Voltage	$I_O = 2\text{ }\mu\text{A}$; $V_I = V_{IH}$ (card side) for CMDA, DATxA	$0.8 \times V_{CCA}$			V
V_{OL}	Low-Level Output Voltage	$I_O = -2\text{ mA}$; $V_I = V_{IL}$ (card side)			$0.15 \times V_{CCA}$	V
Card-Side Input Signals: CMDB and DAT0B to DAT3B						
V_{IH}	High-Level Input Voltage	SEL = LOW (3.0 V card interface)	$0.625 \times V_{O(LDO)}$		$V_{O(LDO)} + 0.3$	V
		SEL = HIGH (1.8 V card interface)	$0.625 \times V_{O(LDO)}$		$V_{O(LDO)} + 0.3$	V
V_{IL}	Low-Level Input Voltage	SEL = LOW (3.0 V card interface)	-0.3		$0.3 \times V_{O(LDO)}$	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		SEL = HIGH (1.8 V card interface)	−0.3		0.35 × V _{O (LDO)}	V
Card-Side Output Signal						
CMDB and DAT3B, CLKB						
V _{OH}	High-Level Output Voltage for CLKB only	I _O = 4 mA; V _I = V _{IH} (host side); SEL = LOW (3.0 V card interface)	0.85 × V _{O (LDO)}		V _{O (LDO)} +0.3	V
		I _O = 2 mA; V _I = V _{IH} (host side); SEL = HIGH (1.8 V card interface)	0.85 × V _{O (LDO)}		2.0	V
	High-Level Output Voltage for CMDB, DATxB	I _O = 2 μA; V _I = V _{IH} (host side); SEL = HIGH (1.8 V card interface)	0.85 × V _{O (LDO)}		2.0	V
V _{OL}	Low-Level Output Voltage	I _O = −4 mA; V _I = V _{IL} (host side); SEL = LOW (2.9 V card interface)	−0.3		0.125 × V _{O(LDO)}	V
		I _O = −2 mA; V _I = V _{I card L} (host side); SEL = HIGH (1.8 V interface)	−0.3		0.125 × V _{O (LDO)}	V
Bus Signal Equivalent Capacitance ⁽¹⁾						
C _{ch}	Channel Capacitance	V _I = 0 V; f _i = 1 MHz; V _{SD} = 3.0 V; V _{CCA} = 1.8 V				
		host side		7		pF
		card side		15		pF
Current Consumption						
I _{CC (stat)}	Static Supply Current	V _{SD} ≥ V _{SDen} (active mode); all inputs = HIGH				
		SEL = LOW (3.0 V card interface)		72	110	uA
		SEL = HIGH (1.8 V card interface)		76	115	uA
I _{CC (stb)}	Standby Supply Current	V _{SD} ≤ V _{SDen} and V _{CCA} ≤ 1.0 V (inactive mode); all host side inputs = HIGH				
		SEL = LOW (3.0 V card interface)		6	14	uA
		SEL = HIGH (1.8 V card interface)		6	14	uA

(1) EMI filter line capacitance per data channel from I/O driver to pin; C_{CH} is provided by design simulation.

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Switching Characteristics AC Performance

Table 4. Voltage Regulator, Typical Test Condition is $V_{SD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage Regulator Output Pin: V_{CCB}						
t_{startup} (LDO)	Regulator Start-up Time	$V_{CCA} = 1.8\text{ V}$; $V_{SD} = 3.0\text{ V}$; $C_{\text{ext}} = 2.2\text{ }\mu\text{F}$; see Figure			400	μs
$t_{f(o)}$	Output Fall Time	$V_{O(LDO)} = 3.0\text{ V}$ to 1.8 V ; $\text{SEL} = \text{LOW}$ to HIGH ; see Figure			1	ms
$t_{r(o)}$	Output Rise Time	$V_{O(LDO)} = 1.8\text{ V}$ to 3.0 V ; $\text{SEL} = \text{HIGH}$ to LOW ; see Figure			100	μs

Table 5. Level Translator, Typical Test Condition is $V_{SD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Host Side Transition Times						
t _r	Rise Time	SEL = HIGH (1.8 V card interface); V _{CCA} = 1.8 V		0.4	-- (1)	ns
t _f	Fall Time			0.4	-- (1)	ns
t _r	Rise Time	SEL = HIGH (1.8 V card interface); V _{CCA} = 1.2 V		0.4	-- (1)	ns
t _f	Fall Time			0.4	-- (1)	ns
Card Side Transition Times						
t _r	Rise Time	SEL = HIGH (1.8 V card interface)	-- (2)	0.75	-- (2)	ns
t _f	Fall Time		-- (2)	0.75	-- (2)	ns
Card Input Transition Times						
t _r	Rise Time	SEL = HIGH (1.8 V card interface) (1)	-- (3)	0.5	-- (3)	ns
t _f	Fall Time			0.45	-- (3)	ns
Host to Card Propoagation Delay						
t _{pd1}	Propagation Delay, DATxA to DATxB, CMDA to CMDB, CLKA to CLKB	SEL = HIGH (1.8 V card interface); V _{CCA} = 1.2 V		3.75	-- (4)	ns
t _{pd2}	Propagation Delay, CLKA to CLK_FB	SEL = HIGH (1.8 V card interface); V _{CCA} = 1.2 V		6.5	-- (4)	ns
Card to Host Propagation Delay						
t _{pd3}	Propagation Delay, DATxB to DATxA, CMDB to CMDA	SEL = HIGH (1.8 V card interface); V _{CCA} = 1.2 V		3.5	-- (4)	ns
Automatic Direction						
t _{dst}	Auto Direction Swapping Time of Data Flow Between from Host to Card and from Card to Host	SEL = HIGH (1.8 V card interface); V _{CCA} = 1.2 V		5	-- (5)	ns

(1) Transition between $V_{OL} = 0.35B \times V_{CCA}$ and $V_{OH} = 0.65 \times V_{CCA}$, $t_{rmax} = 1\text{ ns}$; $t_{fmax} = 1\text{ ns}$ in lab test;

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- (2) Transition between $V_{OL} = 0.45\text{ V}$ and $V_{OH} = 1.4\text{ V}$, $t_{rmin} = 0.4\text{ ns}$; $t_{fmin} = 0.4\text{ ns}$; $t_{rmax} = 1.32\text{ ns}$; $t_{fmax} = 1.32\text{ ns}$ in lab test;
- (3) By design simulation, transition between $V_{IL} = 0.58\text{ V}$ and $V_{IH} = 1.27\text{ V}$ with $C_{trace} = 3.5\text{ pF}$ and $C_{card+CRADLE} = 12\text{ pF}$, trace length = 11 mm; $t_{rmin} = 0.2\text{ ns}$, $t_{rmax} = 0.96\text{ ns}$; $t_{fmax} = 0.96\text{ ns}$ by design simulation;
- (4) Parameters are provided by the lab bench test, $t_{pd1max} = 6.5\text{ ns}$ in lab test, $t_{pd2max} = 15\text{ ns}$ in lab test, $t_{pd3max} = 6.0\text{ ns}$ in lab test;
- (5) By design simulation, $t_{dstmax} = 9.6\text{ ns}$.

Detailed Description

Functional Block Diagram

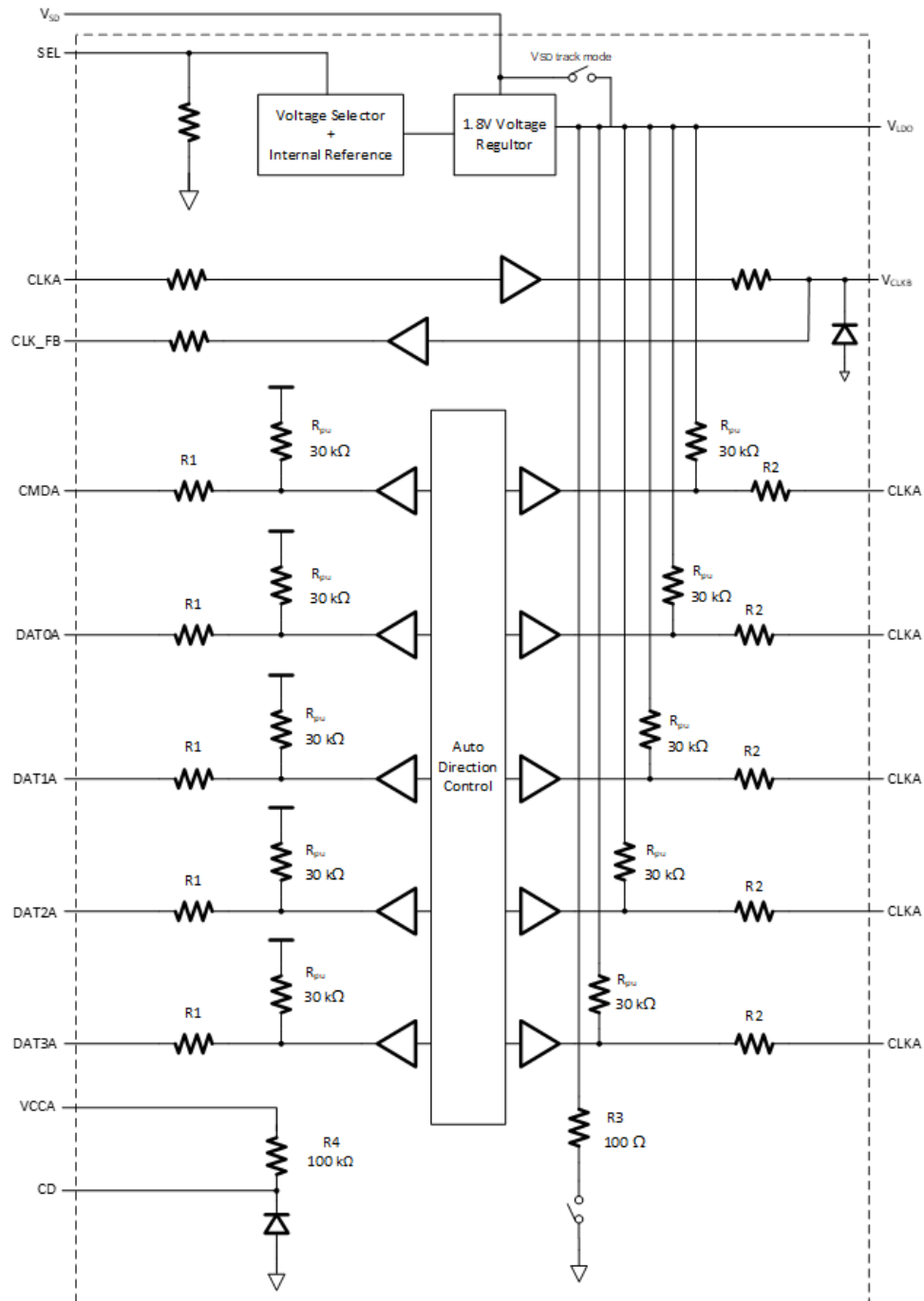


Figure 1. Functional Block Diagram

SD 3.0-SDR104 Compliant Memory Card Voltage-Level Translator

Feature Description

Enable and Direction Control

The TPT24857 has an auto-enable feature. When V_{SD} rises above 2.65 V, the LDO and the level translator logic is enabled automatically. As soon as V_{SD} drops below the $V_{SDdisable}$, the LDO and the card side drivers and the level translator logic is disabled. All host side pins excluding CLKA are configured as inputs with a 30-k Ω resistor pulled up to V_{CCA} , refer to [Table 2](#).

Integrated Voltage Regulator

The low dropout voltage regulator delivers the supply voltage for the voltage translators and the card-side input/output stages. It can support 1.8 V and 3.0 V signaling modes as required in the SD 3.0 specification. The switching time between the two output voltage modes is compliant with the SD 3.0 specification. Depending on the signaling level at the pin SEL, the regulator delivers 1.8 V (SEL = HIGH) or 3.0 V (SEL = LOW). See [Table 3](#) for the SD card side voltage level control signal truth table.

There is an external capacitor between the regulator output pin V_{CCB} and ground for proper operation of the integrated voltage regulator. See [Table 2](#) for equivalent series resistance, and recommended capacitance in [Recommended Operating Conditions](#). It is recommended to place the capacitor close to the V_{SD} and V_{CCB} pin and also maintain short connections of both to the ground.

Feedback Clock Channel

The clock is transmitted from the host side to the SD card side, and the voltage translator and the PCB traces have some delay. It reduces timing margin for data read back from SD card, especially at higher data rate. In real case, the clock is always delivered by the host, while the data in the timing critical read mode comes from the card, so there is a feedback path provided to compensate the delay. That's why a feedback clock channel is needed here.

EMI Filter

In the sensitive mobile application, the high speed communication is very complicated, then all input/output driver stages must be designed with EMI filters to reduce interferences.

ESD Protection

The TPT24857 has robust ESD protections on all SD card pins as well as on the VSD pin. The architecture prevents any stress for the host: the voltage translator discharges any stress through the supply ground.

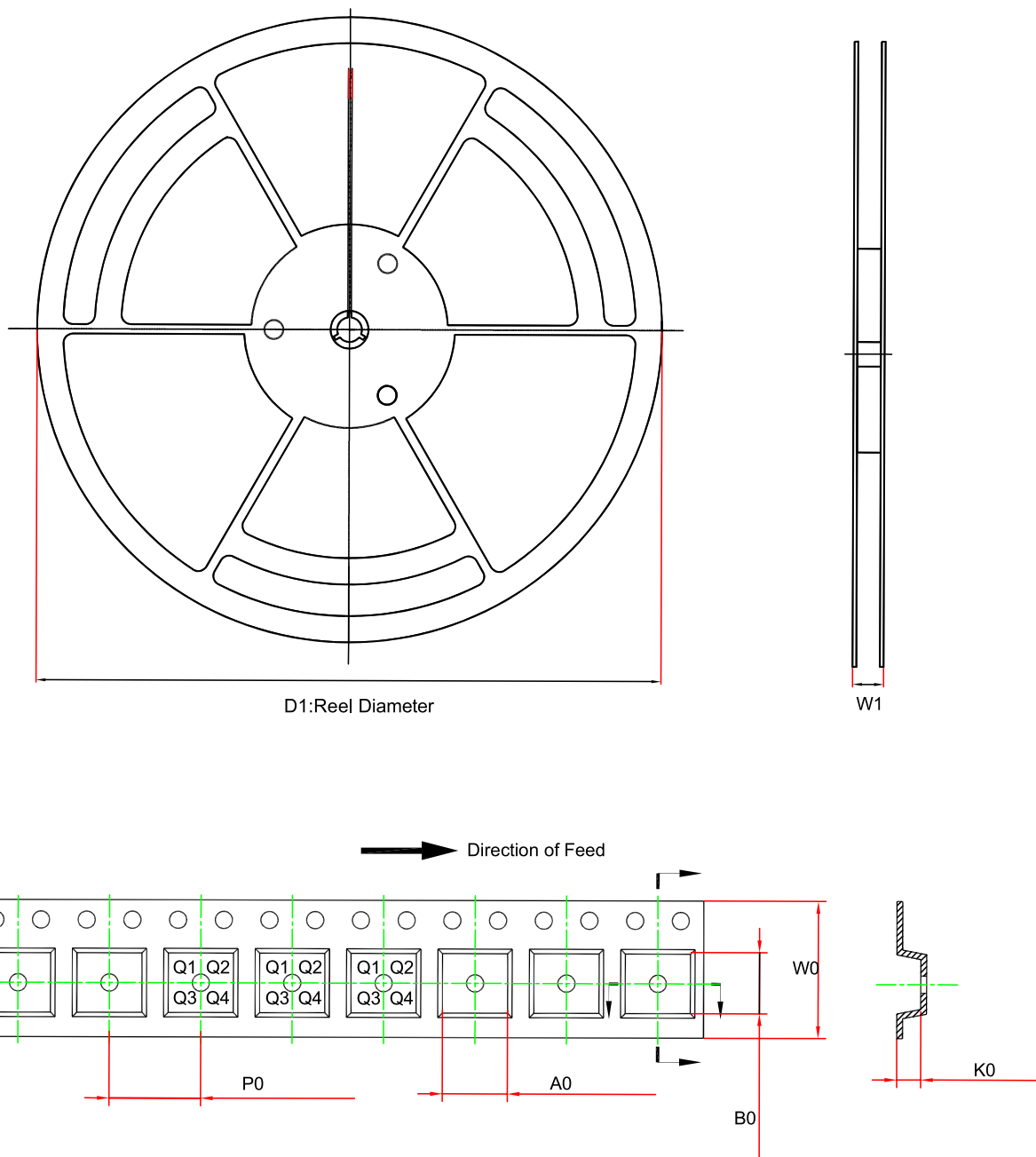
The pin Card Detection (CD) might be pulled down by the SD card which has to be detected by the host. The pin is designed with International Electrotechnical Commission (IEC) system-level ESD protection and pull-up resistor connected to the host supply V_{CCA} .

SD 3.0-SDR104 Compliant Memory Card Voltage-Level Translator**Application and Implementation****Note**

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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Tape and Reel Information



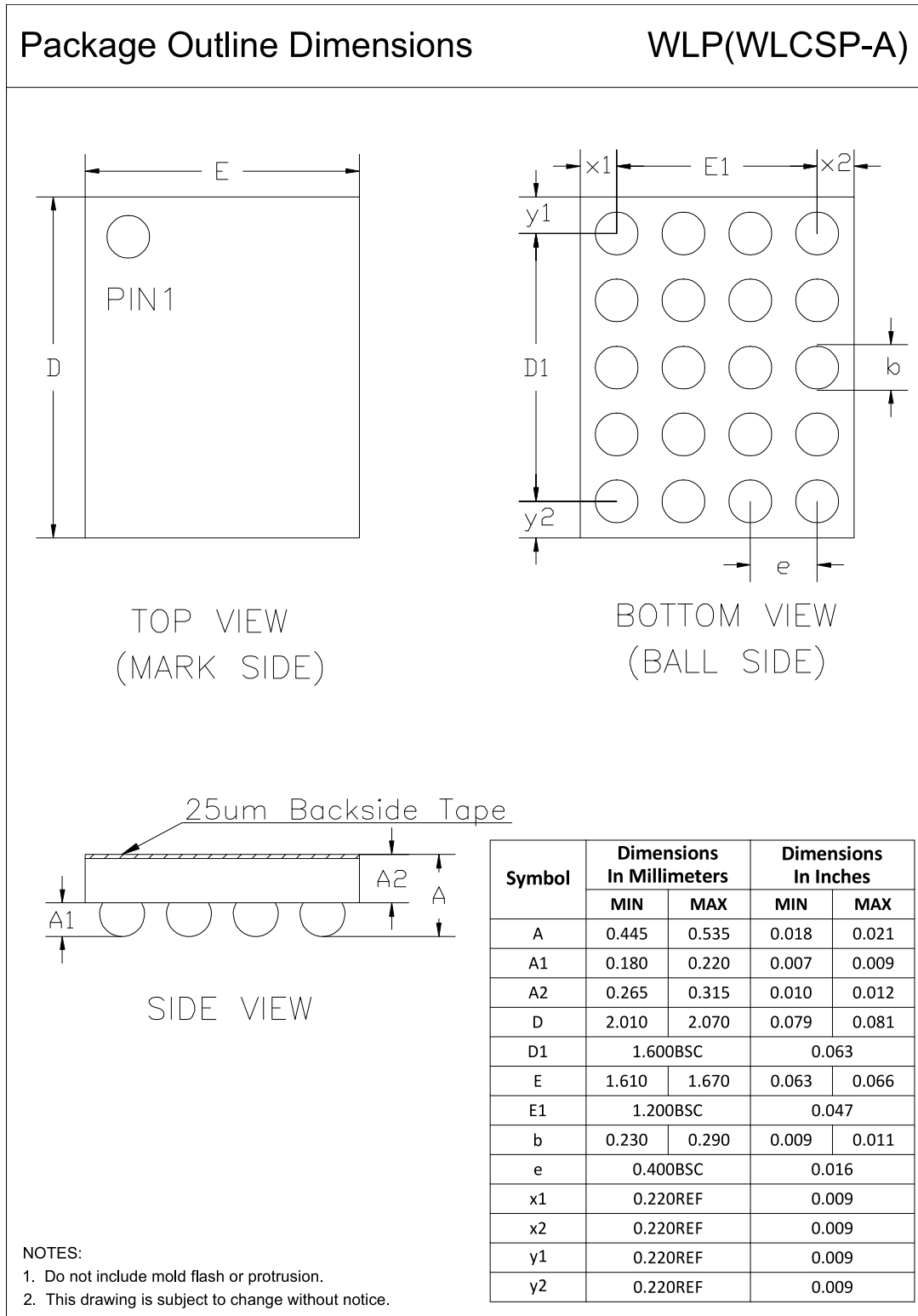
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) ⁽¹⁾	B0 (mm) ⁽¹⁾	K0 (mm) ⁽¹⁾	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT24857-WS8R-S	WLCSP20	178	12.5	1.75	2.30	0.75	4	8	Q1

(1) The value is for reference only. Contact the 3PEAK factory for more information.

SD 3.0-SDR104 Compliant Memory Card Voltage-Level Translator

Package Outline Dimensions

WLCSP



SD 3.0-SDR104 Compliant Memory Card Voltage-Level Translator**Order Information**

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT24857-WS8R-S	-40 to 85°C	WLCSP20	T27	1	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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