4-bit Bidirectional Level Shifter, Push-Pull Mode

Features

- 4-bit Bidirectional Level Shift, Push-Pull Output
- Max Data Rate (Push-Pull):
  - 100 Mbps at V_{CCA} = 3.3 V and V_{CCB} = 5 V
- Voltage-Level Translation between:
  - V_{CCA} Range: 1.65 V to 3.6 V
  - V_{CCB} Range: 1.65 V to 5.5 V
- 5-V Tolerant OE Enable Pin
- High-impedance A1~4 and B1~4 pins for OE = LOW
- VCC Isolation Feature: Either VCC Input = GND, All Outputs in the High-Impedance State
- I_{OFF} Supports Partial Power-down Mode
- No Power Up Sequence Required for V_{CCA} and V_{CCB}
- ESD Protection:
  - A Port ±4000-V Human-Body Model
  - B Port ±8000-V Human-Body Model
  - B Port ±4000-V IEC 61000-4-2 Contact Discharge
  - 1500-V Charged-Device Model

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Description

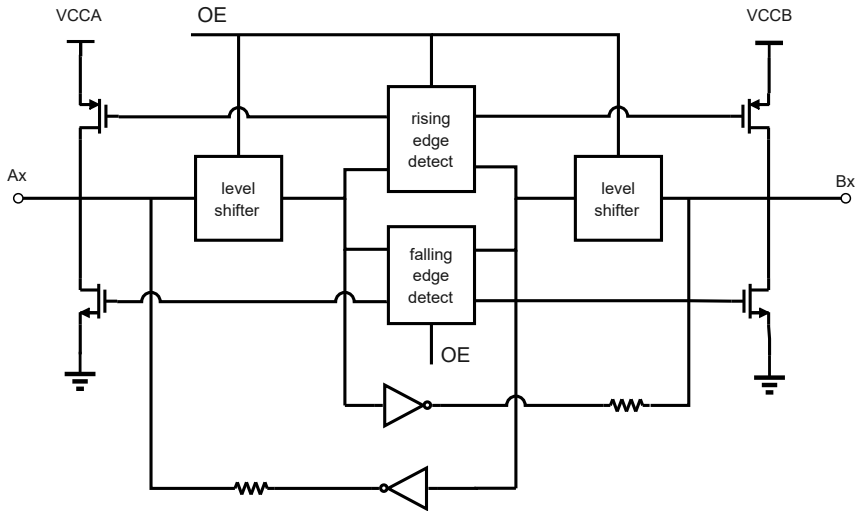
The TPT20204 device is a 4-bit level shifter, and only supports Push-Pull mode, which functions with an enable (OE) input and can work within the V_{CCA} range from 1.65 V to 3.6 V and the V_{CCB} range from 1.65 V to 5.5 V. V_{CCA} must be less than or equal to V_{CCB}. TPT20204 supports bidirectional voltage translation among 1.8 V, 2.5 V, 3.3 V, and 5 V.

The A1~4 I/Os are connected to the B1~4 I/Os, which allows bidirectional data flowing between ports. If OE is low, the translator switch is off, and a high-impedance state exists between port A and port B to isolate both sides. The OE input circuit is internally connected to V_{CCA}.

The 4-bit bidirectional buffer isolates capacitance and allows 15 pF on either side of the device to support 100-Mbps speed in Push-Pull mode in 3.3 V V_{CCA} and 5 V V_{CCB} supply.

The TPT20204 is available in the QFN1.7x2.0-12 package and is characterized from −40°C to +125°C.

Functional Block Diagram



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Revision History

Date	Revision	Notes
2024-12-24	Rev.A.0	Released version

Pin Configuration and Functions

TPT20204-QN5R
QFN1.7x2-12 Package
Top View

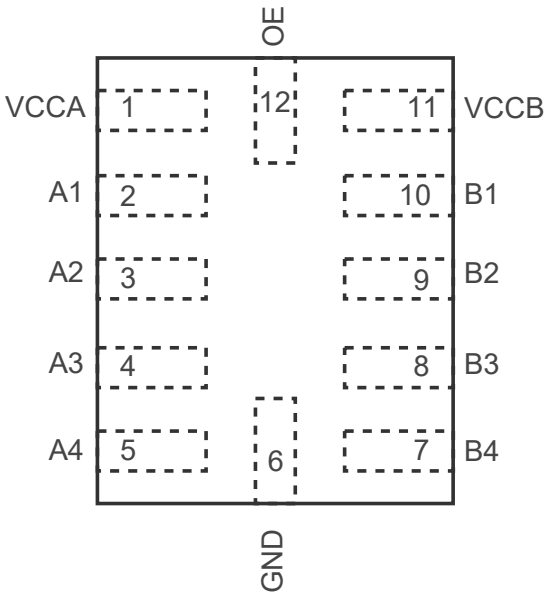


Table 1. Pin Functions: TPT20204

Pin		I/O	Description
No.	Name		
1	VCCA	I	side-A supply voltage
2	A1	I/O	Input/output A1. Referenced to V_{CCA}
3	A2	I/O	Input/output A2. Referenced to V_{CCA}
4	A3	I/O	Input/output A3. Referenced to V_{CCA}
5	A4	I/O	Input/output A4. Referenced to V_{CCA}
6	GND	I	Supply ground
7	B4	I/O	Input/output B4. Referenced to V_{CCB}
8	B3	I/O	Input/output B3. Referenced to V_{CCB}
9	B2	I/O	Input/output B2. Referenced to V_{CCB}
10	B1	I/O	Input/output B1. Referenced to V_{CCB}
11	VCCB	I	side-B supply voltage
12	OE	I	Active-high enable input, Reference to V_{CCA}

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CCA}	DC Reference Voltage Range (side-A)	−0.5	4.6	V
V_{CCB}	DC Reference Bias Voltage Range (side-B)	−0.5	6.5	V
V_I	Input Voltage Range, side-A	−0.5	4.6	V
	Input Voltage Range, side-B	−0.5	6.5	V
V_O	Voltage Range Applied to Any Output in the High-impedance or Power-off State, V_O, side-A	−0.5	4.6	V
	Voltage Range Applied to Any Output in the High-impedance or Power-off State, V_O, side-B	−0.5	6.5	V
	Voltage Range Applied to Any Output in the High or Low State, V_O, side-A	−0.5	V_{CCA} + 0.5	V
	Voltage Range Applied to Any Output in the High or Low State, V_O, side-A	−0.5	V_{CCB} + 0.5	V
I_{IK}	Input Clamp Current, V_I < 0		−50	mA
I_{OK}	Output Clamp Current, $V_{I/O}$ < 0		−50	mA
I_O	Continuous Output Current	−50	50	mA
I_C	Continuous Current through Each V_{CCA}, V_{CCB}, or GND	−100	100	mA
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD, side-A ports	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
	Human Body Model ESD, side-B ports	ANSI/ESDA/JEDEC JS-001 (1)	±8	kV
IEC ESD	IEC Contact Discharge	IEC-61000-4-2, Bus Pin: B ports	±4	kV
	IEC Air-Gap Discharge	IEC-61000-4-2, Bus Pin: B ports	±8	kV
CDM	Charged Device Model ESD, side-A and side-B ports	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV
LU	Latch up	LU, per JESD78, All Pin (3)	±500	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Test at the temperature of 25℃.

Recommended Operating Conditions

Parameter		V_{CCA}	V_{CCB}	Min	Max	Unit
V_{CCA}	Reference Voltage, side-A			1.65	3.6	V
V_{CCB}	Reference Voltage, side-B			1.65	5.5	V
V_{IH}	Side-A Ports High-level Input Voltage	1.65 V to 1.95 V	1.65 V to 5.5 V	V_{CCI} (1) x 0.65	V_{CCI} (1)	V
	Side-B Ports High-level Input Voltage	1.65 V to 3.6 V	1.65 V to 5.5 V	V_{CCI} (1) x 0.65	V_{CCI} (1)	V
	OE Inputs High-level Input Voltage	1.65 V to 3.6 V	1.65 V to 5.5 V	V_{CCA} x 0.65	5.5	V
V_{IL}	Side-A Ports Low-level Input Voltage	1.65 V to 3.6 V	1.65 V to 5.5 V	0	V_{CCI} (1) x 0.35	V
	Side-B Ports Low-level Input Voltage	1.65 V to 3.6 V	1.65 V to 5.5 V	0	V_{CCI} (1) x 0.35	V
	OE Inputs Low-level Input Voltage	1.65 V to 3.6 V	1.65 V to 5.5 V	0	V_{CCA} x 0.35	V
Δt/Δv	Side-A Ports Input Transition Rise or Fall Rate	1.65 V to 3.6 V	1.65 V to 5.5 V		40	ns/V
	Side-B Ports Input Transition Rise or Fall Rate	1.65 V to 3.6 V	1.65 V to 5.5 V		40	
	OE Input Transition Rise or Fall Rate	1.65 V to 3.6 V	1.65 V to 5.5 V		40	
T_A	Operating Ambient Temperature			−40	125	°C

(1) V_{CCI} is the supply voltage of the input side-A or side-B port.
(2) V_{CCO} is the supply voltage of the output side-A or side-B port.
(3) V_{CCA} should be less than or equal to V_{CCB}, and V_{CCA} must not be higher than 3.6 V.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
QFN1.7x2-12	171	80	°C/W

Electrical Characteristics

All test conditions: V_{CCA} = 1.65 V to 3.6 V, V_{CCB} = 1.65 V to 5.5 V, GND = 0 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Conditions	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
Supply Voltage and Current								
V_{OHA}	Port A High-level Output Voltage	I_{OH} = –20 μA, V_{IB} ≥ V_{CCB} – 0.4 V	1.65 V to 3.6 V	1.65 V to 5.5 V	V_{CCA} − 0.4			V
V_{OLA}	Port A Low-level Output Voltage	I_{OL} = 20μA, V_{IB} ≤ 0.15 V	1.65 V to 3.6 V	1.65 V to 5.5 V			0.4	V
V_{OHB}	Port B High-level Output Voltage	I_{OH} = –20 μA, V_{IA}≥ V_{CCA} – 0.2 V	1.65 V to 3.6 V	1.65 V to 5.5 V	V_{CCB} − 0.4			V
V_{OLB}	Port B Low-level Output Voltage	I_{OL} = 20 μA, V_{IA} ≤ 0.15 V	1.65 V to 3.6 V	1.65 V			0.4	V
I_I	Input Leakage Current	OE: V_I = V_{CCI} or GND	1.65 V	1.65 V to 5.5 V	−2		2	μA
I_{OZ}	High Impedance State Output Current	Port A or B, OE = GND	1.65 V	1.65 V to 5.5 V	−2		2	μA
I_{CCA}	Quiescent Supply Current for V_{CCA}	V_I = V_{CCI} or GND, I_O=0, OE = V_{CCA}	1.65 V to 3.6 V	1.65 V to 5.5 V			5	μA
			3.6 V	0			5	
			0	5.5 V	−1		1	
I_{CCB}	Quiescent Supply Current for V_{CCB}	V_I = V_{CCI} or GND, I_O = 0, OE = V_{CCA}	1.65 V to 3.6 V	1.65 V to 5.5 V			15	μA
			3.6 V	0	−1		1	
			0	5.5 V			10	
I_{CCA}+ I_{CCB}	Combined Supply Current	V_I = V_{CCI} or GND, I_O = 0, OE = V_{CCA}	1.65 V to 3.6 V	1.65 V to 5.5 V			15	μA
I_{OFF}	OFF Current	A port: VI or Vo =0 to 3.6	0	1.65 V to 5.5 V	−5		5	μA
		B port: VI or Vo =0 to 3.6	1.65 V to 3.6 V	0	−5		5	μA
I_{CCZA}	High Impedance State V_{CCA} Supply Current	V_I= V_{CCI} or GND, I_O = 0, OE = GND	1.65 V to 3.6 V	1.65 V to 5.5 V			5	μA
I_{CCZB}	High Impedance State V_{CCB} Supply Current	V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.65 V to 3.6 V	1.65 V to 5.5 V			15	μA
C_I	Input Capacitance (1)	OE	3.3 V	3.3 V		5	10	pF
C_{IO}	Input/Output Capacitance (1)	Port A	3.3 V	3.3 V		7	10	pF
		Port B	3.3 V	3.3 V		10	15	pF

(1) Test data based on bench tests and design simulation; NOT test in production.

AC Timing Requirements — VCCA = 1.8 V

All test conditions: V_{CCA} = 1.65 V to 1.95 V, GND = 0 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
f_D (1)	Data Rate	Push-pull mode	1.65 V to 1.95 V			35	Mbps
			2.3 V to 2.7 V			50	Mbps
			3.0 V to 3.6 V			60	Mbps
			4.5 V to 5.5 V			60	Mbps
t_W (1)	Pulse Duration	Push-pull mode	1.65 V to 1.95 V	28.6			ns
			2.3 V to 2.7 V	20			ns
			3.0 V to 3.6 V	16.7			ns
			4.5 V to 5.5 V	16.7			ns
t_{PHL} (1)	Propagation Delay (High-to-Low)	A-to-B, or B-to-A, push-pull driving	1.65 V to 1.95 V (1)			20	ns
			2.3 V to 2.7 V (1)			20	ns
			3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V (1)			15	ns
t_{PLH} (1)	Propagation Delay (Low-to-High)	A-to-B, or B-to-A, push-pull driving	1.65 V to 1.95 V (1)			20	ns
			2.3 V to 2.7 V (1)			20	ns
			3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V (1)			15	ns
t_{en} (1)	Enable Time	OE-to-A or B, push-pull driving	1.65 V to 5.5 V			100	ns
t_{dis} (1)	Disable Time	OE-to-A or B, push-pull driving	1.65 V to 5.5 V			410	ns
tr_A (1)	Input Rise Time	A-port rise time, push-pull driving	1.65 V to 1.95 V			20	ns
			2.3 V to 2.7 V	1.6		20	ns
			3.0 V to 3.6 V	1.4		15	ns
			4.5 V to 5.5 V	1.4		15	ns
		A-port rise time, open-drain driving	1.65 V to 1.95 V	1.7		1200	ns
			2.3 V to 2.7 V	1.7		800	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			3.0 V to 3.6 V	1.4		600	ns
			4.5 V to 5.5 V	1.2		500	ns
tr_B (1)	Input Rise Time	B-port rise time, push-pull driving	1.65 V to 1.95 V	1.3		22	ns
			2.3 V to 2.7 V	1.3		20	ns
			3.0 V to 3.6 V	0.9		15	ns
			4.5 V to 5.5 V	0.7		15	ns
		B-port rise time, open-drain driving	1.65 V to 1.95 V	1		1200	ns
			2.3 V to 2.7 V	1		800	ns
			3.0 V to 3.6 V	1		700	ns
			4.5 V to 5.5 V	0.6		500	ns
tf_A (1)	Input Fall Time	A-port fall time, push-pull driving	1.65 V to 1.95 V	1		20	ns
			2.3 V to 2.7 V	1.6		20	ns
			3.0 V to 3.6 V	1.4		15	ns
			4.5 V to 5.5 V	1.4		15	ns
		A-port fall time, open-drain driving	1.65 V to 1.95 V	1.7		20	ns
			2.3 V to 2.7 V	1.7		15	ns
			3.0 V to 3.6 V	1.4		15	ns
			4.5 V to 5.5 V	1.2		15	ns
tf_B (1)	Input Fall Time	B-port fall time, push-pull driving	1.65 V to 1.95 V	1.3		20	ns
			2.3 V to 2.7 V	1.3		15	ns
			3.0 V to 3.6 V	0.9		10	ns
			4.5 V to 5.5 V	0.7		10	ns
		B-port fall time, open-drain driving	1.65 V to 1.95 V	1		20	ns
			2.3 V to 2.7 V	1		20	ns
			3.0 V to 3.6 V	1		15	ns
			4.5 V to 5.5 V	0.7		15	ns
$t_{SK(O)}$ (1)	Skew (time), Output	Channel-to-channel skew, push-pull driving	1.65 V to 5.5 V			1	ns

(1) The data is based on bench test and design simulation; NOT test in production.

AC Timing Requirements — VCCA = 2.5 V

All test conditions: V_{CCA} = 2.3 V to 2.7 V, GND = 0 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Condition	VCCB	Min	Typ	Max	Unit
f_D (1)	Data Rate	Push-pull mode	2.3 V to 2.7 V			65	Mbps
			3.0 V to 3.6 V			80	Mbps
			4.5 V to 5.5 V			90	Mbps
t_W (1)	Pulse Duration	Push-pull mode	2.3 V to 2.7 V	15.4			ns
			3.0 V to 3.6 V	12.5			ns
			4.5 V to 5.5 V	11.1			ns
t_{PHL} (1)	Propagation Delay (High-to-Low)	A-to-B, or B-to-A, push-pull driving	2.3 V to 2.7 V			15	ns
			3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			15	ns
t_{PLH} (1)	Propagation Delay (Low-to-High)	A-to-B, or B-to-A, push-pull driving	2.3 V to 2.7 V			15	ns
			3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			15	ns
t_{en} (1)	Enable Time	OE-to-A or B, push-pull driving	2.3 V to 5.5 V			100	ns
t_{dis} (1)	Disable Time	OE-to-A or B, push-pull driving	2.3 V to 5.5 V			400	ns
tr_A (1)	Input Rise Time	A-port rise time, push-pull driving	2.3 V to 2.7 V	1.9		15	ns
			3.0 V to 3.6 V	1.6		15	ns
			4.5 V to 5.5 V	1.5		15	ns
tr_B (1)	Input Rise Time	B-port rise time, push-pull driving	2.3 V to 2.7 V	1.7		15	ns
			3.0 V to 3.6 V	1.3		10	ns
			4.5 V to 5.5 V	0.9		10	ns
tf_A (1)	Input Fall Time	A-port fall time, push-pull driving	2.3 V to 2.7 V	1.5		10	ns
			3.0 V to 3.6 V	1.2		10	ns
			4.5 V to 5.5 V	1.3		10	ns
tf_B (1)	Input Fall Time	B-port fall time, push-pull driving	2.3 V to 2.7 V	1.4		10	ns
			3.0 V to 3.6 V	0.9		10	ns
			4.5 V to 5.5 V	0.7		10	ns
$t_{SK(O)}$ (1)	Skew (time), Output	Channel-to-channel skew, push-pull driving	2.3 V to 5.5 V			1	ns

(1) The data is based on bench test and design simulation; NOT test in production.

AC Timing Requirements — VCCA = 3.3 V

All test conditions: V_{CCA} = 3.0 V to 3.6 V, GND = 0 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
f_D (1)	Data Rate	Push-pull mode	3.0 V to 3.6 V			90	Mbps
		Push-pull mode	4.5 V to 5.5 V			100	Mbps
t_W (1)	Pulse Duration	Push-pull mode	3.0 V to 3.6 V	11.1			ns
		Push-pull mode	4.5 V to 5.5 V	10			ns
t_{PHL} (1)	Propagation Delay (High-to-Low)	A-to-B, or B-to-A, push-pull driving	3.0 V to 3.6 V			20	ns
			4.5 V to 5.5 V			15	ns
t_{PLH} (1)	Propagation Delay (Low-to-High)	A-to-B, or B-to-A, push-pull driving	3.0 V to 3.6 V			20	ns
			4.5 V to 5.5 V			15	ns
t_{en} (1)	Enable Time	OE-to-A or B, push-pull driving	3.0 V to 5.5 V			100	ns
t_{dis} (1)	Disable Time	OE-to-A or B, push-pull driving	3.0 V to 3.6 V			410	ns
tr_A (1)	Input Rise Time	A-port rise time, push-pull driving	3.0 V to 3.6 V	2.1		15	ns
			4.5 V to 5.5 V	1.4		15	ns
tr_B (1)	Input Rise Time	B-port rise time, push-pull driving	3.0 V to 3.6 V	2		15	ns
			4.5 V to 5.5 V	0.7		10	ns
tf_A (1)	Input Fall Time	A-port fall time, push-pull driving	3.0 V to 3.6 V	1.4		10	ns
			4.5 V to 5.5 V	1.2		10	ns
tf_B (1)	Input Fall Time	B-port fall time, push-pull driving	3.0 V to 3.6 V	1.3		10	ns
			4.5 V to 5.5 V	1.1		10	ns
$t_{SK(O)}$ (1)	Skew (time), Output	Channel-to-channel skew, push-pull driving	3.0 V to 5.5 V			1	ns

(1) The data is based on bench test and design simulation; NOT test in production.

Parameter Measurement Waveforms

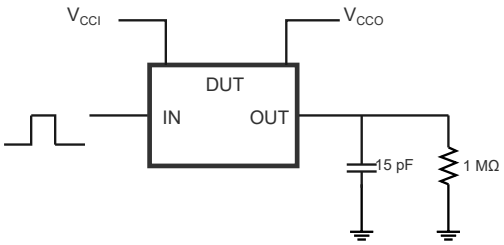


Figure 1. Timing Measurement Load Circuit of Push-Pull Driver

Test	S1
t_{PZL}/t_{PLZ}	2 x V_{CCO}
t_{PHZ}/t_{PZH}	Open

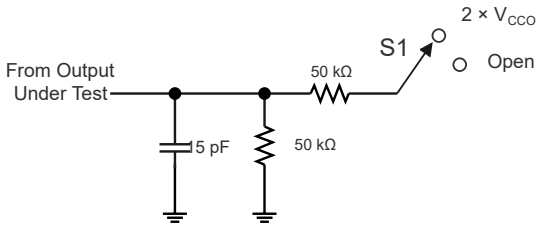


Figure 2. Load Circuit for Enable and Disable Time Measurement

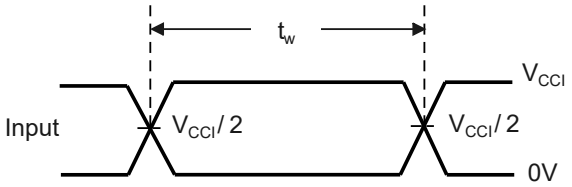


Figure 3. Pulse Duration

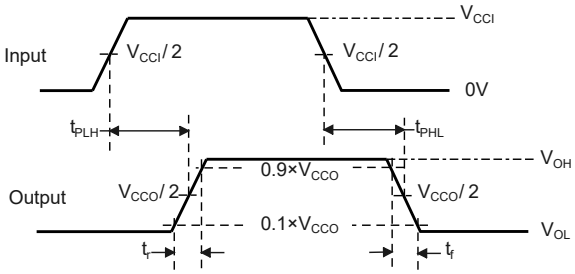


Figure 4. Propagation Delay Times

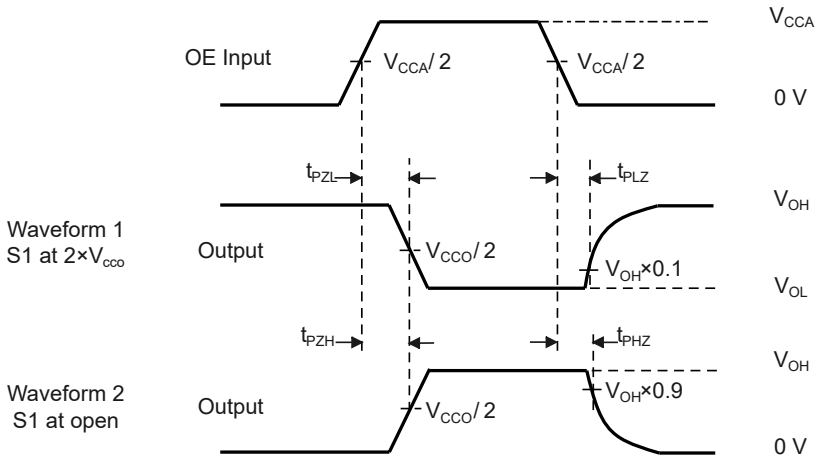


Figure 5. Enable and Disable Times

Detailed Description

Overview

The TPT20204 device is a 4-bit level shifter and supports Push-Pull mode, which functions with an enable (OE) input and can work within the V_{CCA} range from 1.65 V to 3.6 V and the V_{CCB} range from 1.65 V to 5.5 V. V_{CCA} must be less than or equal to V_{CCB}. The TPT20204 supports bidirectional voltage translation among 1.8 V, 2.5 V, 3.3 V, and 5 V. The A1~4 I/Os are connected to the B1~4 I/Os, which allows bidirectional data flow between ports. If OE is low, the translator switch is off, and a high-impedance state exists between ports to isolate both sides. The OE input circuit is internally connected to V_{CCA}. 4-bit bidirectional buffer isolates capacitance and allows 15 pF on either side of the device to support 100 Mbps speeds in Push-Pull mode at 3.3 V V_{CCA} and 5 V V_{CCB}.

Functional Block Diagram

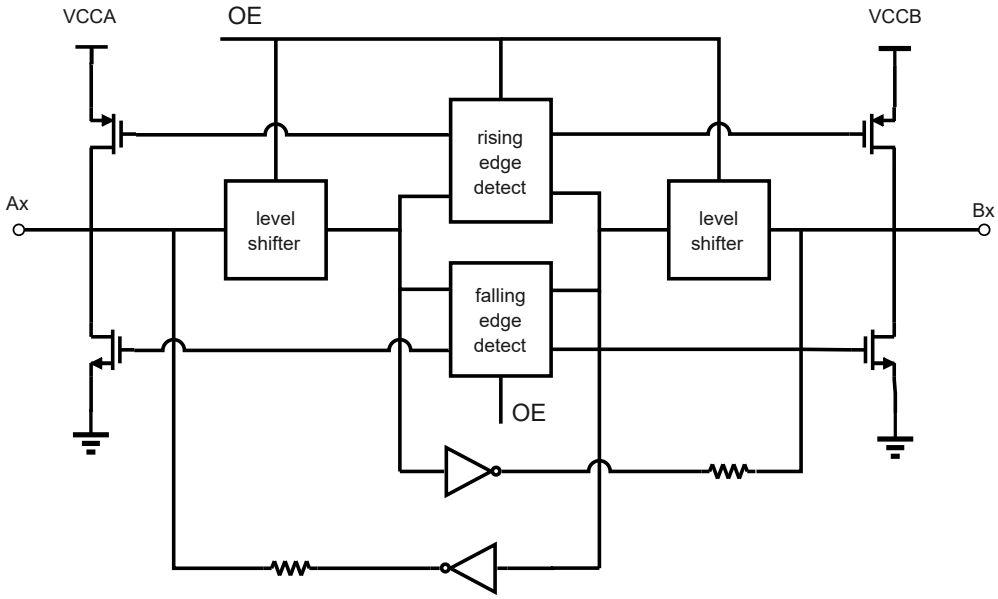


Figure 6. Functional Block Diagram

Feature Description

Power Up

During operation, make sure that $V_{CCA} \leq V_{CCB}$ at all times. During the power-up period, even $V_{CCA} \geq V_{CCB}$, does not damage the device, so there is no power on the sequence requirement, any power supply can be ramped up first.

Enable (OE)

The TPT20204 device has two functional modes: enabled mode and disabled mode. To disable the device setting the OE input as LOW level, which places all I/Os in a high impedance state. Setting the OE input as a HIGH level enables the device.

The OE pin is active HIGH with thresholds referenced to V_{CCA} and an internal pull-up to V_{CCA} that maintains the device active, unless the user selects to disable the TPT20204 when setting OE low to place all I/Os in the high impedance state. The t_{dis} parameter indicates the delay time between the OE pin going low and I/Os outputs entering the high-impedance state. Then Enable time t_{en} indicates the period time during which the user operates the one-shot circuit after the OE pin is going high.

Table 2. Device Function Table

Input OE (1)	Translator Function
H	Ax = Bx
L	Ax is disconnected to Bx, high impedance

(1) OE = Floating, the I/O goes Hi-Z

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT20204 device is a 4-bit level shifter, functions with an enable (OE) input, and can work within the V_{CCA} range from 1.65 V to 3.6 V and the V_{CCB} range from 1.65 V to 5.5 V. V_{CCA} must be less than or equal to V_{CCB}. The TPT20204 supports bidirectional voltage translation between 1.8 V, 2.5 V, 3.3 V, and 5 V. The A1~4 I/Os are connected to the B1~4 I/Os, which allows bidirectional data flow between ports. If EN is low, the translator switch is off, and a high-impedance state exists between ports to isolate both sides. The OE input circuit is internally connected to V_{CCA}.

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

Typical Application

A typical application is shown in Figure 7. The TPT20204 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TPT20204 device is ideal for use in applications where a push-pull driver is connected to the data I/Os.

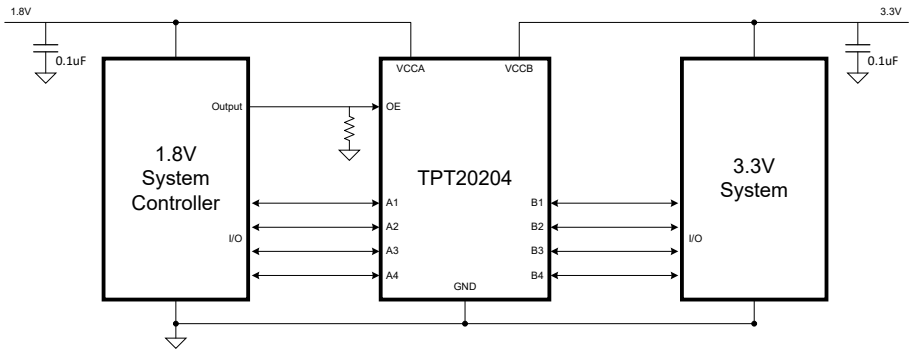


Figure 7. Typical Application Circuit

Layout

Layout Example

Reflections and matching are closely related to loop antenna theory but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they have to turn corners. Below are progressively better techniques for rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

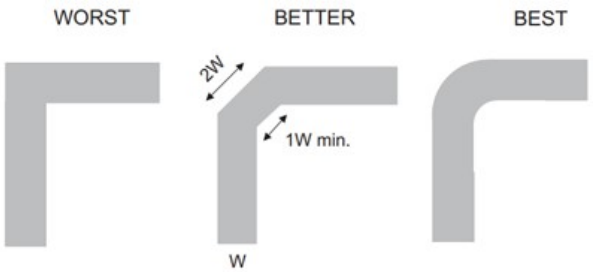


Figure 8. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequency.

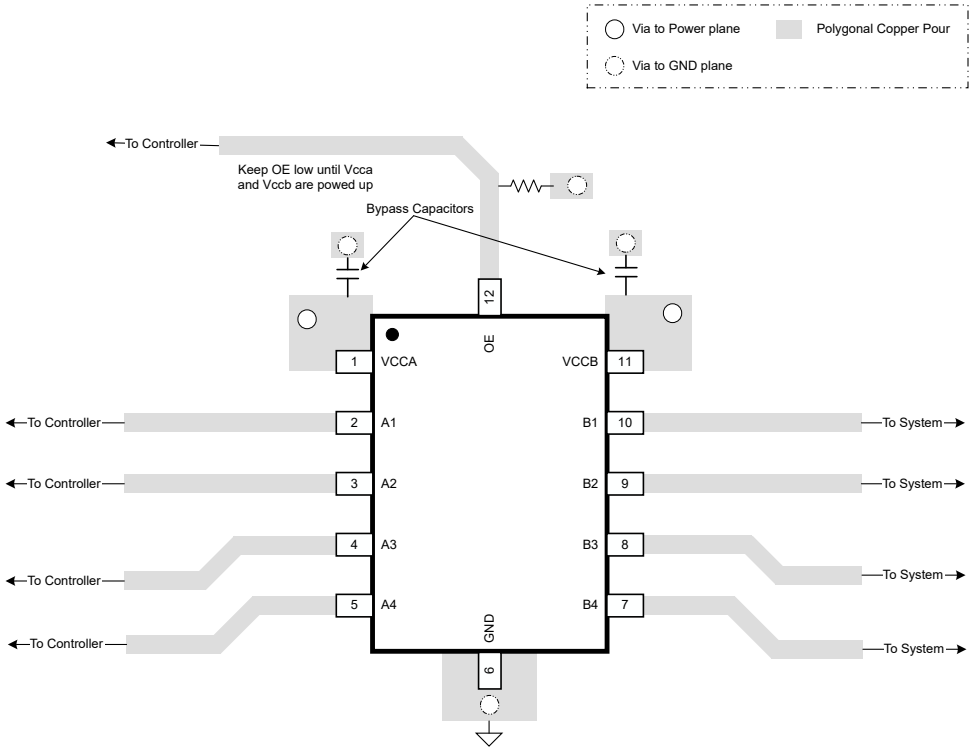
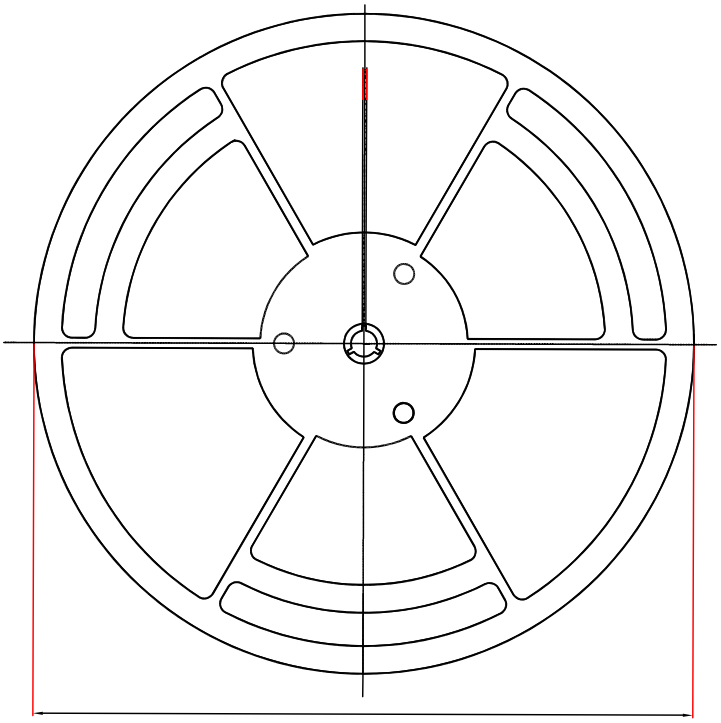
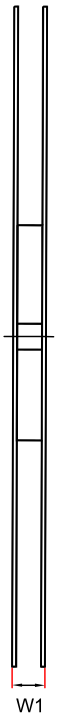
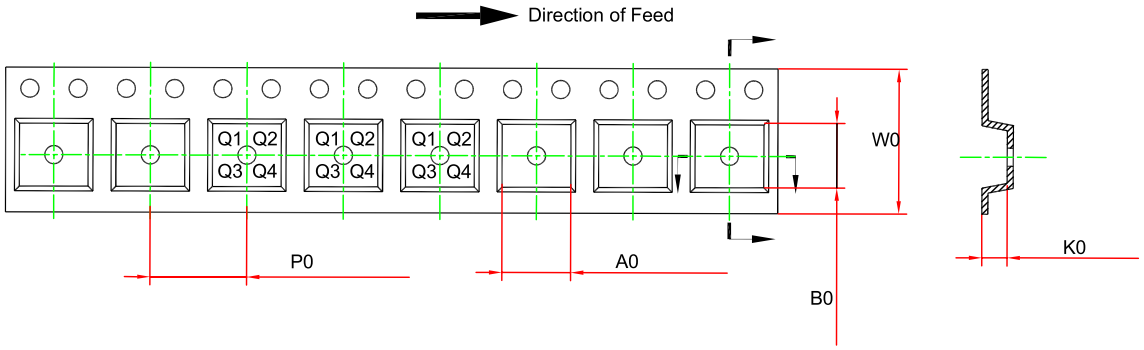


Figure 9. Layout Example

Tape and Reel Information





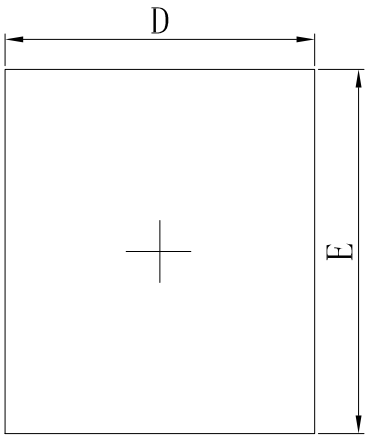


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPT20204-QN5R	QFN1.7x2-12	180.0	1.9	0.75	8.0	13.1	2.3	4.0	Q1

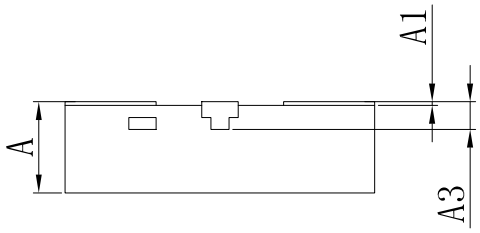
Package Outline Dimensions

QFN1.7X2-12

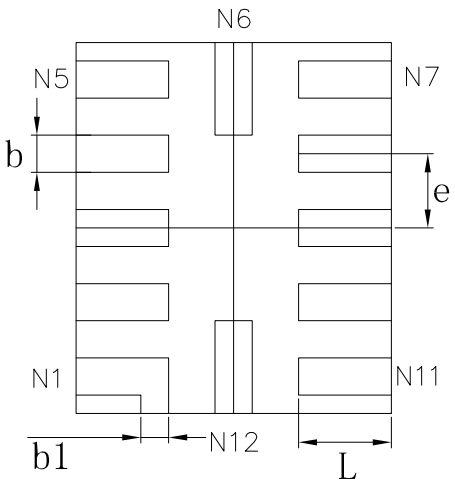
Package Outline Dimensions QN5(QFN1.7X2-12-A)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
A3	0.152 REF		0.006 REF	
b	0.150	0.250	0.006	0.010
b1	0.150 REF		0.006 REF	
D	1.600	1.800	0.063	0.071
E	1.900	2.100	0.075	0.083
e	0.400 BSC		0.016 BSC	
L	0.400	0.600	0.016	0.024

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT20204-QN5R	−40 to 125°C	QFN1.7x2-12	T24	MSL1	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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