TPT1462VQ, TPT1462Q

Automotive Fault Protected High-Speed CAN FD SIC Transceiver with Standby Mode

Features

- Meets the ISO 11898-2:2024 and CiA601-4 for Signal Improvement Capability(SIC) and SAE J2284-1 to SAE J2284-5 Physical Layer Standards
- Supports Classical CAN and Optimized CAN FD SIC up to 8 Mbps Data Rates
- Short and Symmetrical Propagation Delay and Fast Loop Delay for Enhanced Timing Margin
- 5-V Power Supply, I/O Voltage Range Supports 1.7-V to 5.5-V MCU Interface (V variants only)
- Ultra-low Current Standby Mode with Bus Wake-up Capability
- Ideal Passive Behavior to CAN Bus when Unpowered
- Glitch-free on CAN Bus and RXD when Power on/off
- Protection Feature:
  - Bus HBM ESD Protection up to 15 kV and IEC 61000-4-2 ESD Protection
  - Bus Fault Protection: ±45 V
  - VCC and VIO (V variants only) Undervoltage Protection
  - TXD Dominant Time-out Function and Bus-dominant Time-out
  - Thermal Shutdown Protection
- Available in the SOP8 Package and the Leadless DFN3X3-8 Package with Improved Automated Optical Inspection (AOI) Capability
- AEC-Q100 Qualified for Automotive Applications， Grade 1

Applications

- All Devices Supporting Highly Loaded CAN Networks
- Automotive and Transportation
  - Body Electronics / Lighting
  - Power Train / Chassis
  - Infotainment / Cluster
  - ADAS / Safety

Description

The TPT1462VQ and the TPT1462Q are CAN transceivers that meet the ISO11898-2:2024, CiA601-4 signal improvement capability (SIC), and SAEJ2284-1 to SAE J2284-5 high-speed CAN (Controller Area Network) physical layer standards.

The devices are designed to be used in CAN FD networks up to 8 Mbps with enhanced timing margin. The system design can be optimized with excellent electromagnetic compatibility (EMC) and electrostatic discharge (ESD) performance. The TPT1462VQ has a secondary power supply input VIO pin for I/O level shifting to support 1.8-V, 2.5-V, 3.3-V, and 5-V MCU logic levels directly. This family has a low-current standby mode with CAN bus waked-up capability via wake-up pattern (WUP) which is defined in ISO11898-2:2024.

As designed, the devices feature bus fault protection from −45 V to +45 V, TXD dominant time-out (DTO), over-temperature shutdown (TSD). Additionally, all devices include power-off ideal passive behavior fail-safe features to enhance the network robustness.

The TPT1462VQ and the TPT1462Q are available in SOP8 and DFN3X3-8 packages and are AEC-Q100 qualified for automotive applications.

Typical Application Circuit

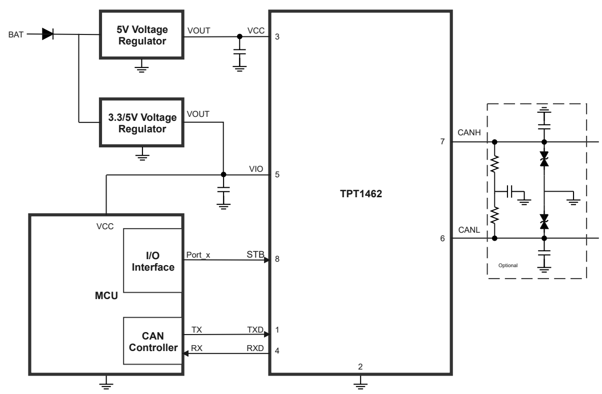


Table of Contents

Product Family Table

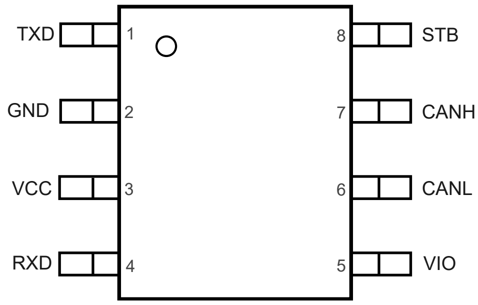
Order Number	VCC (V)	VIO (V)	BUS Protection (V)	Package
TPT1462VQ-SO1R-S	5	1.7 to 5.5	±45	SOP8
TPT1462VQ-DFCR-S	5	1.7 to 5.5	±45	DFN3X3-8
TPT1462Q-SO1R-S	5	NC	±45	SOP8
TPT1462Q-DFCR-S	5	NC	±45	DFN3X3-8

Revision History

Date	Revision	Notes
2023-01-05	Rev.Pre.0	Initial version
2024-11-22	Rev.A.0	Released version

Pin Configuration and Functions

TPT1462VQ
SOP8 Package
Top View



TPT1462VQ
DFN3X3-8 Package
Top View

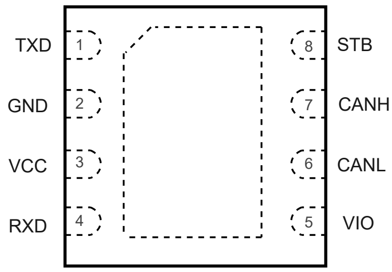
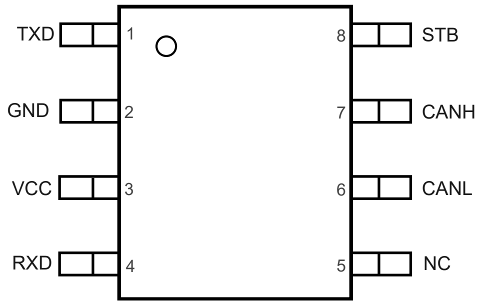


Table 1. Pin Functions: TPT1462VQ

Pin		I/O	Description
No.	Name		
1	TXD	I	CAN transmit data input, internal weak pull-up (low for dominant and high for recessive bus states)
2	GND (1)	GND	Ground
3	VCC	POWER	Transceiver 5-V supply voltage
4	RXD	O	CAN receive data output (low for dominant and high for recessive bus states)
5	VIO	POWER	Transceiver I/O level shifting supply voltage
6	CANL	BUS I/O	Low-level CAN bus input/output line
7	CANH	BUS I/O	High-level CAN bus input/output line
8	STB	I	Standby mode control input, internal weak pull-up (active high)

(1) The DFN package die is connected to both the GND pin and the exposed pad. The GND pin must be soldered to the board ground and for enhanced thermal and electrical performance, the exposed pad is also recommended to be soldered to the board ground.



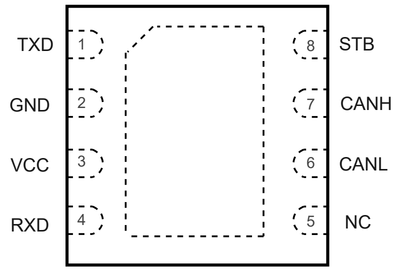


Table 2. Pin Functions: TPT1462Q

Pin		I/O	Description
No.	Name		
1	TXD	I	CAN transmit data input (low for dominant and high for recessive bus states)
2	GND (1)	GND	Ground
3	VCC	Power	Transceiver 5-V supply voltage
4	RXD	O	CAN receive data output (low for dominant and high for recessive bus states)
5	NC	−	Not connected, no bonding
6	CANL	Bus I/O	Low-level CAN bus input/output line
7	CANH	Bus I/O	High-level CAN bus input/output line
8	STB	I	Standby mode control input (active high)

(1) The DFN package die is connected to both the GND pin and the exposed pad. The GND pin must be soldered to the board ground and for enhanced thermal and electrical performance, the exposed pad is also recommended to be soldered to the board ground.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Supply Voltage Range	−0.3	7	V
V_{IO}	I/O Level-shifting Voltage Range	−0.3	7	V
V_{BUS}	CAN Bus Voltage Range (CANH, CANL)	−45	45	V
V_{BUS_DIFF}	Differential Output Voltage of CAN Bus, (CANH - CANL)	−45	45	V
V_{LOGIC_IN}	Logic Input Terminal Voltage Range (TXD, STB)	−0.3	7	V
V_{LOGIC_OUT}	Logic Output Terminal Voltage Range (RXD)	−0.3	7	V
T_J	Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature	−55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD and Transient Ratings

Parameter		Condition	Min	Max	Unit
V_{ESD}	Electrostatics Discharge (1)(2)	IEC61000-4-2(150pF, 330Ω discharge circuit), contact discharge on bus pins (CANH, CANL)	−8	8	kV
		Human Body Model (HBM) on all pins Human Body Model (HBM) on bus pins (CANH, CANL)	−15	15	kV
		Human Body Model (HBM) on all pins	−8	8	kV
		Charged Device Model (CDM) on all pins	−750	750	V
V_{TRAN}	Transient Immunity ISO 7637-2 on Bus Pins	Pulse1	−100		V
		Pulse2a		75	V
		Pulse3a	−150		V
		Pulse3b		100	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

	Parameter	Min	Max	Unit
V_{IO}	Input/output Voltage, TXD, RXD, STB	1.7	5.5	V
V_{CC}	Power Supply	4.5	5.5	V
$I_{OH(RXD)}$	RXD Terminal High-Level Output Current	−1		mA
$I_{OL(RXD)}$	RXD Terminal Low-Level Output Current		1	mA
T_J	Operating Junction Temperature	−40	150	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8	118	48	°C/W
DFN3x3-8	51	23	°C/W

Electrical Characteristics

All test conditions: V_{CC} = 4.5 V to 5.5 V, V_{IO} = 1.7 V to 5.5 V, R_L = 60 Ω, T_J = −40°C to 150°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pin VCC; Power Supply						
V_{CC}	Supply Voltage		4.5		5.5	V
$V_{UVD\_STB\_VCC}$	Standby Undervoltage Detection on V_{CC}		4		4.5	V
$V_{UVD\_SWOFF\_VCC}$	Switch-off Undervoltage Detection on V_{CC} for Protected Mode (Variants without V suffix)		1.35	1.5	1.65	V
I_{CC}	Normal Mode Supply Current	Dominant, V_{TXD} = 0 V; t < t_{TXD_DTO}		48	70	mA
		Dominant bus fault, V_{TXD} = 0 V; short circuit on bus lines; −40 V < (V_{CANH} = V_{CANL}) < +40 V		65	115	mA
		Recessive; V_{TXD} = V_{IO}		2.5	10	mA
	Standby Mode Supply Current	Device with the "V" suffix; V_{STB} = V_{IO}		0.3	2	µA
		Device without the "V" suffix; V_{STB} = V_{CC}		8.0	17.5	µA
Pin VIO; IO Level Adapter Power Supply (variants with V suffix only)						
V_{IO}	Supply Voltage		1.7		5.5	V
V_{UV_VIO}	Rising Undervoltage Detection on V_{IO} for Protected Mode				1.65	V
	Falling Undervoltage Detection on V_{IO} for Protected Mode		1.35			V
V_{HYS_UVVIO}	Hysteresis Voltage on V_{IO} Undervoltage Detection (1)			300		mV
I_{IO}	Normal Mode Supply Current	Dominant; V_{TXD} = 0 V		290	500	µA
		Recessive; V_{TXD} = V_{IO}		110	210	µA
	Standby Mode Supply Current	V_{STB} = V_{IO}		10	19	µA
Pin STB; Standby Mode Control Input						
V_{IH}	High-level Input Voltage	VIO = VCC for variants without V suffix	0.7 × V_{IO}		V_{IO} + 0.3	V
V_{IL}	Low-level Input Voltage	VIO = VCC for variants without V suffix	−0.3		0.3 × V_{IO}	V
V_{HYS_STB}	Hysteresis Voltage on Pin STB (1)			300		mV
R_{PU}	Pull-up Resistance		20		80	kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance (1)				10	pF
Pin TXD; CAN Transit Data Input						
V_{IH}	High-level Input Voltage	$V_{IO} = V_{CC}$ for variants without V suffix	0.7 × V_{IO}		V_{IO} + 0.3	V
V_{IL}	Low-level Input Voltage	$V_{IO} = V_{CC}$ for variants without V suffix	−0.3		0.3 × V_{IO}	V
V_{HYS_TXD}	Hysteresis Voltage on Pin TXD (1)			300		mV
R_{PU}	Pull-up Resistance		20		80	kΩ
C_{IN}	Input Capacitance (1)				10	pF
Pin RXD; CAN Receive Data Output						
I_{OH}	High-level Output Current	$V_{RXD} = V_{IO}$ - 0.4 V	−10		−1	mA
I_{OL}	Low-level Output Current	V_{RXD} = 0.4 V; Bus dominant	1		35	mA
Pin CANH, CANL; Bus lines						
V_{O_DOM}	Dominant Output Voltage, CANH	Dominant; V_{TXD} = 0 V; t < t_{TXD_DTO}; 50 Ω ≤ R_L ≤ 65 Ω; 4.75 V ≤ VCC ≤ 5.25 V	2.89	3.5	4.26	V
	Dominant Output Voltage, CANH	Dominant; V_{TXD} = 0 V; t < t_{TXD_DTO}; 50 Ω ≤ R_L ≤ 65 Ω	2.75	3.5	4.5	V
	Dominant Output Voltage, CANL	Dominant, V_{TXD} = 0 V; t < t_{TXD_DTO}; 50 Ω ≤ R_L ≤ 65 Ω ; 4.75 V ≤ VCC ≤ 5.25 V	0.77	1.5	2.13	V
	Dominant Output Voltage, CANL	Dominant, V_{TXD} = 0 V; t < t_{TXD_DTO}; 50 Ω ≤ R_L ≤ 65 Ω	0.5	1.5	2.25	V
$V_{DOM\_TX\_SYM}$	Transmitter Dominant Voltage Symmetry	$V_{DOM\_TX\_SYM} = V_{CC} - V_{CANH} - V_{CANL}$	−300		300	mV
V_{SYM}	Transmitter Symmetry (Dominant or Recessive) (1)	$V_{SYM} = V_{CANH} + V_{CANL} / V_{CC}$; C_{SPLIT} = 4.7 nF; f_{TXD} = 250 kHz, 1 MHz, 2.5 MHz	0.9		1.1	V/V
V_{OD_DOM}	Dominant Differential Output Voltage	Normal mode; 4.75 V ≤ VCC ≤ 5.25 V ;V_{TXD} = 0 V; t < t_{TXD_DTO}; 50 Ω ≤ R_L ≤ 65 Ω	1.5		3.0	V
		Normal mode; 4.75 V ≤ VCC ≤ 5.25V ;V_{TXD} = 0 V; t < t_{TXD_DTO}; 45 Ω ≤ R_L ≤ 70 Ω	1.4		3.3	V
		Normal mode; 4.75 V ≤ VCC ≤ 5.25V ;V_{TXD} = 0 V; t < t_{TXD_DTO}; R_L = 2240 Ω	1.5		5.0	V
V_{OD_REC}	Recessive Differential Output Voltage	Normal mode; $V_{TXD} = V_{IO}$; no load	−50		50	mV
		Standby mode; no load	−0.2		0.2	V
V_{O_REC}	Recessive Output Voltage	Normal mode; $V_{TXD} = V_{IO}$; no load	2.0	2.5	3.0	V
		Standby mode; no load	−0.1		0.1	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{TH\_RX\_DIF}$	Differential Receiver Threshold Voltage	Normal mode; $t < t_{TXD\_DTO}$; −12 V ≤ V_{CANH}/ V_{CANL} ≤ +12 V	0.5		0.9	V
		Standby mode; $t < t_{TXD\_DTO}$; −12 V ≤ V_{CANH}/ V_{CANL} ≤ +12 V	0.4		1.1	V
V_{REC_RX}	Receiver Recessive Voltage (1)	Normal mode; $t < t_{TXD\_DTO}$; −12 V ≤ V_{CANH}/ V_{CANL} ≤ +12 V	−4		0.5	V
		Standby mode; $t < t_{TXD\_DTO}$; −12 V ≤ V_{CANH}/ V_{CANL} ≤ +12 V	−4		0.4	V
V_{DOM_RX}	Receiver Dominant Voltage (1)	Normal mode; $t < t_{TXD\_DTO}$; −12 V ≤ V_{CANH}/ V_{CANL} ≤ +12 V	0.9		9.0	V
		Standby mode; $t < t_{TXD\_DTO}$; −12 V ≤ V_{CANH}/ V_{CANL} ≤ +12 V	1.1		9.0	V
$V_{HYS\_RX\_DIF}$	Differential Receiver Hysteretic Threshold	Normal mode; $t < t_{TXD\_DTO}$; −12 V ≤ V_{CANH}/ V_{CANL} ≤ +12 V	50	100	300	mV
$I_{O\_SC\_DOM}$	Dominant Short-Circuit Output Current	V_{TXD} = 0 V; $t < t_{TO\_DOM\_TXD}$; V_{CC} = 5 V; −40V ≤ V_{CANH}/ V_{CANL} ≤ +40V		55	100	mA
$I_{O\_SC\_REC}$	Recessive Short-Circuit Output Current	V_{TXD} = V_{IO}; $t < t_{TO\_DOM\_TXD}$; V_{CC} = 5 V; −40V ≤ V_{CANH}/ V_{CANL} ≤ +40V	−3		3	mA
I_L	Unpowered Bus Input Leakage Current	V_{CC} = V_{IO} = 0 V or V_{CC} = V_{IO} pins shorted to GND via 47 kΩ; V_{CANH} = V_{CANL} = 5 V	−10		10	μA
R_{IN}	CANH or CANL Input Resistance	−2 V ≤ V_{CANH} / V_{CANL} ≤ +7 V	25	35	50	kΩ
ΔR_{IN}	Input Resistance Deviation	−2 V ≤ V_{CANH} / V_{CANL} ≤ +7 V CANH	−3		3	%
R_{IN_DIF}	Differential Input Resistance	−2 V ≤ V_{CANH} / V_{CANL} ≤ +7 V	50	70	100	kΩ
C_{IN}	Common Mode Input Capacitance (1)				20	pF
C_{IN_DIF}	Differential Input Capacitance (1)				10	pF
Pin CANH, CANL; Bus Lines Signal Improvement Capability (SIC)						
$R_{IN\_ACT\_REC}$	Active Recessive Phase Internal Resistance (1)	Recessive; V_{TXD} = 0 V; $t < t_{TXD\_DTO}$; −12 V ≤ V_{CANH} / V_{CANL} ≤ +12 V; $R_{IN\_DIF\_ACT\_REC}$ = $R_{IN\_ACT\_REC\_CANH}$ + $R_{IN\_ACT\_REC\_CANL}$	37.5		66.5	Ω
$R_{IN\_DIF\_ACT\_REC}$	Active Recessive Phase Differential Internal Resistance (1)	Recessive; V_{TXD} = 0 V; $t < t_{TXD\_DTO}$; −12 V ≤ V_{CANH} / V_{CANL} ≤ +12 V; $R_{IN\_DIF\_ACT\_REC}$ = $R_{IN\_ACT\_REC\_CANH}$ + $R_{IN\_ACT\_REC\_CANL}$	75		133	Ω
Temperature Detection						
T_{J_SD}	Thermal Shutdown Temperature (1)		160	175	190	℃
$_{J\_SD\_HYS}$	Thermal Shutdown Hysteresis (1)			20		℃

(1) The data is based on bench test and design simulation.

AC Timing Requirements

All test conditions: V_{CC} = 4.75 V to 5.25 V, V_{IO} = 1.7 V to 5.5 V, R_L = 60 Ω, T_J = −40°C to 150°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
CAN Timing Characteristics						
$t_{D\_TXD\_BUSDOM}$	Delay time from TXD to bus dominant	Normal mode;			80	ns
$t_{D\_TXD\_BUSREC}$	Delay time from TXD to bus recessive	Normal mode;			80	ns
$t_{D\_BUSDOM\_RXD}$	Delay time from bus dominant to RXD	Normal mode;			110	ns
$t_{D\_BUSREC\_RXD}$	Delay time from bus recessive to RXD	Normal mode;			110	ns
$t_{D\_TXDL\_RXDL}$	Loop delay time from TXD low to RXD low	Normal mode;			190	ns
$t_{D\_TXDH\_RXDH}$	Loop delay time from TXD high to RXD high	Normal mode;			190	ns
CAN FD Signal Improvement Capability (SIC) Timing Characteristics;						
t_{BIT_BUS}	Transmitted recessive bit width	2 Mbps, tBIT_TXD = 500 ns	490		510	ns
		5 Mbps, tBIT_TXD = 200 ns	190		210	ns
		8 Mbps, tBIT_TXD = 125 ns	115		135	ns
t_{BIT_RXD}	RXD bit width	2 Mbps, tBIT_TXD = 500 ns	470		520	ns
		5 Mbps, tBIT_TXD = 200 ns	170		220	ns
		8 Mbps, tBIT_TXD = 125 ns	95		145	ns
Δt_{REC}	Receiver timing symmetry	2, 5, 8 Mbps; $\Delta t_{REC} = t_{BIT\_RXD} - t_{BIT\_BUS}$	−20		15	ns
Δt_{BIT_BUS}	Transmitted recessive bit width variation	$\Delta t_{BIT\_BUS} = t_{BIT\_BUS} - t_{BIT\_TXD}$	−10		10	ns
Δt_{BIT_RXD}	Received recessive bit width variation	$\Delta t_{BIT\_RXD} = t_{BIT\_RXD} - t_{BIT\_TXD}$	−30		20	ns
Δt_{REC}	Receiver timing symmetry variation	$\Delta t_{REC} = t_{BIT\_RXD} - t_{BIT\_BUS}$	−20		15	ns
$t_{ACT\_REC\_START}$	Start time of active signal improvement phase Start time of active signal improvement phase (1)				120	ns
$t_{PAS\_REC\_START}$	Signal improvement start time of passive recessive phase (1)				530	ns
$t_{ACT\_REC\_END}$	End time of active signal improvement phase (1)		355			ns
Device Timing Characteristics						

Parameter		Conditions	Min	Typ	Max	Unit
t_{TXD_DTO}	TXD dominant time-out time	Normal mode; V_{TXD} = 0 V	0.8	2.0	9.0	ms
t_{WAKE_BUS}	Bus wake-up time (dominant or recessive)	Standby mode	0.5		1.8	µs
$t_{WAKE\_BUS\_TO}$	Bus wake-up time-out time (1)	Standby mode	0.8	3.0	9.0	ms
$t_{WAKE\_BUS\_FILTER}$	Bus wake-up filter time (1)	Standby mode			1.8	µs
t_{MODE}	Mode transition time (1)				40	µs
t_{START_UP}	Start-up time (1)				0.5	ms
$t_{START\_UP\_RXD}$	RXD Start-up time (1)	After wake-up detected	4		20	µs
t_{UVD}	Undervoltage detection time (1)	Pin VCC			30	µs
t_{UVD_OFF}	Switch-off undervoltage detection time (1)	Pin VCC; Device without V suffix			30	µs
		Pin VIO; Device without V suffix			30	µs
t_{UVR}	Undervoltage recovery time (1)	Pin VCC			30	µs

(1) The test data is based on bench tests and design simulation.

Parameter Measurement Information

Test Circuit

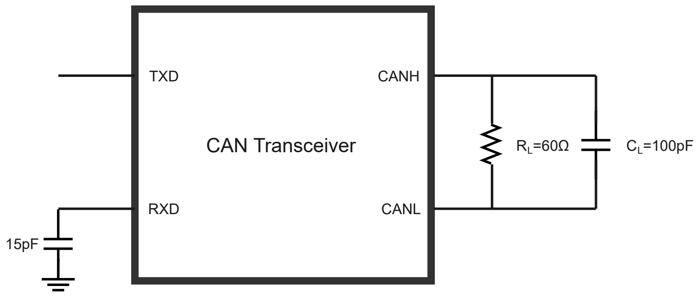


Figure 1. CAN Transceiver Timing Parameter Test Circuit

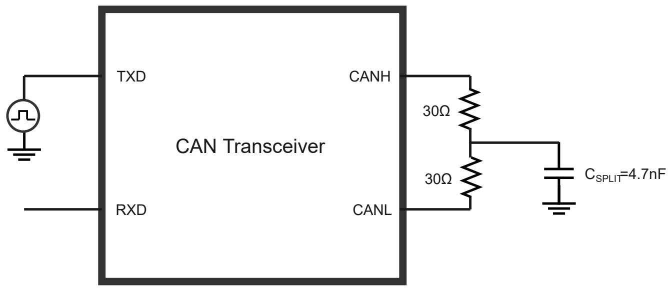


Figure 2. CAN Transceiver Driver Symmetry Test Circuit

Parameter Diagram

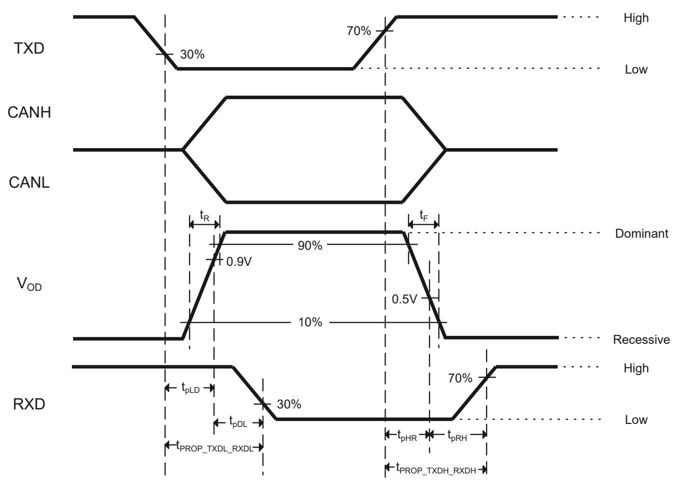


Figure 3. CAN Transceiver Timing Diagram

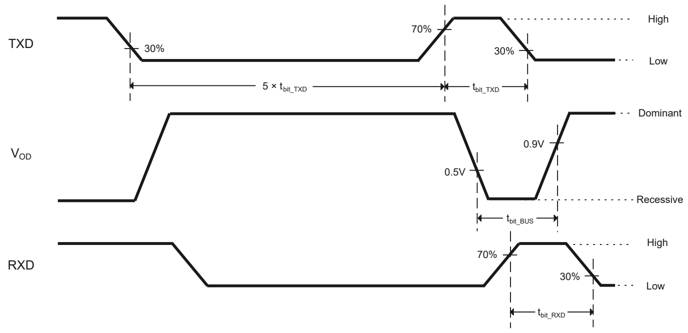


Figure 4. CAN FD Timing Parameter Diagram

Detailed Description

Overview

The TPT1462VQ and the TPT1462Q are CAN transceivers that meet the ISO11898-2:2024, CiA601-4 signal improvement capability(SIC), and SAEJ2284-1 to SAE J2284-5 high-speed CAN (Controller Area Network) physical layer standards. The devices are designed to be used in CAN FD networks up to 8 Mbps with an enhanced timing margin. The system design can be optimized with excellent electromagnetic compatibility (EMC) and electrostatic discharge (ESD) performance. The TPT1462VQ has a secondary power supply input VIO pin for I/O level shifting to support 1.8-V, 2.5-V, 3.3-V, and 5-V MCU logic levels directly. This family has a low-current standby mode with CAN bus waked-up capability via wake-up pattern (WUP) which is defined in ISO11898-2:2024. As designed, the devices feature bus fault protection from −45 V to +45 V, TXD dominant time-out (DTO), and over-temperature shutdown (TSD). Additionally, all devices include power-off ideal passive behavior fail-safe features to enhance the network robustness. The TPT1462VQ and the TPT1462Q are available in SOP8 and DFN3X3-8 packages and are AEC-Q100 qualified for automotive applications.

Functional Block Diagram

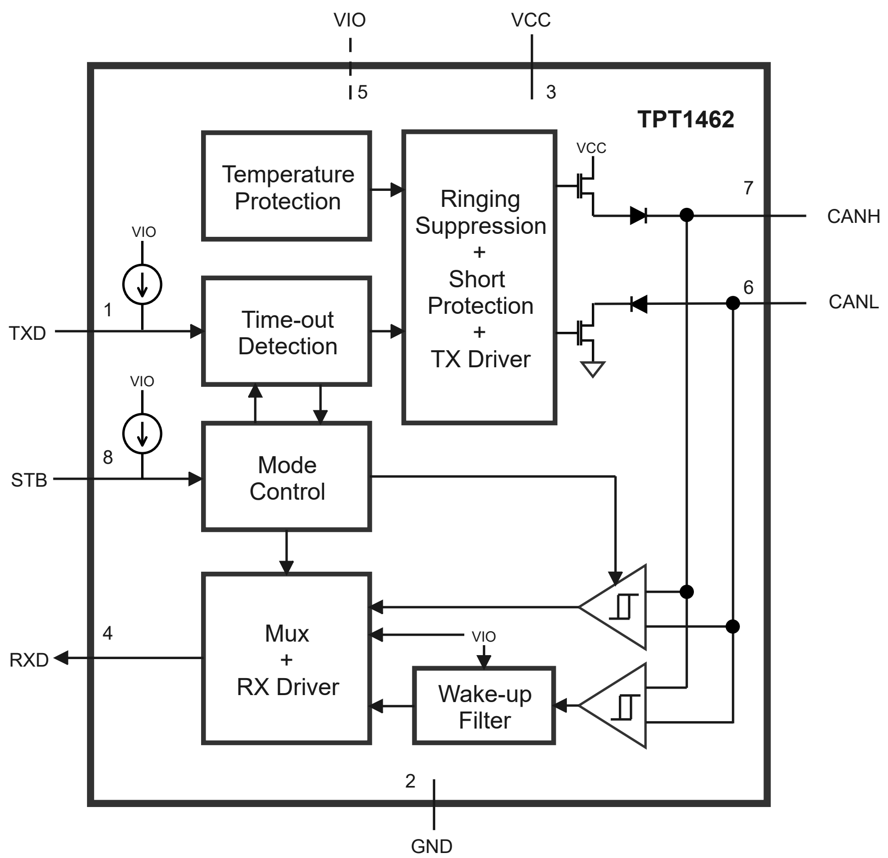


Figure 5. Functional Block Diagram

(1) Pin5 is not connected and VIO = VCC in variants without V suffix

Feature Description

Device Operating Modes

Table 3. Operating Modes Table

<table>
<tr><th rowspan="2">Mode</th><th colspan="2">Inputs</th><th colspan="2">Outputs</th></tr>
<tr><th>STB Pin</th><th>TXD Pin</th><th>CAN BUS State</th><th>RXD Pin</th></tr>
<tr><td rowspan="3">Normal</td><td rowspan="3">Low</td><td>Low</td><td>Dominant</td><td>L</td></tr>
<tr><td rowspan="2">H or Open (Internal weak pull-up)</td><td rowspan="2">Recessive</td><td>Low when bus dominant</td></tr>
<tr><td>High when bus recessive</td></tr>
<tr><td rowspan="2">Standby</td><td rowspan="2">High or Open (Internal weak pull-up)</td><td rowspan="2">X (Don't care)</td><td rowspan="2">Biased to ground</td><td>Follow bus state when wake-up detected</td></tr>
<tr><td>High when no wake-up detected</td></tr>
</table>

Normal Mode

A low level on the STB pin sets the device into Normal mode. In normal mode, the transceiver is fully operational, it can transmit and receive data via CANH and CANL bus lines. The differential receiver converts the analog data on the bus lines into digital output on the RXD pin. The driver converts the digital data on the TXD pin to differential analog output on bus lines, the slopes of the output signals on the bus lines are controlled internally and optimized to guarantee the lowest possibility for Electro Magnetic Emission (EME).

Standby Mode

Activate the low-power standby mode by setting the STB terminal high. In this mode, the bus transmitter is not able to send data, and the normal mode receiver is not able to accept data as the bus lines are biased to ground minimizing the system supply current. Only the low-power receiver is actively monitoring the bus for activity. RXD follows the bus state after a valid wake-up signal has been detected on the bus. For the variants with the V suffix, the low-power receiver is powered using the VIO pin only, this allows V_{CC} to be removed reducing power consumption further. The device transmits into Normal mode after the STB pin is forced low.

Remote Wake-up

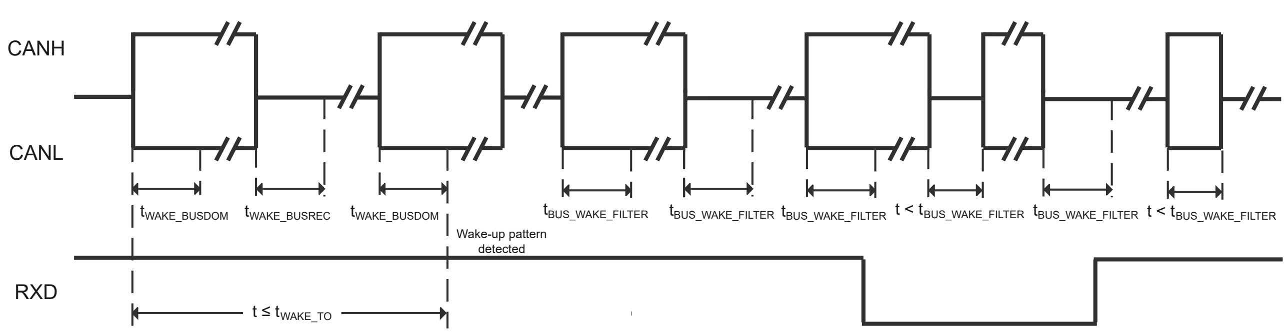
A dedicated wake-up pattern (specified in ISO11898-2:2024) on the can bus wakes up the device from standby mode, this filtering prevents the device from being woken up by bus dominant clamped, or noise on the bus. The wake-up pattern consists of the following:

- a dominant phase of at least t_{WAKE_BUSDOM} followed by
- a recessive phase of at least t_{WAKE_BUSRES} followed by
- a dominant phase of at least t_{WAKE_BUSDOM}

The complete wake-up pattern (dominant-recessive-dominant) must be received within $t_{TO\_WAKE\_BUS}$, otherwise, the internal wake-up logic is reset to wait for the next valid wake-up pattern, the complete wake-up pattern needs to be reserved to wake-up the device. RXD pin keeps high until the device is woken up. A wake-up event is not flagged on the RXD pin if any of the following events occurs:

- The device transits to Normal mode
- An undervoltage event is detected

- The complete wake-up pattern was not received within $t_{TO\_WAKE\_BUS}$



Protection Features

TXD Dominant Time-out

The device detects TXD dominant time-out and prevents a permanent low on the TXD pin, caused by application failure, driving the CAN bus into permanent dominant blocking the CAN bus network. A TXD dominant time-out timer is started when the TXD pin is set low, if the TXD pin remains low for longer than t_{TXD_DTO}, the transmitter is disabled, releasing the bus lines to a recessive state. The TXD dominant time-out timer is reset when the TXD pin is set high.

TXD and STB Pins Internal Biasing

There are internal weak pull-ups to VCC (variants without V suffix) or VIO (variants with V suffix) on TXD and STB pins to ensure a defined safe state in case these pins are floating. Both pins should be held high in Standby mode to minimize the supply current.

Under-voltage Lockout (UVLO)

The device integrates under-voltage to detect and lockout the circuit of the supply terminal to keep the device in protected mode if the supply voltage drops below the threshold until the supply voltage is higher than the UVLO threshold. This protects the device and system during undervoltage events on supply terminals.

If VCC drops below the standby undervoltage detection threshold, the device transits to Standby mode. The STB pin state is ignored until the VCC power supply is recovered. If VCC (variants without V suffix) or VIO (variants with V suffix) drops below the switch-off undervoltage detection threshold, the device switches off until the power supply has recovered.

Overtemperature Protection (OTP)

The device is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature T_{J_SD}, the output drivers is disabled until the virtual junction temperature falls below $T_{J\_SD\_R}$ and TXD sets to high again.

VIO Supply Pin

VIO pin should be connected to the microcontroller supply voltage, this adjusts the voltage level of TXD, RXD, and STB pins to the microcontroller I/O level, this allows the device to interface with 5-V, 3.3-V, and 1.8-V supplied microcontroller without additional level shifter. VIO pin also powers the low-power receiver, this allows wake-up frame to be detected without VCC power supply in low-power applications. For the device without a VIO pin, all block is connected to VCC, pin5 is not connected internally.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT1462xQ is a CAN SIC transceiver that supports CAN FD up to 8 Mbps, with BUS protection voltage from –45 V to +45 V. The VIO of TPT1462VQ can support the voltage level of TXD and RXD from 1.7 V to 5.5 V. The following sections show a typical application of the TPT1462xQ.

Typical Application

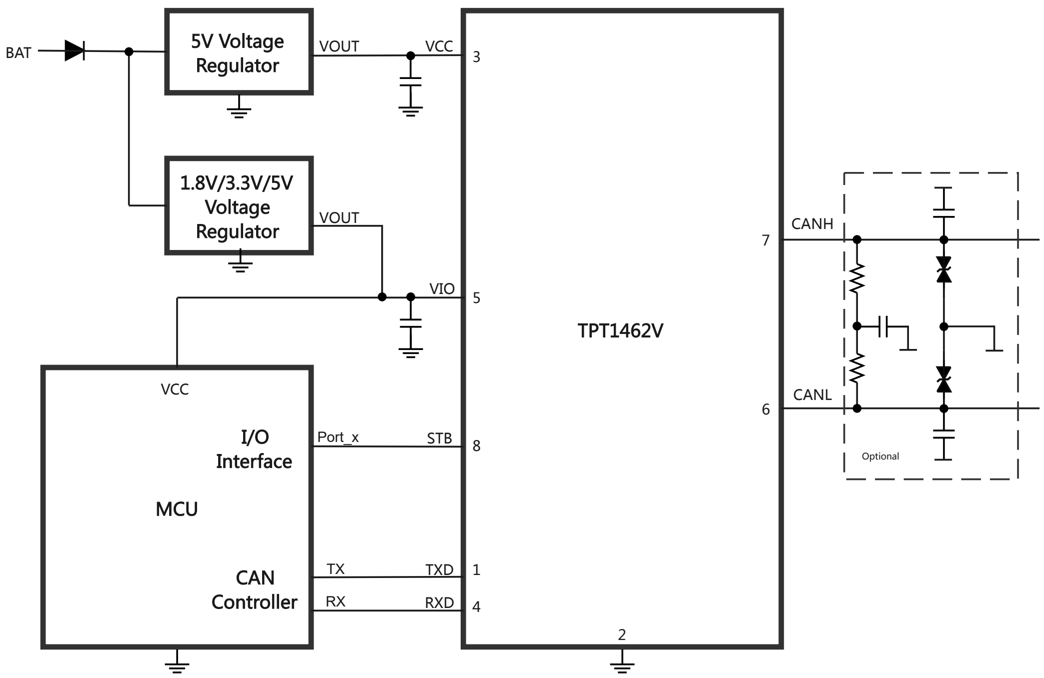


Figure 6. TPT1462VQ Typical Application Circuit

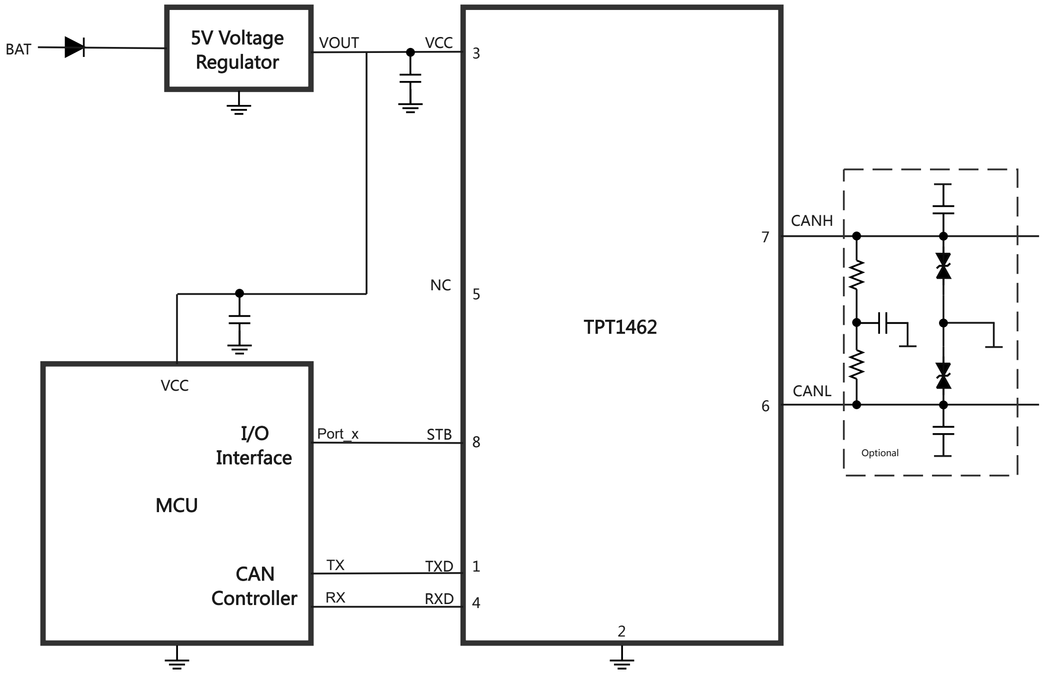
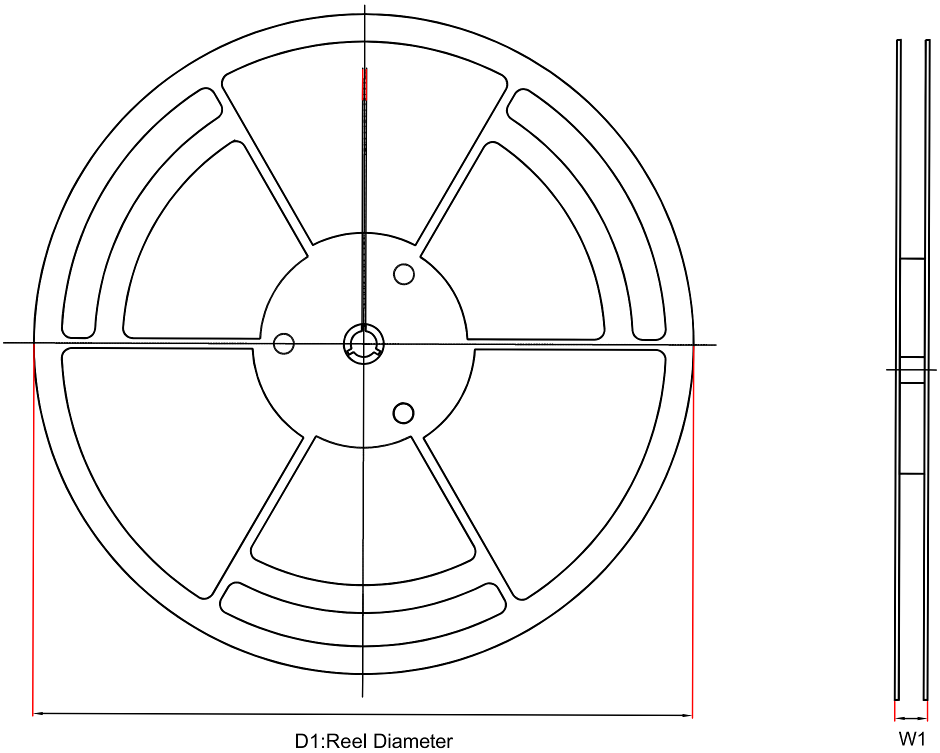
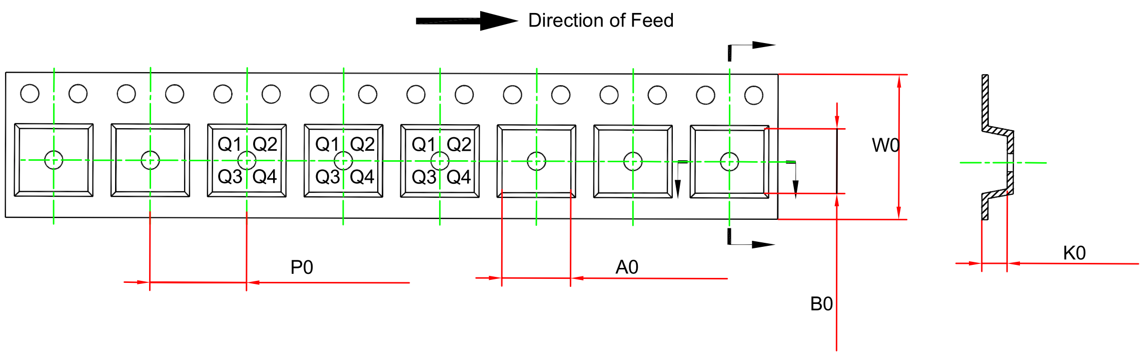


Figure 7. TPT1462Q Typical Application Circuit

Tape and Reel Information



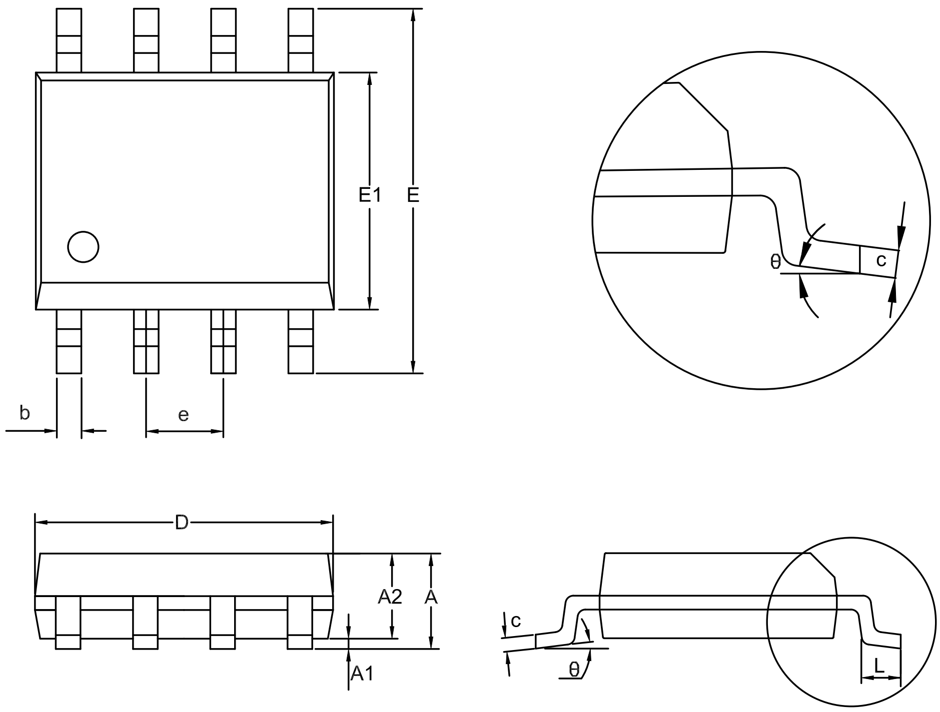


Order Number	Package	D1 (mm)	A0 (mm)	K0(mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPT1462VQ-SO1R-S	SOP8	330	6.5	2	12	17.6	5.4	8	Q1
TPT1462VQ-DFCR-S	DFN3x3-8	330	3.3	1.1	12	17.6	3.3	8	Q1
TPT1462Q-SO1R-S	SOP8	330	6.5	2	12	17.6	5.4	8	Q1
TPT1462Q-DFCR-S	DFN3x3-8	330	3.3	1.1	12	17.6	3.3	8	Q1

Package Outline Dimensions

SOP8

Package Outline Dimensions SO1(SOP-8-A)



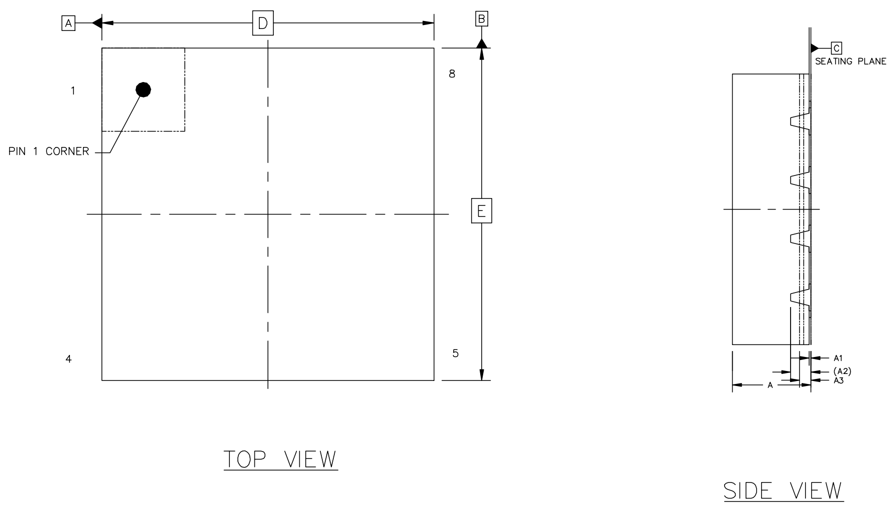
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

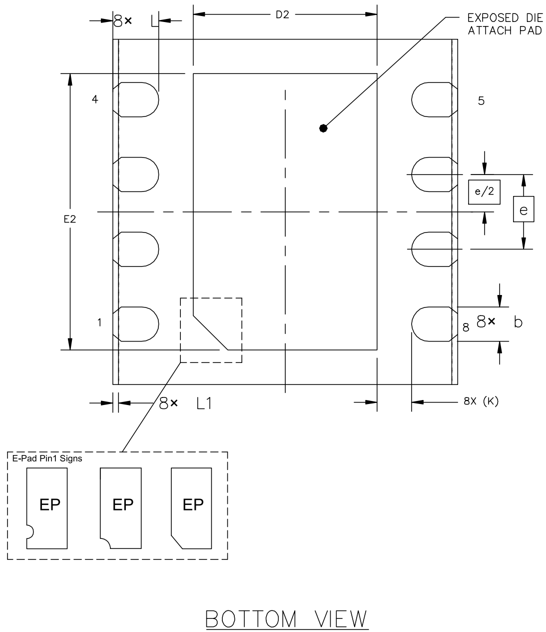
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN3X3-8

Package Outline Dimensions DFC(DFN3X3-8-WET-H)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
A2	0.150	0.250	0.006	0.010
A3	0.080	0.180	0.003	0.007
D	2.900	3.100	0.114	0.122
D2	1.500	1.700	0.059	0.067
E	2.900	3.100	0.114	0.122
b	0.250	0.350	0.010	0.014
E2	2.300	2.500	0.091	0.098
e	0.650 BSC		0.026 BSC	
L	0.350	0.450	0.014	0.018
L1	0.010	0.090	0.0004	0.004
K	0.300 REF		0.012 REF	

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT1462VQ-SO1R-S	−40 to 125°C	SOP8	T62VQ	MSL1	Tape and Reel, 4000	Green
TPT1462VQ-DFCR-S	−40 to 125°C	DFN3x3-8	T62VQ	MSL1	Tape and Reel, 4000	Green
TPT1462Q-SO1R-S	−40 to 125°C	SOP8	T162Q	MSL1	Tape and Reel, 4000	Green
TPT1462Q-DFCR-S	−40 to 125°C	DFN3x3-8	T162Q	MSL1	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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