

# Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

## Features

- Meets the ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5 and SAE J1939-14 Physical Layer Standards
- Supports Classical CAN and Optimized CAN FD up to 8 Mbps Data Rates
- Short and Symmetrical Propagation Delay and Fast Loop Delay for Enhanced Timing Margin
- 5 V Power Supply, I/O Voltage Range Supports 1.7 V to 5.5 V MCU Interface
- Support Partial Networking by Means of Selective Wake Up/Wake-Up Frame with INH Output
- SPI for Device Configuration and Status Retrieving
- Ideal Passive Behavior to CAN Bus when Unpowered
- Common-Mode Input Voltage:  $\pm 12$  V
- Protection Feature:
  - IEC 61000-4-2 ESD Protection up to  $\pm 6$  kV
  - Bus Fault Protection:  $\pm 45$  V
  - VCC Undervoltage Protection
  - TXD Dominant Time-Out Function and Bus-Dominant Time-Out Function
  - Thermal Shutdown Protection
- Available in SOP14 Package and DFN4.5X3-14 Package with Improved Automated Optical Inspection (AOI) Capability
- AEC-Q100 Qualified for Automotive Application, Grade 1

## Applications

- All Devices Supporting Highly Loaded CAN Networks
- Automotive and Transportation
  - Body Electronics / Lighting
  - Power Train / Chassis
  - Infotainment / Cluster
  - ADAS / Safety

## Description

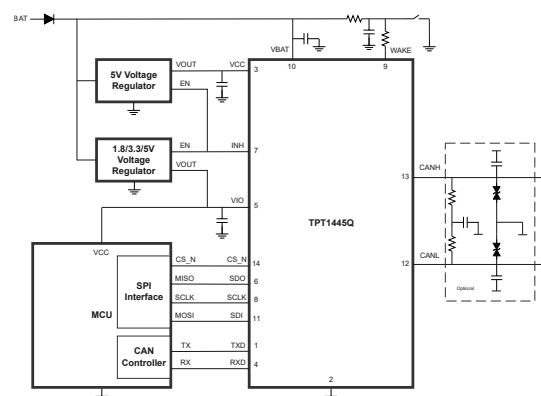
The TPT1445Q is a CAN transceiver that meets the ISO11898-2:2024, SAEJ2284-1 to SAE J2284-5, and SAE J1939-14 high-speed CAN (Controller Area Network) physical layer standard.

The devices are designed to be used in CAN FD networks up to 8 Mbps with enhanced timing margin and higher data rates in long and highly loaded networks, and support up to 8-Mbps data rates in simple CAN bus networks. The system design could be optimized with excellent electromagnetic compatibility (EMC) and electrostatic discharge (ESD) performance. The TPT1445Q has a secondary power supply input VIO pin for I/O level shifting to support 1.8 V, 2.5 V, 3.3 V, and 5 V MCU logic levels directly. The device supports selective wake up and enables the Electronic Control Unit (ECU) to implement the partial networking function which is operating in an active state while it is in a low-power sleep mode. The device comes with the standby mode, which can be waked up from the CAN bus, and ultra-low power management controls the ECU in standby and sleep modes, then enable the power supply by inhibiting output through the local or remote wake-up via wake-up pattern (WUP) or wake-up frame (WUF) which is defined in ISO11898-2:2024.

As designed, the devices feature bus fault protection from  $-45$  V to  $+45$  V, TXD dominant time-out (DTO), and over-temperature protection (OTP). Additionally, all devices include power-off ideal passive behavior fail-safe features to enhance the network robustness.

TPT1445Q is available in SOP14 and DFN4.5X3-14 packages and is characterized from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

## Typical Application Circuit



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**Automotive Fault Protected High-Speed CAN FD Transceiver for  
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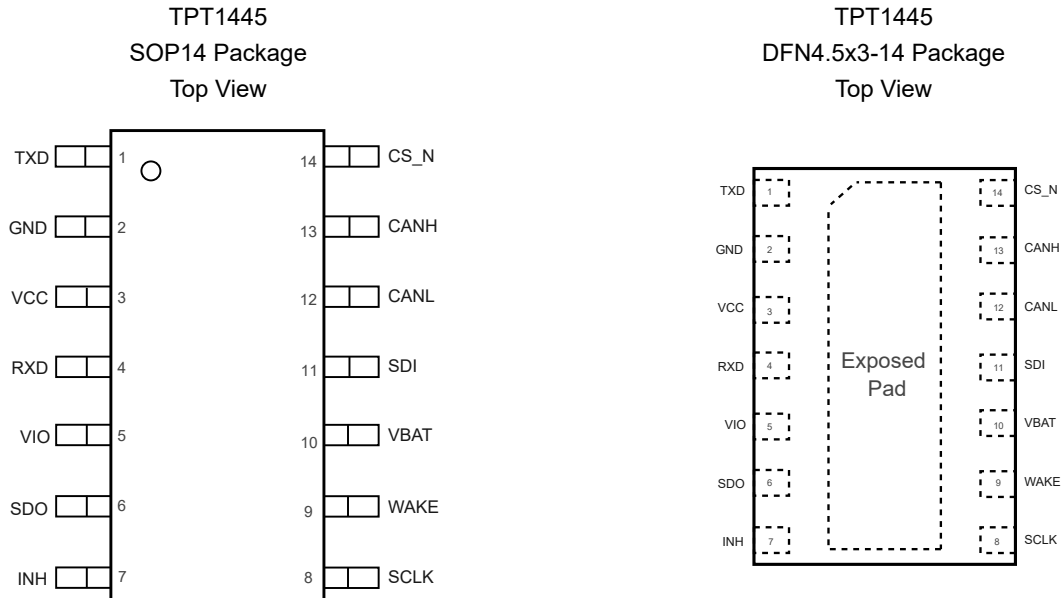
Order Number	VCC (V)	VIO (V)	BUS Protection (V)	Package
TPT1445Q-SO2R-S	4.5 to 5.5	1.7 to 5.5	±45	SOP14
TPT1445Q-DFKR-S	4.5 to 5.5	1.7 to 5.5	±45	DFN4.5X3-14

**Revision History**

Date	Revision	Notes
2023-11-12	Rev.Pre.0	Initial version.
2025-03-12	Rev.A.0	Released version.
2025-12-3	Rev.A.1	Corrected typos for some descriptions. Deleted the configuration information and description of the 0x55 register. Added Example Board Layout. The actual product remains unchanged.

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## Pin Configuration and Functions



**Table 1. Pin Functions: TPT1445**

Pin		I/O	Description
No.	Name		
1	TXD	Digital input	CAN transmit data input (low to drive dominant state and high to drive recessive state on CAN bus).
2	GND	GND	Ground, must be soldered to board ground.
3	VCC	Power	5-V CAN transceiver supply voltage.
4	RXD	Digital output	CAN receive data output (low for dominant and high for recessive bus states), output voltage adapted to the VIO input voltage.
5	VIO	Power	Supply voltage for Digital I/O level adaptor.
6	SDO	Digital output	SPI Serial data output, tri-state when CS_N is high.
7	INH	High voltage output	Inhibit pin to control external system voltage supplies.
8	SCLK	Digital input	SPI clock input.
9	WAKE	High voltage input	Local wake-up input.
10	VBAT	High voltage Power	High-voltage battery supply.
11	SDI	Digital input	SPI Serial data input.
12	CANL	Bus I/O	Low-level CAN bus line.
13	CANH	Bus I/O	High-level CAN bus line.
14	CS_N	Digital input	SPI Chip select input, active low.
	Exposed pad	GND	Thermal pad of DFN package, for enhanced thermal and electrical performance, it is required to solder the exposed pad to Ground.

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### Specifications

#### Absolute Maximum Ratings <sup>(1)</sup>

Parameter		Min	Max	Unit
V <sub>BAT</sub>	Battery Supply Voltage Range	-0.3	45	V
V <sub>CC</sub>	Power Supply Voltage Range	-0.3	7	V
V <sub>IO</sub>	I/O Level-Shifting Voltage Range	-0.3	7	V
V <sub>BUS</sub>	CAN Bus I/O Voltage Range (CANH, CANL)	-45	45	V
V <sub>BUS_DIFF</sub>	Differential Voltage of CAN Bus (CANH - CANL)	-45	45	V
V <sub>LOGIC</sub>	Logic Input and Output Terminal Voltage Range (TXD, RXD, SDI, SDO, SCLK, CS_N)	-0.3	7	V
V <sub>WAKE</sub>	WAKE Input Pin Voltage Range	-18	40	V
V <sub>INH</sub>	INH Output Pin Voltage Range	-18	40	V
I <sub>O_LOGIC</sub>	RXD Output Current	-4	4	mA
I <sub>O_INH</sub>	INH Output Current	-180	180	μA
T <sub>J</sub>	Maximum Junction Temperature	-40	150	°C
T <sub>STG</sub>	Storage Temperature Range	-65	150	°C
T <sub>OTW</sub>	Over-Temperature Warning Junction Temperature	-	146	°C
T <sub>OTP</sub>	Over-Temperature Protection Junction Temperature	-	188	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

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### ESD (Electrostatic Discharge Protection)

Parameter		Condition	Minimum Level	Unit
IEC	IEC Contact Discharge	IEC-61000-4-2, Bus Pin	±6	kV
HBM	Human Body Model ESD	Human Body Model (HBM) on all pins, per AEC Q100-002	±8	kV
CDM	Charged Device Model ESD	Charged Device Model (CDM) on all pins, per AEC Q100-011	±1.5	kV
V <sub>tran</sub>	ISO7637-2 transients per IEC 62228-3, CANH, CANL, WAKE, VBAT	Pulse 1	-100	V
		Pulse 2a	75	V
		Pulse 3a	-150	V
		Pulse 3b	100	V

### Recommended Operating Conditions

Description		Min	Max	Unit
V <sub>BAT</sub>	Battery Supply Voltage Range	4.5	40	V
V <sub>IO</sub>	Input/Output Voltage (TXD, RXD, SPI)	1.7	5.5	V
V <sub>CC</sub>	CAN Transceiver Power Supply	4.5	5.5	V
I <sub>OH_RXD</sub>	RXD Terminal HIGH Level Output Current	-4	-	mA
I <sub>OL_RXD</sub>	RXD Terminal LOW Level Output Current	-	4	mA
I <sub>O_INH</sub>	INH Output Current	-	180	µA
T <sub>A</sub>	Operating Ambient Temperature	-40	125	°C

### Thermal Information

Package Type	θ <sub>JA</sub>	θ <sub>Jc</sub>	Unit
SOP14	65.2	34.1	°C/W
DFN4.5x3-14	38.4	33.2	°C/W

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

### Electrical Characteristics

All test conditions:  $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{IO} = 1.7\text{ V to }5.5\text{ V}$ ,  $V_{BAT} = 4.5\text{ V to }40\text{ V}$ ,  $R_L = 60\ \Omega$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$ , unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Pin VBAT (Supply from Battery)</b>						
$V_{BAT\_R}$	Power-on Detection on VBAT for Protected Mode	$V_{BAT}$ rising	4.2	-	4.5	V
$V_{BAT\_F}$	Power-off Detection on VBAT for Protected Mode	$V_{BAT}$ falling	2.75	-	3	V
$UV_{BAT\_R}$	Undervoltage Recovery on VBAT for Protected Mode	$V_{BAT}$ rising	4.5	-	5	V
$UV_{BAT\_F}$	Undervoltage Detection on VBAT for Protected Mode	$V_{BAT}$ falling	4.2	-	4.5	V
$V_{HYS\_UVBAT}$	Hysteresis Voltage on $UV_{BAT}$ <sup>(1)</sup>		-	300	-	mV
$I_{BAT}$	Battery Supply Current	Normal mode	-	0.46	1	mA
		Sleep mode, CAN Offline Mode, $4.5\text{ V} \leq V_{BAT} \leq 40\text{ V}$	-	49	73	$\mu\text{A}$
		Standby mode, CAN Offline Mode, $4.5\text{ V} \leq V_{BAT} \leq 40\text{ V}$	-	54	91	$\mu\text{A}$
		Additional current in CAN Offline Bias Mode, CAN bus is connected to 2.5 V	-	47	70	$\mu\text{A}$
		Additional current in CAN Offline Bias Mode when selective wake is enabled and CAN bus active <sup>(1)</sup>	-	0.5	2	mA
		Additional current from WAKE input <sup>(1)</sup>	-	0.05	0.1	$\mu\text{A}$
<b>Pin VCC (Power Supply)</b>						
$V_{CC}$	Supply Voltage		4.5	-	5.5	V
$UV_{VCC\_R}$	Undervoltage Recovery on $V_{CC}$ for Protected Mode	$V_{CC}$ Rising	-	4.6	4.8	V
$UV_{VCC\_F}$	Undervoltage Detection on $V_{CC}$ for Protected Mode	$V_{CC}$ Falling	4.25	4.4	-	V
$V_{HYS\_UVVCC}$	Hysteresis Voltage on $UV_{VCC}$ <sup>(1)</sup>		-	200	-	mV
$I_{CC}$	Supply Current	Normal mode (recessive), $V_{TXD} = V_{IO}$ , $R_L = 60\ \Omega$ , $C_L = \text{open}$	-	1.8	3	mA

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Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
		Normal mode (dominant), $V_{TXD} = 0\text{ V}$ , $R_L = 60\ \Omega$ , $C_L =$ open	-	40	58	mA
		Standby/Normal mode, CAN inactive, $V_{TXD} = V_{CC}$ , selective wake off, $R_L = 60\ \Omega$ , $C_L =$ open	-	1.8	4	$\mu\text{A}$
		Sleep mode, CAN inactive, $V_{TXD} = V_{CC}$ , $R_L = 60\ \Omega$ , $C_L =$ open	-	1.8	4	$\mu\text{A}$
		Dominant with bus fault, short circuit on bus line, $V_{TXD} = 0\text{ V}$ , $-3\text{ V} < (V_{CANH} = V_{CANL}) < +18$ $\text{V}$ , $R_L = \text{Open}$ , $C_L = \text{open}$	-	80	110	mA
<b>Pin VIO (I/O Supply)</b>						
$V_{IO}$	Supply Voltage on $V_{IO}$ Pin		1.7	-	5.5	V
$UV_{VIO\_R}$	Undervoltage Recovery on $V_{IO}$ for Protected Mode	$V_{IO}$ Rising	-	-	1.65	V
$UV_{VIO\_F}$	Undervoltage Detection on $V_{IO}$ for Protected Mode	$V_{IO}$ Falling	1.25	-	-	V
$V_{HYS\_UVVI}$ O	Hysteresis Voltage on $UV_{VIO}$ for Protected Mode <sup>(1)</sup>		-	50	-	mV
$I_{IO}$	Supply Current from VIO	Normal and Standby mode, $V_{TXD} = V_{IO}$	-	1.2	3	$\mu\text{A}$
		Sleep mode	-	1.1	3	$\mu\text{A}$
<b>Pin SDI, SCLK, CS_N (Serial Peripheral Interface Inputs)</b>						
$V_{IH\_SPI}$	High-Level Input Voltage	$1.7\text{ V} \leq V_{IO} \leq 5.5\text{ V}$	$0.7 \times$ $V_{IO}$	-	-	V
$V_{IL\_SPI}$	Low-Level Input Voltage	$1.7\text{ V} \leq V_{IO} \leq 5.5\text{ V}$	-	-	$0.3 \times$ $V_{IO}$	
$V_{HYS\_SPI}$	Hysteresis Voltage on SPI Inputs <sup>(1)</sup>	$1.7\text{ V} \leq V_{IO} \leq 5.5\text{ V}$	$0.05 \times$ $V_{IO}$	-	-	V
$C_{IN}$	Input Capacitance <sup>(1)</sup>	At 20 MHz	4	-	15	pF
$R_{PD\_SCLK}$	SCLK Pin Pull-Down Resistance		40	60	80	k $\Omega$
$R_{PU\_CSN}$	CS_N Pin Pull-Up Resistance		40	60	80	k $\Omega$
$R_{PD\_SDI}$	SDI Pin Pull-Down Resistance		40	60	80	k $\Omega$
$R_{PU\_SDI}$	SDI Pin Pull-Up Resistance		40	60	80	k $\Omega$
<b>Pin SDO (Serial Peripheral Interface Outputs)</b>						
$V_{OH\_SPI}$	High-Level Output Voltage	$2.85\text{ V} \leq V_{IO} \leq 5.5\text{ V}$ , $I_{OH} = -4$ mA or $1.7\text{ V} \leq V_{IO} < 2.85\text{ V}$ , $I_{OH} = -2\text{ mA}$	$V_{IO} -$ 0.4	-	-	V

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Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	
V <sub>OL_SPI</sub>	Low-Level Output Voltage	2.85 V ≤ V <sub>IO</sub> ≤ 5.5 V, I <sub>OL</sub> = 4 mA or 1.7 V ≤ V <sub>IO</sub> < 2.85 V, I <sub>OL</sub> = 2 mA	-	-	0.4	V	
I <sub>LKG_OFF</sub>	Unpowered Leakage Current	V <sub>CS_N</sub> = V <sub>IO</sub> , 0 V ≤ V <sub>O</sub> ≤ V <sub>IO</sub>	-5	-	5	μA	
<b>Pin INH (Inhibit high voltage output)</b>							
V <sub>O_INH</sub>	High-Level Output Voltage	I <sub>INH</sub> = -180 μA	V <sub>BAT</sub> - 0.8	-	V <sub>BAT</sub>	V	
R <sub>PD_INH</sub>	INH Pin Pull-Down Resistance	Sleep mode	3	4	5	MΩ	
<b>Pin TXD (CAN transmit data input)</b>							
V <sub>IH_TXD</sub>	High-Level Input Voltage	1.7 V ≤ V <sub>IO</sub> ≤ 5.5 V	0.7 x V <sub>IO</sub>	-	-	V	
V <sub>IL_TXD</sub>	Low-Level Input Voltage	1.7 V ≤ V <sub>IO</sub> ≤ 5.5 V	-	-	0.3 x V <sub>IO</sub>	V	
V <sub>HYS_TXD</sub>	Hysteresis Voltage on TXD Inputs	1.7 V ≤ V <sub>IO</sub> ≤ 5.5 V	0.05 x V <sub>IO</sub>	-	-	V	
R <sub>PU_TXD</sub>	TXD Pin Pull-Up Resistance		40	60	80	kΩ	
<b>Pin RXD (CAN Receive Data Output)</b>							
V <sub>OH_RXD</sub>	High-Level Output Voltage	2.85 V ≤ V <sub>IO</sub> ≤ 5.5 V, I <sub>OH</sub> = -4 mA or 1.7 V ≤ V <sub>IO</sub> < 2.85 V, I <sub>OH</sub> = -2 mA	V <sub>IO</sub> - 0.4	-	-	V	
V <sub>OL_RXD</sub>	Low-Level Output Voltage	2.85 V ≤ V <sub>IO</sub> ≤ 5.5 V, I <sub>OL</sub> = 4 mA or 1.7 V ≤ V <sub>IO</sub> < 2.85 V, I <sub>OL</sub> = 2 mA	-	-	0.4	V	
R <sub>PU_RXD</sub>	RXD Pin Pull-Up Resistance		40	60	80	kΩ	
<b>Pin WAKE (Local wake-up pin)</b>							
V <sub>IH_WAKE</sub>	High-Level Input Voltage		3	-	3.8	V	
V <sub>IL_WAKE</sub>	Low-Level Input Voltage		2.5	-	3.4	V	
V <sub>HYS_WAKE</sub>	Hysteresis Voltage on WAKE Inputs <sup>(1)</sup>		250	325	800	mV	
I <sub>IL</sub>	Low-Level Input Current		-	-	1.5	μA	
<b>Pin CANH, CANL (CAN Bus lines)</b>							
V <sub>O(DOM)</sub>	Dominant Bus Output Voltage	CANH	CAN active mode, V <sub>TXD</sub> = 0 V, 50 Ω ≤ R <sub>L</sub> ≤ 65 Ω, C <sub>L</sub> = open, t < t <sub>to(dom)TXD</sub>	2.75	3.5	4.5	V
		CANL		0.5	1.5	2.25	V
V <sub>SYM_DC</sub>	DC Output Symmetry (dominant or recessive) (V <sub>CC</sub> - V <sub>O(CANH)</sub> - V <sub>O(CANL)</sub> )		4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V, R <sub>L</sub> = 60 Ω, C <sub>L</sub> = open,	-0.4	-	0.4	V
V <sub>SYM</sub>	Transient Symmetry (dominant or recessive) (V <sub>O(CANH)</sub> + V <sub>O(CANL)</sub> ) / V <sub>CC</sub> <sup>(1)</sup>		4.75 V ≤ V <sub>CC</sub> ≤ 5.25 V, R <sub>L</sub> = 60 Ω, C <sub>L</sub> = open, C <sub>SPLIT</sub> = 4.7 nF, T <sub>XD</sub> = 250 kHz, 1 MHz, 2.5 MHz	0.9	1.0	1.1	V/V

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Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>OD_DOM</sub>	Differential Output Voltage (dominant)	CAN active mode, $t < t_{to(dom)TXD}$ , $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ , $V_{TXD} = 0\text{ V}$ , $50\ \Omega \leq R_L < 65\ \Omega$ , $C_L = \text{open}$	1.5	-	3	V
		CAN active mode, $t < t_{to(dom)TXD}$ , $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ , $V_{TXD} = 0\text{ V}$ , $45\ \Omega \leq R_L \leq 70\ \Omega$ , $C_L = \text{open}$	1.4	-	3.3	V
		CAN active mode, $t < t_{to(dom)TXD}$ , $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ , $V_{TXD} = 0\text{ V}$ , $R_L = 2240\ \Omega$ , $C_L = \text{open}$	1.5	-	5.5	V
V <sub>OD_REC</sub>	Differential Output Voltage (recessive)	CAN active mode, Silentmode, $V_{TXD} = V_{IO}$ , no load	-50	-	50	mV
		CAN Offline mode, no load	-0.2	-	0.2	V
V <sub>O_REC</sub>	Recessive Output Voltage	CAN Active mode, $V_{TXD} = V_{IO}$ , no load	2	0.5 x V <sub>CC</sub>	3	V
		CAN Offline mode; no load	-0.1	-	0.1	V
		CAN Offline Bias and Silent mode; no load; $V_{CC} = 0\text{ V}$	2	2.5	3	V
I <sub>O_SC_DOM</sub>	Dominant Short-Circuit Output Current	CANH CAN active mode, $-15\text{ V} \leq V_{CANH} \leq 27\text{ V}$ , CANL = open, $V_{TXD} = 0\text{ V}$	-115	-	-	mA
		CANL CAN active mode, $-15\text{ V} \leq V_{CANL} \leq 27\text{ V}$ , CANH = open, $V_{TXD} = 0\text{ V}$	-	-	115	mA
I <sub>O_SC_REC</sub>	Recessive Short-Circuit Output Current	$-27\text{ V} \leq V_{CANH} / V_{CANL} \leq 32\text{ V}$ , $V_{TXD} = V_{CC}$ , normal modes	-5	-	5	mA
V <sub>TH_RX_DIF</sub>	Differential Receiver Threshold Voltage	CAN active mode or Silent mode $-12\text{ V} \leq V_{CANH} / V_{CANL} \leq 12\text{ V}$	0.5	0.7	0.9	V
		CAN offline mode, $-12\text{ V} \leq V_{CANH} / V_{CANL} \leq 12\text{ V}$	0.4	0.7	1.15	V
V <sub>REC_RX</sub>	Receiver Recessive Voltage <sup>(1)</sup>	CAN active mode or Silent mode, Bus bias active $-12\text{ V} \leq V_{CANH} / V_{CANL} \leq 12\text{ V}$	-4	-	0.5	V
		CAN offline mode, Bus bias inactive $-12\text{ V} \leq V_{CANH} / V_{CANL} \leq 12\text{ V}$	-4	-	0.4	V
V <sub>DOM_RX</sub>	Receiver Dominant Voltage <sup>(1)</sup>	CAN active mode or Silent mode, Bus bias active	0.9	-	9	V

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
		$-12\text{ V} \leq V_{\text{CANH}} / V_{\text{CANL}} \leq 12\text{ V}$				
		CAN offline mode, Bus bias inactive $-12\text{ V} \leq V_{\text{CANH}} / V_{\text{CANL}} \leq 12\text{ V}$	1.15	-	9	V
$V_{\text{HYS\_RX\_DIFF}}$	Differential Receiver Hysteresis Voltage (1)	CAN active mode or Silent mode, $-12\text{ V} \leq V_{\text{CANH}} / V_{\text{CANL}} \leq 12\text{ V}$	50	100	200	mV
$R_{\text{IN}}$	Input Resistance (CANH or CANL)	$V_{\text{TXD}} = V_{\text{CC}} = V_{\text{IO}} = 5\text{ V}$ , $-2\text{ V} \leq V_{\text{CANH}} / V_{\text{CANL}} \leq 7\text{ V}$	8	16	28	k $\Omega$
$R_{\text{IN\_M}}$	Input Resistance Matching: $[1 - R_{\text{IN(CANH)}} / R_{\text{IN(CANL)}}] \times 100\%$	$V_{\text{TXD}} = V_{\text{CC}} = V_{\text{IO}} = 5\text{ V}$	-1	-	+1	%
$R_{\text{ID}}$	Differential Input Resistance	$V_{\text{TXD}} = V_{\text{CC}} = V_{\text{IO}} = 5\text{ V}$ , $-2\text{ V} \leq V_{\text{CANH}} / V_{\text{CANL}} \leq 7\text{ V}$	16	32	56	k $\Omega$
$C_{\text{i}}$	Input Capacitance to Ground (CANH or CANL) (1)		-	-	20	pF
$C_{\text{ID}}$	Differential Input Capacitance (1)		-	-	10	pF
$I_{\text{L}}$	Leakage Current	$V_{\text{BAT}} = V_{\text{CC}} = 0\text{ V}$ or $V_{\text{BAT}} = V_{\text{CC}}$ shorted to ground via 47 k $\Omega$ ; $V_{\text{CANH}} = 5\text{ V}$ , $V_{\text{CANL}} = 5\text{ V}$	-10	-	10	$\mu\text{A}$
<b>Temperature Protection</b>						
$T_{\text{TH\_ACT\_OTP}}$	Overtemperature Protection Activation Threshold Temperature		167	177	197	$^{\circ}\text{C}$
$T_{\text{TH\_REL\_OTP}}$	Overtemperature Protection Release Threshold Temperature		127	137	157	$^{\circ}\text{C}$
$T_{\text{TH\_WARN\_OTP}}$	Overtemperature Protection Warning Threshold Temperature		127	137	157	$^{\circ}\text{C}$

(1) The typical data is based on bench test and design simulation.  $V_{\text{sym}} = 0.9 \sim 1.1\text{ V/V}$  at 250 kbps.

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

### AC Timing Requirements

All test conditions:  $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{IO} = 1.7\text{ V to }5.5\text{ V}$ ,  $V_{BAT} = 4.5\text{ V to }40\text{ V}$ ,  $R_L = 60\ \Omega$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$ , unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Pin BAT, VCC, VIO (Power Supply)</b>						
$t_{PWRUP}$	Power-up Time	Time from $V_{BAT}$ exceeding the power-on detection threshold ( $V_{BAT\_R}$ ) until INH active	-	3	4.7	ms
$t_{d\_UV}$	Under Voltage Detection Delay Time		6	-	54	$\mu\text{s}$
$t_{d\_UVSLP}$	Delay from Undervoltage Detection to Sleep Mode <sup>(1)</sup>	Time from $U_{VCC}$ and/or $U_{VIO}$ event until transition to Sleep mode	200	-	400	ms
<b>Pin CS_N, SCLK, SDI, SDO (SPI Timing)</b>						
$f_{SCLK}$	SPI Clock Frequency <sup>(1)</sup>	Normal, Standby mode, Sleep mode	-	-	4	MHz
$t_{SCLK}$	SPI Clock Period <sup>(1)</sup>	Normal, Standby mode, Sleep mode	250	-	-	ns
$t_{CSS}$	SPI Chip Select Setup Time <sup>(1)</sup>	Normal and Standby mode	100	-	-	ns
		Sleep mode	500	-	-	ns
$t_{CSH}$	SPI Chip Select Hold Time <sup>(1)</sup>	Normal and Standby mode	100	-	-	ns
		Sleep mode	500	-	-	ns
$t_{CLK\_H}$	SPI Clock High Time <sup>(1)</sup>	Normal and Standby mode	100	-	-	ns
		Sleep mode	500	-	-	ns
$t_{CLK\_L}$	SPI Clock Low Time <sup>(1)</sup>	Normal and Standby mode	100	-	-	ns
		Sleep mode	500	-	-	ns
$t_{DI\_SU}$	SPI Data Input Setup Time <sup>(1)</sup>	Normal and Standby mode	50	-	-	ns
		Sleep mode	200	-	-	ns
$t_{DI\_H}$	SPI Data Input Hold Time <sup>(1)</sup>	Normal and Standby mode	50	-	-	ns
		Sleep mode	200	-	-	ns
$t_{DO\_V}$	SPI Data Output Valid Time <sup>(1)</sup>	pin SDO; $C_L = 20\text{ pF}$ ; Normal and Standby modes	-	-	100	ns
		pin SDO; $C_L = 20\text{ pF}$ ; Sleep modes	-	-	100	ns
$t_{d\_SDI-SDO}$	SDI to SDO Delay Time <sup>(1)</sup>	SPI address bits and read-only bit; $C_L = 20\text{ pF}$	-	-	50	ns
$t_{CS\_WH}$	SPI Chip Select Pulse Width High <sup>(1)</sup>	pin SDO; Normal and Standby modes	250	-	-	ns
		pin SDO; Sleep mode	1	-	-	$\mu\text{s}$

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d\_SCLKL-CSL}$	Delay Time from SCLK Low to CS_N Low <sup>(1)</sup>		50	-	-	ns
<b>Transceiver Switching Characteristics</b>						
$t_{pLD}$	Propagation Delay Time, Low TXD to Driver Dominant (recessive to dominant) <sup>(1)</sup>	Normal mode, $R_L = 60 \Omega$ , $C_L = 100 \text{ pF}$	-	60	100	ns
$t_{pHR}$	Propagation Delay Time, High TXD to Driver Recessive (dominant to recessive) <sup>(1)</sup>		-	60	100	ns
$t_{SK\_P}$	Pulse Skew ( $ t_{pHR} - t_{pLD} $ ) <sup>(1)</sup>		-	10	35	ns
$t_R$	Differential Output Signal Rise Time <sup>(1)</sup>		-	45	-	ns
$t_F$	Differential Output Signal Fall Time <sup>(1)</sup>		-	32	-	ns
$t_{pRH}$	Propagation Delay Time, Bus Recessive Input to RXD High Output (Dominant to Recessive) <sup>(1)</sup>	$V_{STB} = 0 \text{ V}$ , $C_{L(RXD)} = 15 \text{ pF}$	-	90	120	ns
$t_{pDL}$	Propagation Delay Time, Bus Dominant Input to RXD Low Output (Recessive to Dominant) <sup>(1)</sup>		-	90	120	ns
$t_{R\_R}$	RXD Output Signal Rise Time <sup>(1)</sup>		-	9	-	ns
$t_{R\_F}$	RXD Output Signal Fall Time <sup>(1)</sup>		-	9	-	ns
$t_{PROP\_TXDL-RXD}$	Total loop delay, driver input (TXD) low to receiver output (RXD) low, recessive to dominant		Normal mode, $R_L = 60 \Omega$ , $C_L = 100 \text{ pF}$ , $C_{L(RXD)} = 15 \text{ pF}$	-	140	255
$t_{PROP\_TXDH-RXD}$	Total loop delay, driver input (TXD) high to receiver output (RXD) high, dominant to recessive	Normal mode, $R_L = 60 \Omega$ , $C_L = 100 \text{ pF}$ , $C_{L(RXD)} = 15 \text{ pF}$	-	140	255	ns
<b>FD Timing Parameters</b>						
$t_{BIT\_BUS}$	Bit time on CAN bus output pins with $t_{BIT\_TXD} = 500 \text{ ns}$	$R_L = 60 \Omega$ , $C_L = 100 \text{ pF}$ , $C_{L(RXD)} = 15 \text{ pF}$ , $\Delta t_{REC} = t_{BIT\_RXD} - t_{BIT\_BUS}$	435	-	530	ns
	Bit time on CAN bus output pins with $t_{BIT\_TXD} = 200 \text{ ns}$		155	-	210	ns
$t_{BIT\_RXD}$	Bit time on RXD output pins with $t_{BIT\_TXD} = 500 \text{ ns}$		400	-	550	ns
	Bit time on RXD output pins with $t_{BIT\_TXD} = 200 \text{ ns}$		120	-	220	ns
$\Delta t_{REC}$	Receiver timing symmetry with $t_{BIT\_TXD} = 500 \text{ ns}$ <sup>(1)</sup>		-65	-	40	ns

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Receiver timing symmetry with $t_{\text{BIT\_TXD}} = 200 \text{ ns}^{(1)}$		-45	-	15	ns
$t_{\text{BIT\_BUS}}$	Bit time on CAN bus output pins with $t_{\text{BIT\_TXD}} = 125 \text{ ns}^{(1)}$	$R_L = 60 \Omega$ , $C_L = 100 \text{ pF}$ , $C_{L(\text{RXD})} = 15 \text{ pF}$ , $\Delta t_{\text{REC}} = t_{\text{BIT\_RXD}} - t_{\text{BIT\_BUS}}$ , $V_{\text{IO}} = 2.85 \text{ V to } 5.5 \text{ V}$	90	-	135	ns
$t_{\text{BIT\_RXD}}$	Bit time on RXD output pins with $t_{\text{BIT\_TXD}} = 125 \text{ ns}^{(1)}$		75	-	145	ns
$\Delta t_{\text{REC}}$	Receiver timing symmetry with $t_{\text{BIT\_TXD}} = 125 \text{ ns}^{(1)}$		-30	-	15	ns
<b>Device Timing Parameters</b>						
$t_{\text{WAKE\_BUS\_DOM}}$	Bus Time to Meet Filtered Bus Dominant Requirement for Wake-up Request	Pulse for wake-up on pins CANH and CANL	0.5	-	1.8	$\mu\text{s}$
$t_{\text{WAKE\_BUS\_REC}}$	Bus Time to Meet Filtered Bus Recessive Requirement for Wake-up Request	Pulse for wake-up on pins CANH and CANL	0.5	-	1.8	$\mu\text{s}$
$t_{\text{WAKE\_TO}}$	Bus Wake-up Time Out-time	Between first and second dominant pulses; CAN Offline mode	0.8	-	10	ms
$t_{\text{TXD\_DTO}}$	TXD dominant time-out time	normal mode, $R_L = 60 \Omega$ , $C_L = \text{open}$ , $V_{\text{TXD}} = 0\text{V}$	2.7	-	3.3	ms
$t_{\text{SILENCE}}$	Bus Silence time-out time <sup>(1)</sup>	Timeout for bus inactivity. Timer is reset and restarted when bus changes from dominant to recessive or vice versa.	0.95	-	1.2	s
$t_{\text{d\_ACT-BIAS}}$	Delay time form bus active to bias		-	-	200	$\mu\text{s}$
$t_{\text{SU\_CAN}}$	CAN start-up time	When switching to Active mode	-	-	220	$\mu\text{s}$
<b>CAN Partial Networking</b>						
$N_{\text{idle\_bits}}$	Number of idle bits <sup>(1)</sup>	Before a new SOF is accepted	6	-	10	
$t_{\text{fltr\_dom}}$	Dominant bit filter time <sup>(1)</sup>	arbitration data rate $\leq 500 \text{ kbps}$	5	-	8.75	%
<b>Pin RXD Interrupt/wake-up Timing</b>						
$t_{\text{d\_event}}$	Event capture delay time	CAN offline mode	0.9	-	1.1	ms
$t_{\text{blank}}$	Blanking time	Switching from Offline mode to Active or Silent mode	-	-	30	$\mu\text{s}$
<b>Pin WAKE</b>						
$t_{\text{WAKE}}$	Wake up time		50	-	-	$\mu\text{s}$
<b>Pin INH</b>						
$t_{\text{d\_BW-INH}}$	Delay time from bus wake-up to INH high		-	-	100	$\mu\text{s}$

(1) The test data is based on bench test and design simulation.

# Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

## Parameter Measurement Information

### Test Circuit

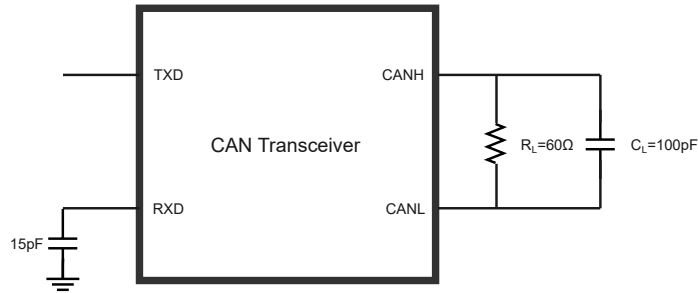


Figure 1. CAN Transceiver Timing Parameter Test Circuit

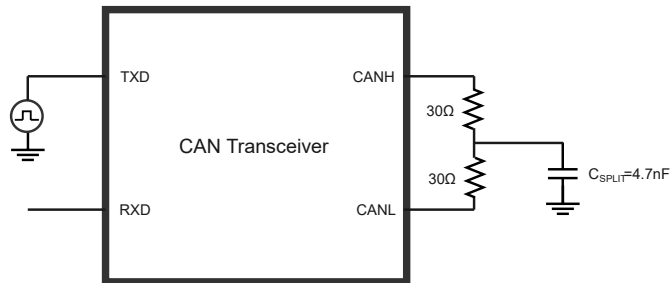


Figure 2. CAN Transceiver Driver Symmetry Test Circuit

# Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

## Parameter Diagram

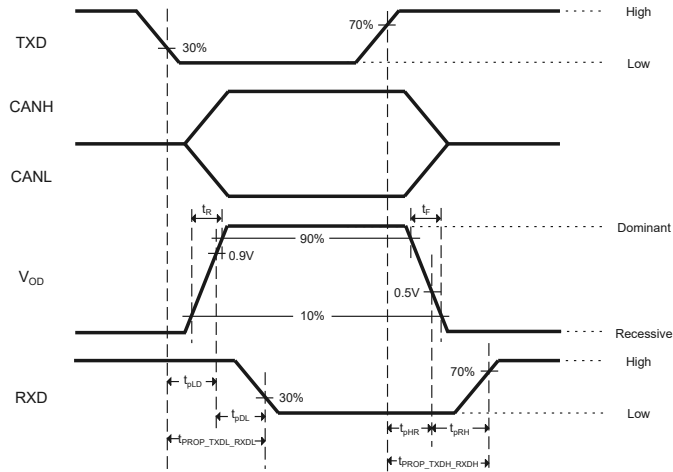


Figure 3. CAN Transceiver Timing Diagram

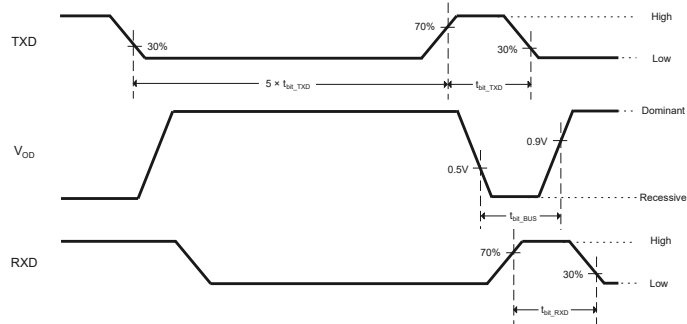


Figure 4. CAN FD Timing Parameter Diagram

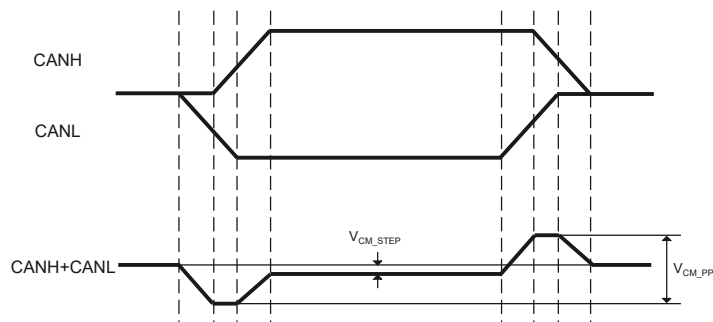


Figure 5. CAN Bus Common-Mode Voltage

Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

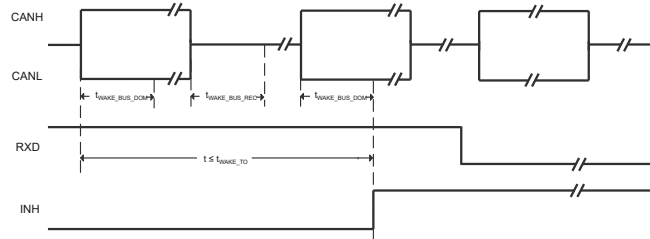


Figure 6. Wake-up Timing Diagram

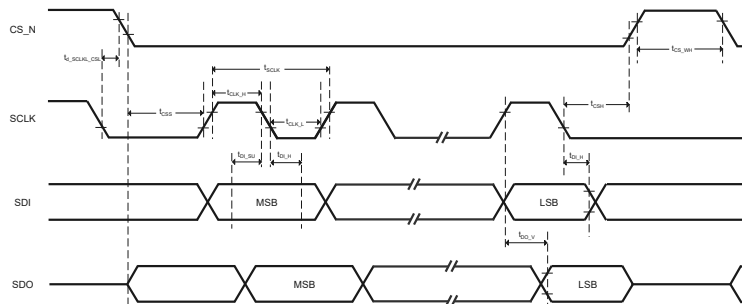


Figure 7. SPI Timing Parameter Diagram

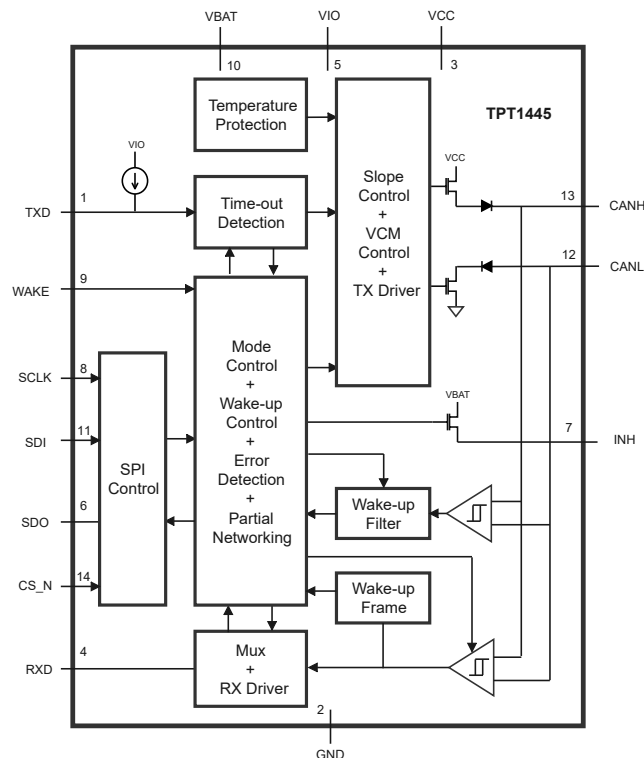
# Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

## Detailed Description

### Overview

The TPT1445 is a CAN transceiver which meets the ISO11898 High-Speed CAN (Controller Area Network) physical layer standard. The device is designed to be used in CAN FD networks up to 8 Mbps, with enhanced timing margins and higher data rates in long and highly loaded networks. As designed, the device features crosswire, overvoltage, and loss of ground protection from -45 V to +45 V, overtemperature shutdown, and a -12 V to +12 V common-mode input voltage range. The TPT1445 has a secondary power supply input for I/O level shifting the input pin thresholds and the RXD output level. A serial peripheral interface (SPI) is provided for configuration and status retrieval. TPT1445 supports selective wake up and enables the Electronic Control Unit (ECU) to implement the Partial Networking function which is operating in an active state while it is in a low-power sleep mode. The device comes with the standby mode, which can be waked up from CAN BUS, and ultra-low power management controls the ECU in standby and sleep modes, then enables the power supply by inhibiting output through the local or remote wake-up via wake-up pattern or wake-up frame identification. The TPT1445 includes many protection features to enhance device and network robustness. The TPT1445 is available in SOP14 and DFN4.5X3-14 packages, and is AEC-Q100 qualified for automotive applications.

### Functional Block Diagram



**Figure 8. Functional Block Diagram**

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

### Feature Description

**Table 2. Driver Function Table**

Device Mode	Inputs	Outputs		Driven BUS State
	TXD	CANH	CANL	
Normal	L	H	L	Dominant
	H or Open	Z	Z	Biased Recessive
Standby	X	Z	Z	Biased to GND
Silent	X	Z	Z	Biased to 2.5V
Sleep	X	Z	Z	Biased to GND

**Table 3. Receiver Function Table**

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	BUS State	RXD Terminal
Normal or Standby	$V_{ID} \geq V_{IT+(MAX)}$	Dominant	L
	$V_{IT-(MIN)} < V_{ID} < V_{IT+(MAX)}$	Indeterminate	Indeterminate
	$V_{ID} \leq V_{IT-(MIN)}$	Recessive	H
	Open ( $V_{ID} \approx 0\text{ V}$ )	Open	H

### System Controller Operating Modes

The device system controller has 5 operating modes: Off mode, Standby mode, Sleep mode, Normal mode, and Over-temperature mode.

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

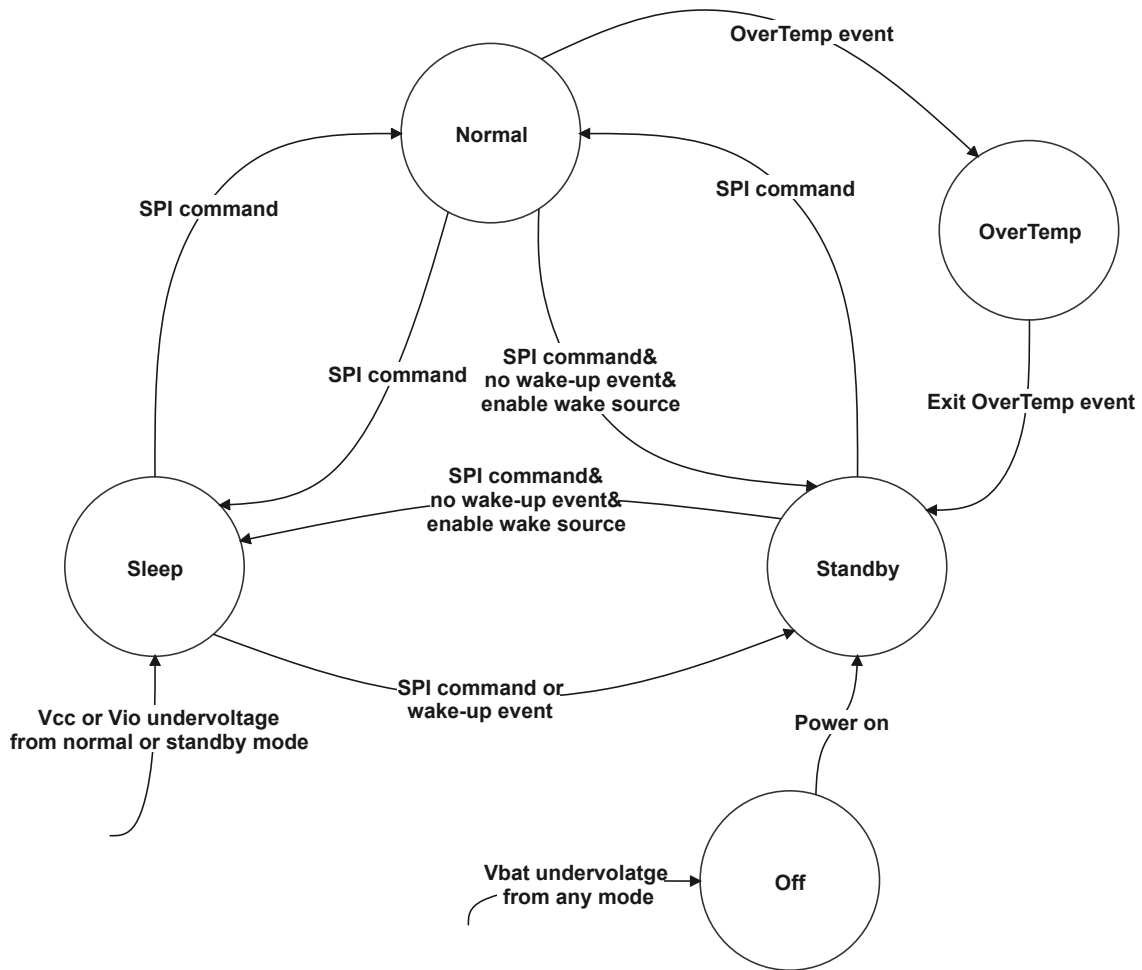


Figure 9. System Operating Mode Transition State Diagram

Table 4. System Operating Mode State Table

Function Module	Operation Mode				
	Off	Standby	Sleep	Normal	Over-temperature
SPI	Disabled	Enabled	Enabled if VIO is on	Enabled	Disabled
INH	High-Z	VBAT level	High-Z	VBAT level	VBAT level
CAN transceiver	Off	Offline or Offline bias	Offline or Offline bias	Active/Offline/Offline bias/Silent determined by CMC bits	Off
RXD	VIO level	VIO level/Low (wake-up event occurs)	VIO level/Low(wake-up event occurs)	Follow CAN bus status if CMC = 01/11/10, or the same as standby and sleep mode	VIO level/Low (wake-up event occurs)

---

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

### Normal Mode

This is the normal operating mode of the device. In the normal mode, the device is fully operational, and all blocks are available.

### Standby Mode

This is the first level of the low-power mode. In the standby mode, the driver and receiver of the CAN transceiver are disabled, and the device is unable to transmit or receive data. The low-power receiver monitors bus activity for valid wake-up requirements. The CAN bus pin is biased to the ground. The INH pin is active to enable the voltage regulator controlled by the INH pin. The pin RXD reflects active wake-up requests as  $V_{IO}$  and  $V_{BAT}$  are powered.

### Sleep Mode

This is the second level of low-power mode as well as the lowest power mode. In the sleep mode, the driver and receiver of the CAN transceiver are disabled, and the device is unable to transmit or receive data, the low-power receiver is monitoring bus activity for valid wake-up requirements. The CAN bus pin is biased to the ground. The INH pin is floating to disable the voltage regulator controlled by the INH pin for additional system-level power saving.

### Off Mode

This is the default mode when  $V_{BAT}$  is first powered, and the device switches to the off mode if  $V_{BAT}$  drops below the power-off threshold  $V_{BAT\_F}$ . The CAN bus pins and INH pin are in High-Z state in off mode. When  $V_{BAT}$  rises above the power on the threshold  $V_{BAT\_R}$ , the device reboots and switches to standby mode after  $t_{SU\_CAN}$ .

### Over-Temperature Mode

The over-temperature mode prevents the device from over-heated induced damage. The device switches to over-temperature mode as soon as the junction temperature rises above the over-temperature warning threshold  $T_{OTW}$ . The CAN driver and receiver are disabled, and CAN bus pins are High-Z state in over-temperature mode.

### High-Speed CAN Transceiver Operating Mode

The high-speed CAN transceiver has 4 operating modes: active mode, silent mode, offline mode, and Offline bias mode. Operating mode selection is made via register setting of bits CMC. The CAN transceiver operating mode can be selected among the offline mode, active mode, and silent mode via register setting in the normal mode. The CAN transceiver is forced to go into the offline mode or offline bias mode when the device is in the standby mode or sleep mode.

# Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

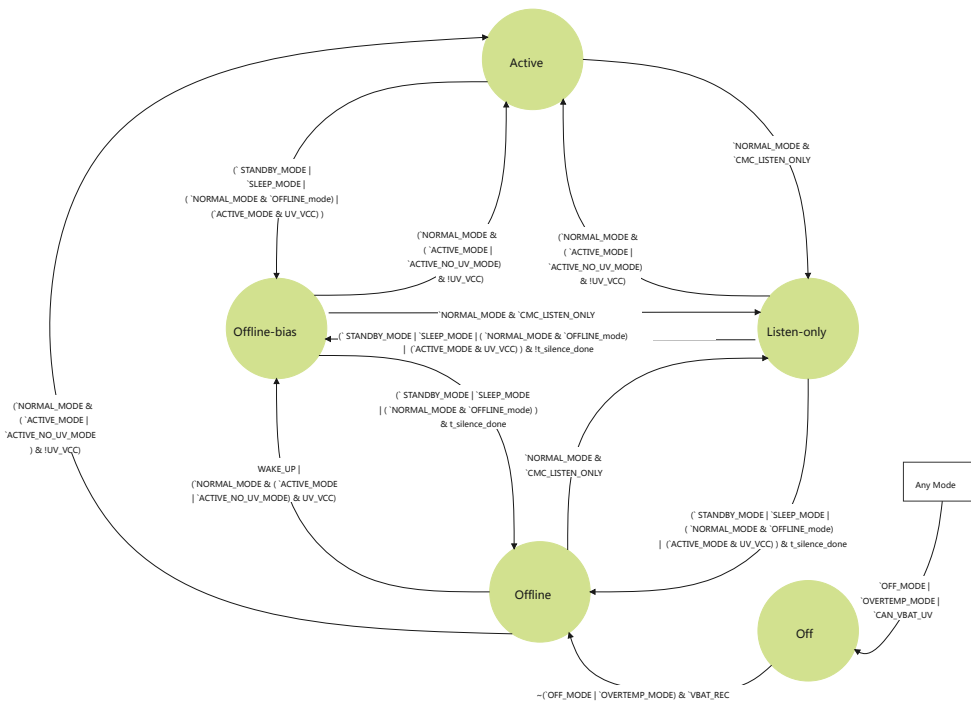


Figure 10. CAN Transceiver Operating Mode Transition State Diagram

### Active Mode

In the active mode, the CAN driver and receiver block are fully operational, the transceiver can transmit and receive data via the bus lines CANH and CANL. The driver translates the digital input data on the TXD pin to differential analog output on the CAN bus. The receiver translates the differential analog data on the CAN bus to digital data output to the RXD pin. The slopes of the CAN bus output signals are controlled by the internal circuit that optimizes the Electro Magnetic Emission (EME) performance.

### Silent Mode

This is the listen-only mode and receive-only mode of the device. In the silent mode, the driver is disabled, releasing the bus pins to a recessive state. All other blocks, including the receiver, continue to operate in the normal mode. The silent mode can be used to prevent a faulty CAN controller from disrupting CAN bus network communications.

### Offline Mode and Offline Bias Mode

The transceiver monitors the CAN bus for the wake-up event in the offline mode if the CAN wake-up detection function is enabled. The CAN bus is biased to ground. The transceiver monitors the CAN bus for the wake-up event in the offline mode if the CAN wake-up detection function is enabled. The CAN bus is biased to 2.5 V. The offline bias mode is activated automatically when the activity is detected on the CAN bus while the transceiver is in the CAN offline mode. The transceiver returns to the offline mode if there is no edge on the CAN bus for longer than  $t_{SILENCE}$ .

### Device Local Faults

#### TXD Dominant Time-out

The device is featured with the TXD dominant time-out detection function. This function prevents a permanent low on the TXD pin, resulting in the CAN bus being driven into permanent dominant, which causes the CAN bus network communication blocked. If the TXD remains low for longer than  $t_{TXD\_DTO}$ , the transmitter is disabled until the fault flag has been cleared.

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

### TXD Shorted to RXD Detection

The device is featured with the function of a short circuit between TXD and RXD detection. This function prevents the CAN bus from being locked in permanent dominance, which results in the CAN bus network communication being blocked. The transmitter is disabled until the fault flag has been cleared.

### Under-Voltage Lockout (UVLO)

The device integrates an under-voltage detect and lockout circuit of the supply terminal to keep the device in the protected mode if the supply voltage drops below the threshold until the supply voltage is higher than the UVLO threshold. This protects the device and system during under-voltage events on supply terminals.

If an undervoltage event occurs on the VCC/VIO pin and remains longer than the undervoltage detection delay time  $t_{d\_UVSLP}$ , the device is forced to sleep mode. To avoid deadlock, the device takes actions below:

All captured events in register 0x61 to 0x64 are cleared to guarantee reliable sleep.

Both CAN wake-up and Local wake-up (WPRE and WPFE) are enabled so that the device can be woken up and work normally.

Partial networking mode is disabled (CPNC=0 and CPNOK = 0) to ensure wake-up event efficiently by CAN bus communication.

State bit FSMS is set to indicate a force sleep event to the microcontroller.

### Over-Temperature Protection (OTP)

The device integrates over-temperature protection circuit to prevent the device from over-heated induced damage. When the junction temperature is higher than the over-temperature protection threshold  $T_{OTP}$ , the device shuts down until the junction temperature  $T_J$  drops below  $T_{OTW}$ .

### Diagnostic Interrupt

Both the wake-up event and diagnostic event are stored in register 0x60 to 0x64 and are signaled on the RXD pin to indicate microcontroller the status and interruption of the device. The description of the wake-up event and diagnostic event are listed below.

**Table 5. Wake-up Event Table**

Symbol	Event	Status After Power-on	Description
CW	CAN wake-up	disable	a Wake-up pattern or Wake-up frame detected on CAN bus
WPR	Wake pin rising	disable	a rising edge detected on WAKE pin
WPF	Wake pin falling	disable	a falling edge detected on WAKE pin

**Table 6. Diagnostic Event Table**

Symbol	Event	Status after Power-on	Description
PO	power-on	always enable	when Vbat voltage supplies

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

Symbol	Event	Status after Power-on	Description
OTW	over temperature warn	disable	when set OTWE temperature exceeds T <sub>OTW</sub> only in Normal mode
SPIF	SPI failure	disable	when set SPIFE: 1. SPI clock count is not 16,24, and 32 2. access locked register 3.illegal value write to 0x01 register
PNFDE	partial networking frame detection error	always enable	detection of error frame in partial networking mode
CBS	CAN bus silence	disable	WHEN CBSE set no active on CAN bus last at least t <sub>SILENCE</sub>
CF	CAN failure	disable	when CFE set: 1. TXD clamped LOW at least DTO time 2. Vcc undervoltage occurs if CMC = 01

All the events must be enabled via the associated event capture register before they take effect except PO and PNFDE, which are always enabled.

When an event occurs while the associated event capture register is enabled, the relevant event bit is set to 1. If CAN transceiver now is in CAN Offline mode, the RXD pin is pulled to LOW (if VIO is supplied) to indicate an interrupt to micro controller. If The device is in sleep mode, the INH pin is pulled HIGH and the device switches to Standby mode (exception SPIF event). That means all the events trigger the RXD pin to pull low, events except SPIF trigger a wake-up if the device is in Sleep mode.

A global event status register, 0x60 can be used to accelerate software to identify which kind of event (System, CAN transceiver, or WAKE pin) occurred.

Once the event occurs the status bit is set to 1. The method to clear the event is writing 1 to the relevant bit (writing 0 takes no effect). A simple way to clear all the occurred events is writing ff to the relevant register and all the bits are cleared.

### Sleep Mode Protection

All event status restored in register 0x61, 0x63, and 0x64 must be clear and at least one regular wake-up source (can wake up or local wake pin wake up) must be enabled before the device switches to sleep mode to avoid deadlock. Otherwise, the device switches to standby mode instead of sleep mode.

### Partial Networking

The device is compatible with ISO11898-2 and ISO11898-5, and supports partial networking (PN) with a selective wake-up function according to ISO11898-6. This feature is disabled after powering on and must be activated before use. Nodes only response to a specified wake-up frame (WUF) while other nodes remain Sleep mode to save power in a CAN network.

The simplified guide to configure partial networking features is to configure frame form including Data rate, frame ID and ID mask, Data length, Data mask, and Frame type; Enable partial networking (set bit CPNC=1&PNCOK=1) and CAN bus wake-up (set CWE=1). If all relative registers are configured correctly, bit CPNC&PNCOK = 1 and CWE=1 partial networking is enabled. Otherwise, partial networking is disabled, and only the wake-up pattern (WUP)can trigger can bus wake-up event.

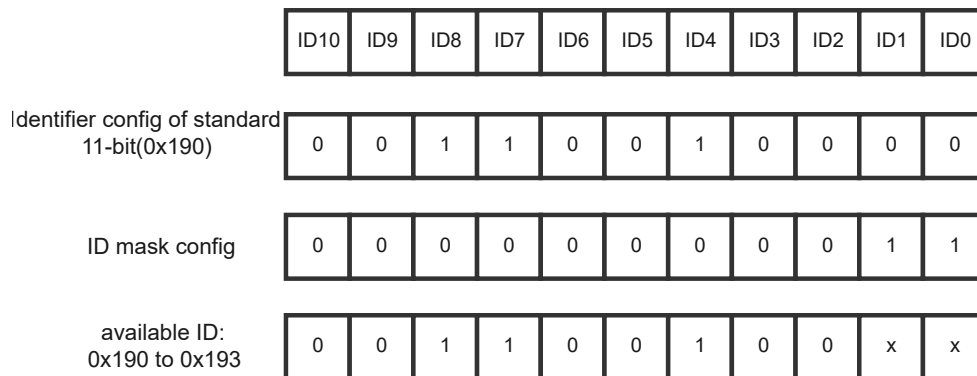
## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

The wake-up frame bit rate is defined in the DATA\_RATE register, valid rates are 50 kbps, 125 kbps, 250 kbps, 500 kbps, and 1 Mbps. The default rate is 500 kbps.

The type of wake-up frame can be the standard format (11-bit ID) or extended format (29-bit ID) via bit IDE in the FRAME\_CONTROL register.

The WUF identifier is configured in the ID register, and the correspondence between the identifier and register bit changes in standard and extended format. The example shows the difference. In standard format, only register 0x2A and 0x29 work and in extended format four ID registers work.

ID mask register can be used to allow a series of identifiers to be recognized as valid frames. The bit value “1” means ‘don’t care about the corresponding ID bit’. The example shows how ID mask registers operate. The identifier configuration is 0x190 via ID register 0x29 and 0x2A. The two least significant bit of ID mask register 0x2D are set to “1”. That means the frame ID:0x190,0x191,0x192 and 0x193 are valid wake-up frames to wake up the device.



**Figure 11. ID Mask Example**

Whether the data field is evaluated is determined via bit PNDM in the FRAME\_CONTROL register. If PNDM=0, only the identifier field is evaluated and the data field is ignored, the device is woken up when the identifier field of the frame matches the ID register configuration, and no CRC error occurs. If PNDM =1, both the identifier and data field are evaluated, and the device is woken up when the identifier field of the frame matches the ID register configuration, and the data field matches the data length and data mask configuration, and no CRC error occurs.

The bits DLC in the FRAME\_CONTROL register determines the expected number of bytes (up to 8 bytes) in the data field as a valid wake-up frame. If a frame contains a valid identifier but the data length doesn't match the DLC value, the device does not wake up. If one or more bytes are expected, The DLC configuration must match the actual number of bytes data fields and at least one bit of data field in the wake-up frame must be set to 1 and the corresponding bit in eight DATA MASK must be set to 1. If all DATA MASK register's value is 0, that means no frame can wake up in partial networking mode. Here is an example showing how the DATA MASK register works. A frame with a one-byte data field and data 0x01, 0x04, and 0x05 are all valid wake-up frames while the identifier field matches ID and ID MASK register while DLC = 1, and DM7 = 0x05.

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking



**Figure 12. Data Mask Example**

Only the data frame is valid WUF, the remote frame is not valid and can't wake up the device.

Any SPI write command to partial networking configuration registers clear bit PNCOK in the CAN\_CONTROL register(0x20), so it's recommended that the CAN\_CONTROL register should be written at the end of the register configuration procedure.

The CANFD frame is not the available frame and causes SBC to wake up by diagnostic wake-up. Then "CAN FD tolerance" feature is useful if CANFD frame exists in CAN net. Once enable CAN FD tolerance ( CFDC = 1 ) The device is passive to the CANFD frame and doesn't be woken up by the CANFD frame. If bit CFDC=0 and CANFD frame is running in the CAN bus network. The device wakes up by the PNFDE event.

If the wake-up frame has some error, e.g. stuff error, or CRC error in front of the ACK field, the internal Error counter of the chip increases. Any correct received frame decreases error counter until 0. Once the counter reaches threshold (default 32) a PNFDE event occurs and if now the device is in Sleep mode, it switches to standby mode by diagnostic wake up.

### Local Wake-up

Local wake-up is enabled by configuring bit WPRE and WPRF in register 0x23. A local wake-up event is triggered by a rising edge on the WAKE pin if WPRE = 1 and by a falling edge if WPRF = 1. It's recommended to connect the WAKE pin directly to GND in Application circuitry without a local wake-up function to enhance EMI performance. The voltage status of the WAKE pin can be monitored by reading bit WPVS in register 0x4B.

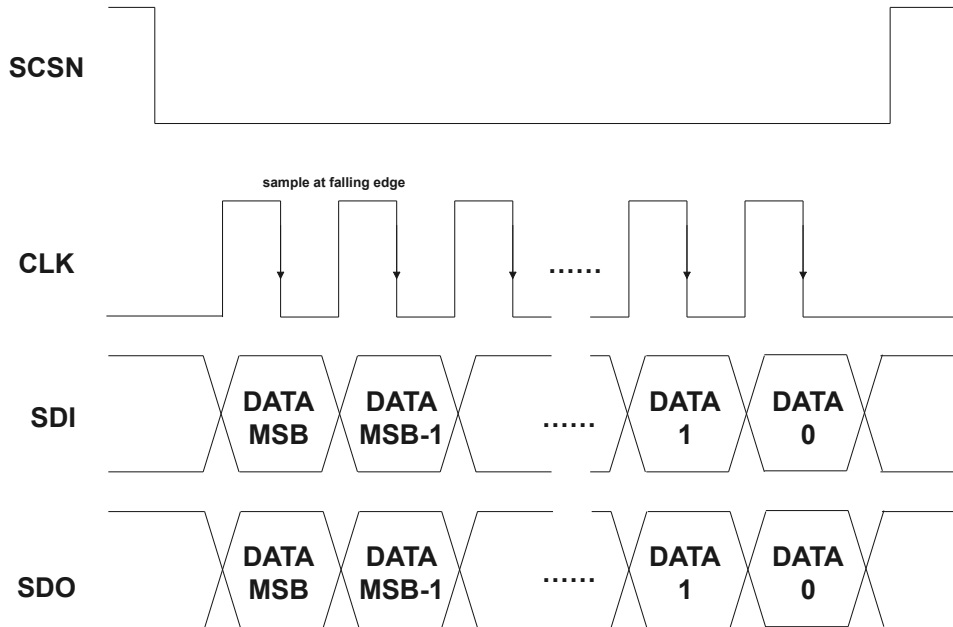
### Serial Peripheral Interface (SPI)

The SPI interface is configured to full duplex mode that register value returns while new data is shifted in. The device contains 4 pins:

- SCSN: SPI chip select, active LOW, default value is HIGH.
- SCLK: SPI chip clock, default value is LOW due to internal pull-down.
- SDI: SPI data input, also called MOSI, the default value depends on the signal from the microcontroller.
- SDO: SPI data output, also called MISO, floating when the SCSN pin is HIGH.

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

SPI is selected by CSN pulling low, data samples at the falling edge of CLK, CLK is Low in the idle state. SDI transmits the address and new data, and SDO transmits the address and current data. The figure shows the access.



**Figure 13. SPI Timing Protocol**

Data on SPI is a 16-bit form consisting of two bytes: the first byte contains a 7-bit address and 1-bit indicating read or write, the second byte is an 8-bit register value, access sequence is MSB first. Setting bit 7 to “0” is writing mode while setting bit 7 to “0” is reading mode. The figure shows the data form.

		MSB							LSB								
SDI	bit sequence	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	bit form	Address							R:1 W:0	Writing Data (W) can be any form (R)							
SDO	bit sequence	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	bit form	Address							R:1 W:0	Register Data							

**Figure 14. SPI Data Structure**

During SPI operation the value of the accessing register is returned via the SDO pin. Access to the register that doesn't exist causes SPIF event. writing operation with an illegal clock number, e.g. not 16, 24, or 32 causes SPIF failure and writing operation is aborted.

### CAN Partial Networking Configuration Registers

Dedicated registers are provided for configuring CAN partial networking.

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

**Table 7. Data Rate Register (Address 26h)**

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	CDR	R/W		CAN data rate selection:
			000	50 kbit/s
			001	100 kbit/s
			010	125 kbit/s
			011	250 kbit/s
			100	reserved (intended for future use; currently selects 500 kbit/s)
			101	500 kbit/s
			110	reserved (intended for future use; currently selects 500 kbit/s)
			111	1000 kbit/s

**Table 8. ID Registers 0 to 3 (Addresses 27h to 2Ah)**

Addr.	Bit	Symbol	Access	Value	Description
27h	7:0	ID7:ID0	R/W	-	bits ID7 to ID0 of the extended frame format
28h	7:0	ID15:ID08	R/W	-	bits ID15 to ID8 of the extended frame format
29h	7:2	ID23:ID18	R/W	-	bits ID23 to ID18 of the extended frame format bits ID5 to ID0 of the standard frame format
	1:0	ID17:ID16	R/W	-	bits ID17 to ID16 of the extended frame format
2Ah	7:5	reserved	R	-	
	4:0	ID28:ID24	R/W	-	bits ID28 to ID24 of the extended frame format bits ID10 to ID6 of the standard frame format

**Table 9. ID Mask Registers 0 to 3 (Addresses 2Bh to 2Eh)**

Addr.	Bit	Symbol	Access	Value	Description
2Bh	7:0	M7:M0	R/W	-	ID mask bits 7 to 0 of extended frame format
2Ch	7:0	M15:M8	R/W	-	ID mask bits 15 to 8 of extended frame format
2Dh	7:2	M23:M18	R/W	-	ID mask bits 23 to 18 of extended frame format ID mask bits 5 to 0 of standard frame format
	1:0	M17:M16	R/W	-	ID mask bits 17 to 16 of extended frame format
2Eh	7:5	reserved	R	-	
	4:0	M28:M24	R/W	-	ID mask bits 28 to 24 of extended frame format ID mask. bits 10 to 6 of standard frame format

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

**Table 10. Frame Control Register (Address 2Fh)**

Bit	Symbol	Access	Value	Description
7	IDE	R/W	-	identifier format:
			0	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W	-	partial networking data mask:
			0	data length code and data field are 'don't care' for wake-up
			1	data length code and data field are evaluated at wake-up
5:4	reserved	R	-	
3:0	DLC	R/W		number of data bytes expected in a CAN frame:
			0000	0
			0001	1
			0010	2
			0011	3
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	tolerated, 8 bytes expected

**Table 11. Data Mask Registers (Addresses 68h to 6Fh)**

Addr.	Bit	Symbol	Access	Value	Description
68h	7:0	DM0	R/W	-	data mask 0 configuration
69h	7:0	DM1	R/W	-	data mask 1 configuration
6Ah	7:0	DM2	R/W	-	data mask 2 configuration
6Bh	7:0	DM3	R/W	-	data mask 3 configuration
6Ch	7:0	DM4	R/W	-	data mask 4 configuration
6Dh	7:0	DM5	R/W	-	data mask 5 configuration
6Eh	7:0	DM6	R/W	-	data mask 6 configuration
6Fh	7:0	DM7	R/W	-	data mask 7 configuration

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

Data mask register usage for different values of DLC

DLC > 8		DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7
		Data 0	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	Data 7
DLC = 8		DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7
		Data 0	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	Data 7
DLC = 7			DM1	DM2	DM3	DM4	DM5	DM6	DM7
		Data 0	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	Data 6
DLC = 6				DM2	DM3	DM4	DM5	DM6	DM7
		Data 0	Data 1	Data 2	Data 3	Data 4	Data 4	Data 5	Data 5
DLC = 5					DM3	DM4	DM5	DM6	DM7
		Data 0	Data 1	Data 2	Data 3	Data 4	Data 4	Data 4	Data 4
DLC = 4						DM4	DM5	DM6	DM7
		Data 0	Data 1	Data 2	Data 3	Data 3	Data 3	Data 3	Data 3
DLC = 3							DM5	DM6	DM7
		Data 0	Data 1	Data 2	Data 2	Data 2	Data 2	Data 2	Data 2
DLC = 2								DM6	DM7
		Data 0	Data 1	Data 1	Data 1	Data 1	Data 1	Data 1	Data 1
DLC = 1									DM7
		Data 0	Data 0	Data 0	Data 0	Data 0	Data 0	Data 0	Data 0

### Device ID

A byte is reserved at address 0x7E for a TPT1445 identification code.

**Table 12. Identification Register (Address 7Eh)**

Bit	Symbol	Access	Value	Description
7:0	IDS[7:0]	R	74h	Device identification code: TPT1445Q

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

### Register Map

The addressable register space contains 128 registers with addresses from 0x00 to 0x7F. An overview of the register mapping is provided below.

Register Name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit Description
MODE_CONTROL <sup>(1)</sup>	0x01	7:3	Reserved	Null	5'h0	
		2:0	MC	CRW	3'h4	mode control 001: sleep 100: standby 111: normal
MAIN_STATUS	0x03	7	FSMS	R/O	1'h0	sleep mode transceiver status 0: by SPI 1: by VCC/VIO undervoltage. bus only can read. Logic can write
		6	OTWS	R/O	1'h0	overtemperature warning status 0: below 1: above. Bus only can read. Logic can write
		5	NMS	R/O	1'h1	normal mode status 0: entered normal mode(power-up) 1: not enter normal mode. Bus only can read. Logic can configuration
		4:0	Reserved	Null	5'h0	
SYSTEM_EVENT_ENABLE	0x04	7:3	Reserved	Null	5'h0	
		2	OTWE	R/W	1'h0	1: overtemperature warning enable 0: overtemperature warning disable
		1	SPIFE	R/W	1'h0	1: SPI failure enable. 0: SPI failure disable
		0	Reserved	Null	1'h0	
GPM_07_00	0x06	7:0	GPM_07_00	R/W	8'h0	memory0
GPM_15_08	0x07	7:0	GPM_15_08	R/W	8'h0	memory1
GPM_23_16	0x08	7:0	GPM_23_16	R/W	8'h0	memory2
GPM_31_24	0x09	7:0	GPM_31_24	R/W	8'h0	memory3
LOCK_CONTROL	0x0a	7	Reserved	Null	1'h0	

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

Register Name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit Description
		6	LK6C	R/W	1'h0	lock 0x68-0x6F 0: SPI write-access enable 1: SPI write-access disable
		5	LK5C	R/W	1'h0	lock 0x50-0x5F. 0: SPI write-access enable 1: SPI write-access disable
		4	LK4C	R/W	1'h0	lock 0x40-0x4F 0: SPI write-access enable 1: SPI write-access disable
		3	LK3C	R/W	1'h0	lock 0x30-0x3F 0: SPI write-access enable 1: SPI write-access disable
		2	LK2C	R/W	1'h0	lock 0x20-0x2F 0: SPI write-access enable 1: SPI write-access disable
		1	LK1C	R/W	1'h0	lock 0x10-0x1F 0: SPI write-access enable 1: SPI write-access disable
		0	LK0C	R/W	1'h0	lock 0x06-0x09 0: SPI write-access enable 1: SPI write-access disable
CAN_CONTROL	0x20	7	Reserved	Null	1'h0	
		6	CFDC	R/W	1'h0	CAN FD tolerance 0: disable 1: enable
		5	PNCOK	RWC	1'h0	CAN partial networking configurate 0: invalid. Only WUP enable 1: partial network config ok. Bus can write and read. and logic can clear it
		4	CPNC	RWC	1'h0	CAN selective wake-up 0: disable CAN selective wake-up 1: enable CAN selective wake-up. Bus can write and read. and logic can clear it
		3:2	Reserved	Null	2'h0	
		1:0	CMC	R/W	2'h1	CAN transceiver mode 00: offline 01: active-Vcc undervoltage detection active 10: active-Vcc undervoltage detection inactive 11: listen only

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

Register Name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit Description
TRANSCEIVER_STATUS	0x22	7	CTS	R/O	1'h0	CAN transceiver status 0: not in active 1: in active. Bus only can read. logic can write
		6	CPNERR	R/O	1'h1	CAN partial networking err status 0:no err detected 1:err detected. Bus only can read. Logic can write
		5	CPNS	R/O	1'h0	CAN partial networking status 0: configuration error detected 1: configuration ok. Bus only can read. Logic can write
		4	COSCS	R/O	1'h0	CAN oscillator status 0: not running at target frequency 1: running at target frequency. Bus only can read. Logic can write
		3	CBSS	R/O	1'h1	CAN bus silence status 0: CAN bus active 1: CAN bus inactive. Bus only can read. Logic can write
		2	Reserved	Null	1'h0	
		1	VCS	R/O	1'h0	Vcc supply voltage status 0: above threshold 1: below threshold. Bus only can read. Logic can write
		0	CFS	R/O	1'h0	CAN failures tatus 0: no TXD dominant timeout event detected 1: CAN transmitter disabled due the event. bus only can read. Logic can write
TRANSCEIVER_EVENT_ENABLE	0x23	7:5	Reserved	Null	3'h0	
		4	CBSE	R/W	1'h0	CAN bus silence enable 0: disable 1: enable
		3:2	Reserved	Null	2'h0	
		1	CFE	R/W	1'h0	CAN failure enable 0: disable 1: enable
		0	CWE	RWS	1'h0	CAN wake-up enable 0: disable

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

Register Name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit Description
						1: enable
DATA_RATE	0x26	7:3	Reserved	Null	5'h0	
		2:0	CDR	R/W	3'h5	CAN data rate 000: 50 kbit/s 001: 100 kbit/s 010: 125 kbit/s 011: 250 kbit/s 100: reserved 101: 500 kbit/s 110: reserved 111: 1000 kbit/s
ID_07_00	0x27	7:0	ID_07_00	R/W	8'h0	CAN frame ID bit 7:0 for partial frame networking wake up
ID_15_08	0x28	7:0	ID_15_08	R/W	8'h0	CAN frame ID bit 15:8 for partial frame networking wake up
ID_23_16	0x29	7:0	ID_23_16	R/W	8'h0	CAN frame ID bit 23:16 for partial frame networking wake up
ID_28_24	0x2a	7:5	Reserved	Null	2'h0	
		4:0	ID_28_24	R/W	5'h0	CAN frame ID bit 28:24 for partial frame networking wake up
M_07_00	0x2b	7:0	M_07_00	R/W	8'h0	CAN frame ID mask bit 7:0 for partial frame networking wake up
M_15_08	0x2c	7:0	M_15_08	R/W	8'h0	CAN frame ID mask bit 15:8 for partial frame networking wake up
M_23_16	0x2d	7:0	M_23_16	R/W	8'h0	CAN frame ID mask bit 23:16 for partial frame networking wake up
M_28_24	0x2e	7:5	Reserved	Null	2'h0	
		4:0	M_28_24	R/W	8'h0	CAN frame ID mask bit 28:24 for partial frame networking wake up
FRAME_CONTROL	0x2f	7	IDE	R/W	1'h0	identifier format 0: standard 1: extended
		6	PNDM	R/W	1'h1	PN data mask 0: data length and field are "don't care" 1: check data length and field
		5:4	Reserved	Null	2'h0	
		3:0	DLC	R/W	4'h0	data payload length in frame 0: data payload length is 0

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

Register Name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit Description
						1: data payload length is 1 2: data payload length is 2 3: data payload length is 3 4: data payload length is 4 5: data payload length is 5 6: data payload length is 6 7: data payload length is 7 others: data payload length is 8
WAKE_PIN_STATUS	0x4b	7:2	Reserved	Null	6'h0	
		1	WPVS	R/O	1'h0	wake pin status 0: below switching threshold 1: above switching threshold
		0	Reserved	Null	1'h0	
WAKE_PIN_ENABLE	0x4c	7:2	Reserved	Null	6'h0	
		1	WPRE	RWS	1'h0	wake pin rising edge enable 0: disable 1: enable
		0	WPFE	RWS	1'h0	wake pin falling edge enable 0: disable 1: enable
EVENT_CAPTURE_STATUS	0x60	7:4	Reserved	Null	4'h0	
		3	WPE	R/O	1'h0	wake pin event 0: no pending wake pin event 1: wake pin event pending
		2	TRXE	R/O	1'h0	transceiver event 0: no pending transceiver event 1: transceiver event pending
		1	Reserved	Null	1'h0	
		0	SYSE	R/O	1'h1	system event 0: no pending system event 1: system event pending
SYSTEM_EVENT_STATUS	0x61	7:5	Reserved	Null	3'h0	
		4	PO	CRW	1'h1	power-on 0: no power-on 1: left off mode after power-on
		3	Reserved	Null	1'h0	
		2	OTW	CRW	1'h0	overtemperature warning

## Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

Register Name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit Description
						0: overtemperature not detected 1: exceed overtemperature warning threshold
		1	SPIF	CRW	1'h0	SPI failure 0: no SPI failure detected 1: SPI failure detected
		0	Reserved	Null	1'h0	
TRANSCEIVER_EVENT_STATUS	0x63	7:6	Reserved	Null	2'h0	
		5	PNFDE	CRW	1'h0	PN frame detection err 0:no err 1:err
		4	CBS	CRW	1'h0	CAN bus status 0:CAN bus active 1:no activity
		3:2	Reserved	Null	2'h0	
		1	CF	CRW	1'h0	CAN failure 0:no CAN failure detected 1: CAN failure event detected
		0	CW	CRW	1'h0	CAN wake up 0:no CAN wake-up event detected 1: CAN wake-up event detected
WAKE_PIN_EVENT_STATUS	0x64	7:2	Reserved	Null	6'h0	
		1	WPR	CRW	1'h0	wake pin rising edge 0:no rising edge 1: rising edge
		0	WPF	CRW	1'h0	wake pin falling edge 0:no falling edge 1: falling edge
DM0	0x68	7:0	DM0	R/W	8'hFF	match byte 0
DM1	0x69	7:0	DM1	R/W	8'hFF	match byte 1
DM2	0x6a	7:0	DM2	R/W	8'hFF	match byte 2
DM3	0x6b	7:0	DM3	R/W	8'hFF	match byte 3
DM4	0x6c	7:0	DM4	R/W	8'hFF	match byte 4
DM5	0x6d	7:0	DM5	R/W	8'hFF	match byte 5
DM6	0x6e	7:0	DM6	R/W	8'hFF	match byte 6
DM7	0x6f	7:0	DM7	R/W	8'hFF	match byte 7

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**Automotive Fault Protected High-Speed CAN FD Transceiver for  
Partial Networking**

Register Name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit Description
ID	0x7e	7:0	ID	R/O	8'h74	chip id

(1) Recommend to add at least 50- $\mu$ s delay after writing to ensure the mode transition is finished and read the right register value.

# Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

## Application and Implementation

**Note**

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## Application Information

The TPT1445Q device is a CAN transceiver to support CAN FD function up to 8 Mbps, with BUS protection voltage from -45 V to +45 V, overtemperature shutdown, and a -12 V to +12 V common-mode range. The VIO of TPT1445Q can support the voltage level of TXD and RXD from 1.8 V to 5.0 V, and V<sub>BAT</sub> is from the battery power supply.

The following sections show a typical application of the TPT1445Q.

## Typical Application

Figure 15 shows the typical application schematic of the TPT1445Q.

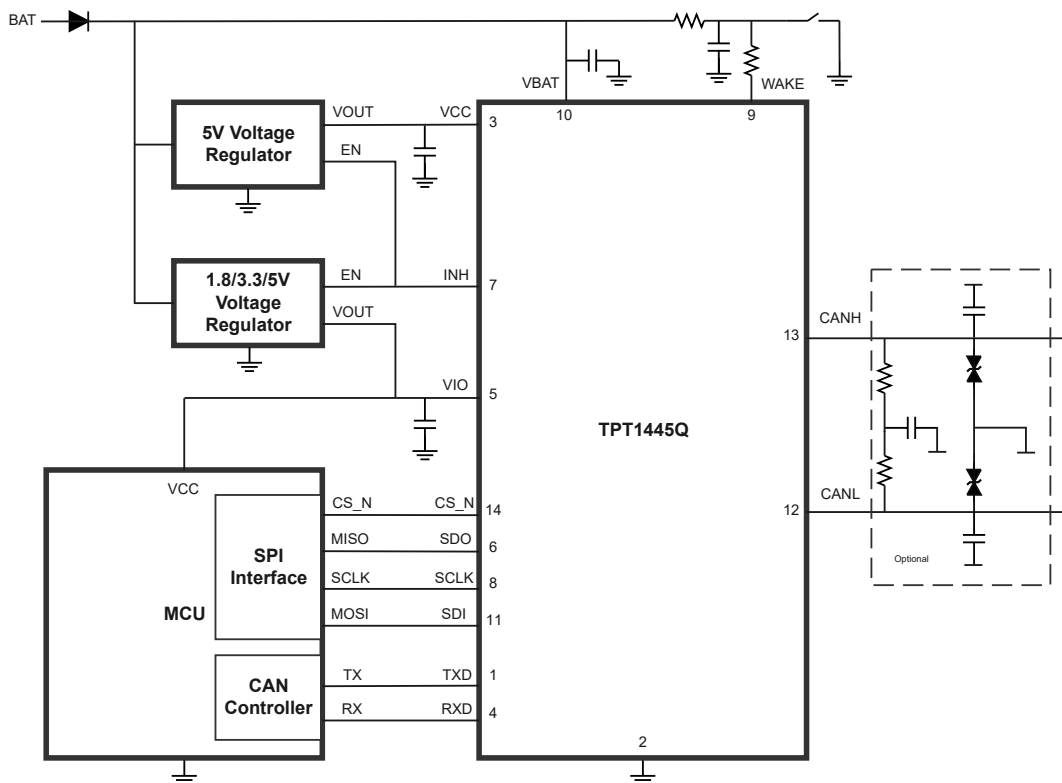
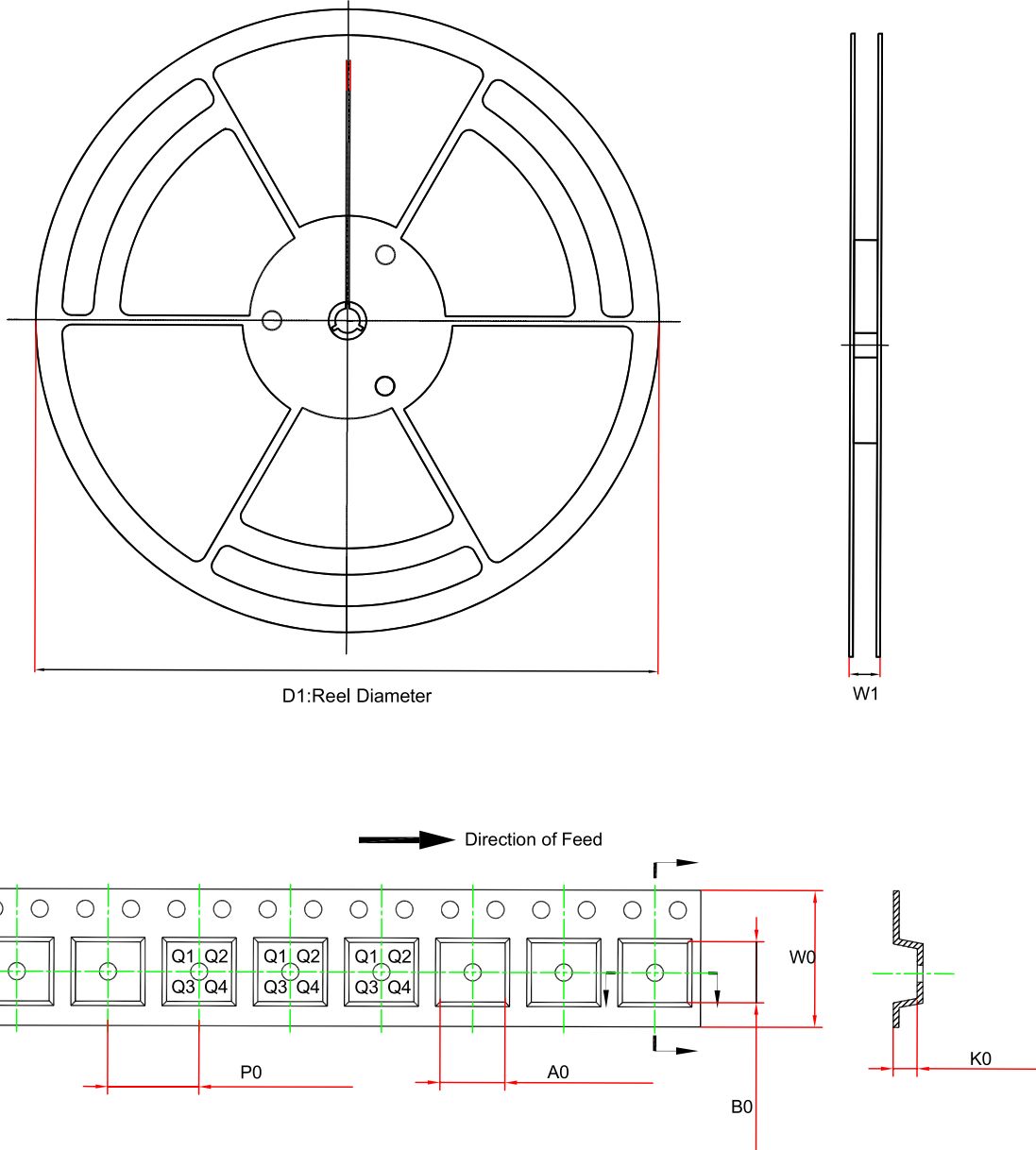


Figure 15. Typical Application Circuit

Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

Tape and Reel Information

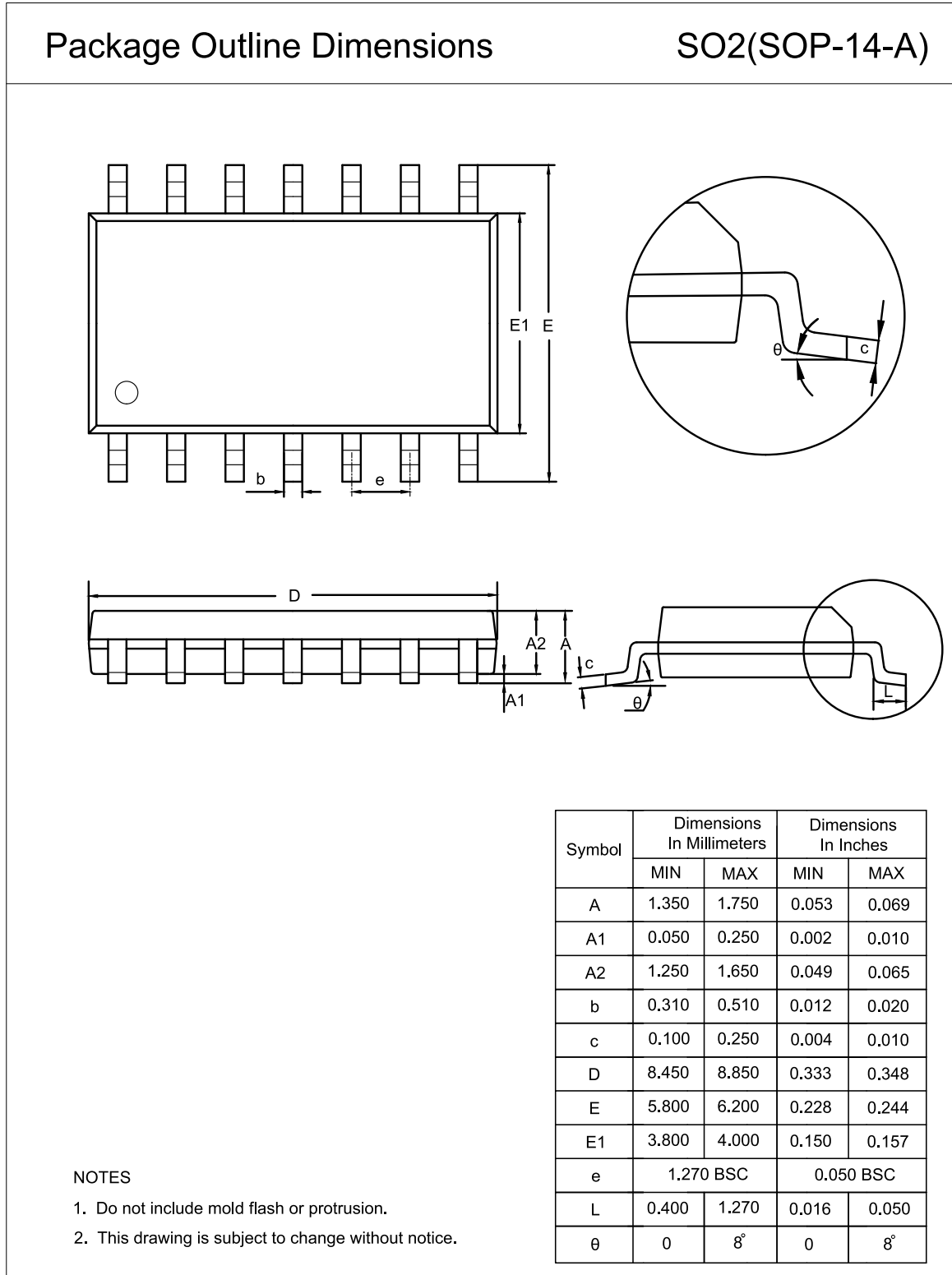


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT1445Q-SO2R-S	SOP14	330	21.6	6.5	9.0	2.1	8.0	16.0	Q1
TPT1445Q-DFKR-S	DFN4.5X3-14	330	17.6	3.3	4.8	1.1	8.0	12.0	Q1

Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

Package Outline Dimensions

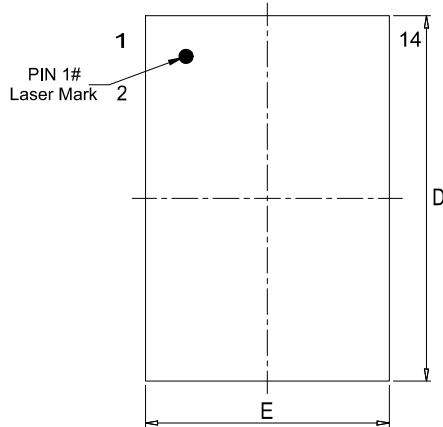
SOP14



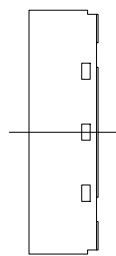
Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

DFN4.5X3-14-WET-B

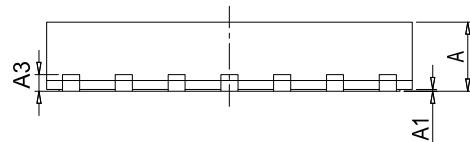
Package Outline Dimensions DFK(DFN4.5X3-14-WET-B)



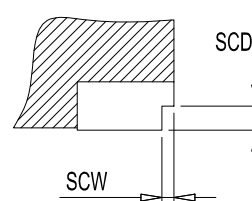
TOP VIEW



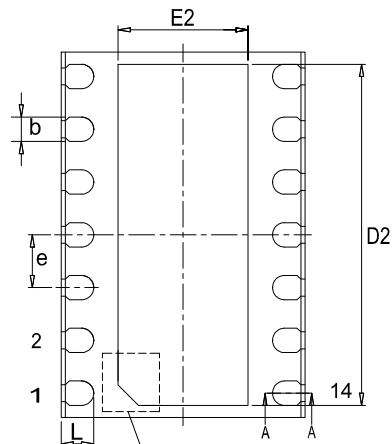
SIDE VIEW



SIDE VIEW



DETAIL A



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.250	0.350	0.010	0.014
A3	0.203 REF		0.008 REF	
D	4.400	4.600	0.173	0.181
E	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.300	0.500	0.012	0.020
D2	4.100	4.300	0.161	0.169
E2	1.500	1.700	0.059	0.067
SCW	0.010	0.090	0.0004	0.004
SCD	0.080	0.180	0.003	0.007

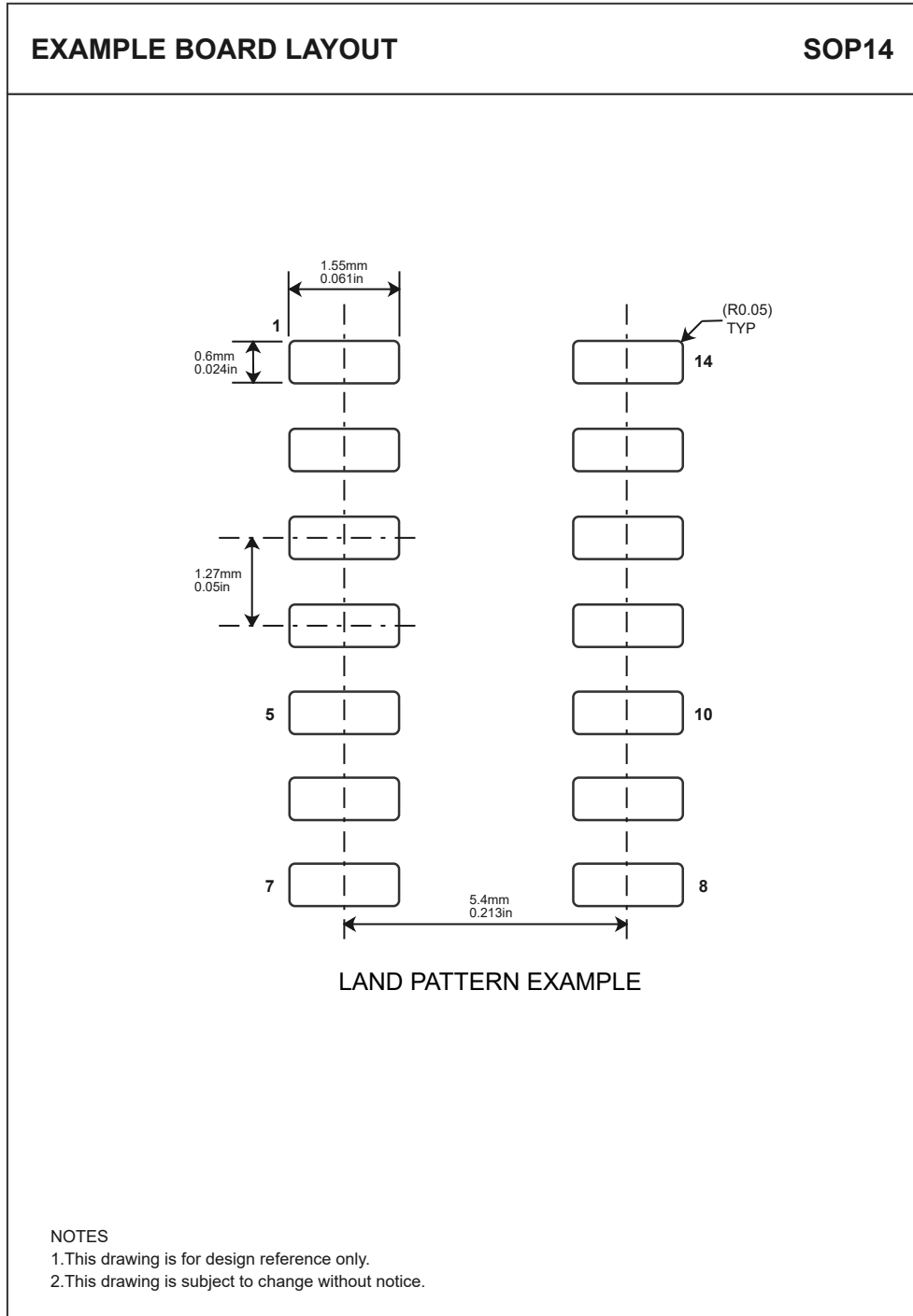
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

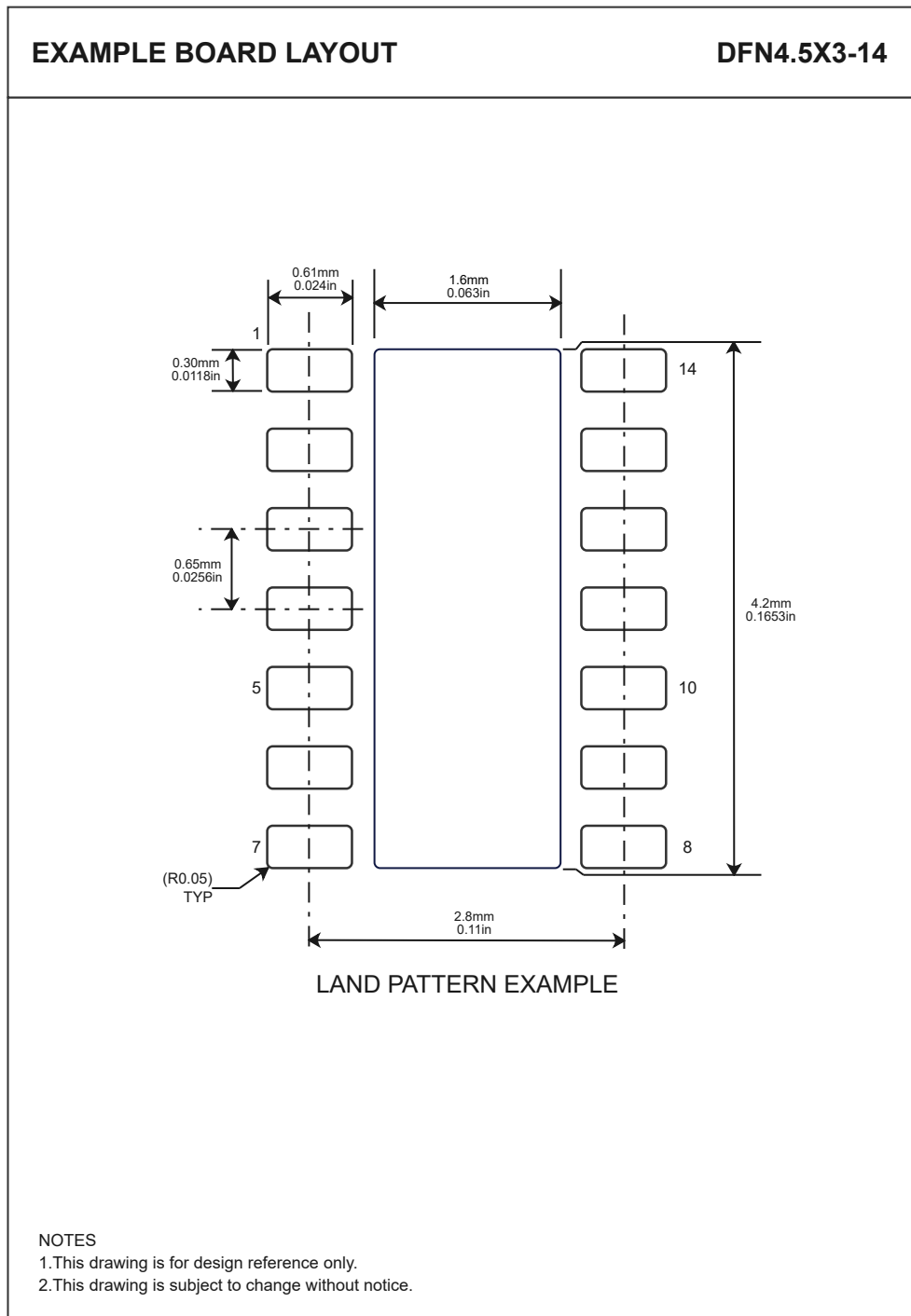
Example Board Layout

SOP14



Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

DFN4.5X3-14



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**Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking****Order Information**

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT1445Q-SO2R-S	-40 to 125°C	SOP14	T1445Q	MSL1	Tape and Reel, 2500	Green
TPT1445Q-DFKR-S	-40 to 125°C	DFN4.5X3-14	T1445Q	MSL1	Tape and Reel, 4000	Green

**Green:** 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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**Automotive Fault Protected High-Speed CAN FD Transceiver for  
Partial Networking****IMPORTANT NOTICE AND DISCLAIMER**

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