Automotive Low-Power Fault-Protected High-Speed CAN FD Transceiver with Sleep Mode

Features

- Meet the ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5 Physical Layer Standards
- Supports Classical CAN and Optimized CAN FD up to 8 Mbps Data Rates
- Short Propagation Delay Times and Fast Loop Times
- 5-V Power Supply, I/O Voltage Range Supports 1.7-V to 5.5-V MCU Interface
- Standby Mode and Extra Low Current Sleep Mode with Local and Remote Bus Wake-Up Capability and INH Output
- Ideal Passive Behavior to CAN Bus when Unpowered
- Glitch-free on CAN Bus and RXD when Power on/off
- Protection Feature:
  - Bus HBM ESD Protection up to 15 kV and IEC 61000-4-2 ESD Protection
  - Bus Fault Protection: ±45 V
  - Undervoltage Protection
  - TXD Dominant Time-Out Function and Bus-Dominant Time-Out Function
  - Thermal Shutdown Protection
- Available in SOP14 Package and DFN4.5X3-14 Package with Improved Automated Optical Inspection (AOI) Capability
- AEC-Q100 Qualified for Automotive Application, Grade 1

Applications

- All Devices Supporting Highly Loaded CAN Networks
- Automotive and Transportation
  - Body Electronics / Lighting
  - Power Train / Chassis
  - Infotainment / Cluster
  - ADAS / Safety

Description

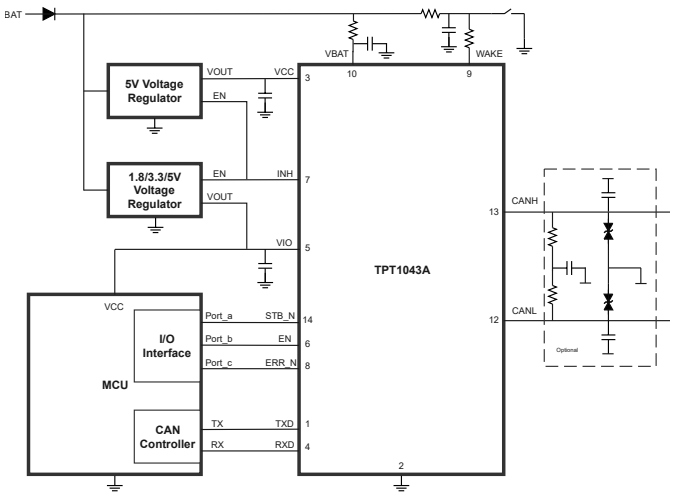
The TPT1043AQ is a CAN transceiver that meets the ISO11898-2:2024, SAEJ2284-1 to SAE J2284-5 high-speed CAN (Controller Area Network) physical layer standard.

The devices are designed to be used in CAN FD networks up to 5 Mbps with enhanced timing margin and higher data rates in long and highly loaded networks, and support up to 8-Mbps data rates in simple CAN bus networks. The system design can be optimized with excellent electromagnetic compatibility (EMC) and electrostatic discharge (ESD) performance. The TPT1043AQ has a secondary power supply input VIO pin for I/O level shifting to support 1.8-V, 2.5-V, 3.3-V, and 5-V MCU logic levels directly. The device has low-current standby and sleep mode with CAN bus wake-up capability via wake-up pattern (WUP) which is defined in ISO11898-2:2024. The device supports ultra-low power management to power down the entire node and enables the power supply by the INH pin through the local or remote wake-up with wake-up source recognition capability.

As designed, the devices feature bus fault protection from −45 V to +45 V, TXD dominant time-out (DTO), and over-temperature shutdown (TSD). Additionally, all devices include power-off ideal passive behavior fail-safe features to enhance the network robustness.

The TPT1043AQ is available in SOP14 and DFN4.5X3-14 packages and is AEC-Q100 qualified for automotive applications.

Typical Application Circuit



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Product Family Table

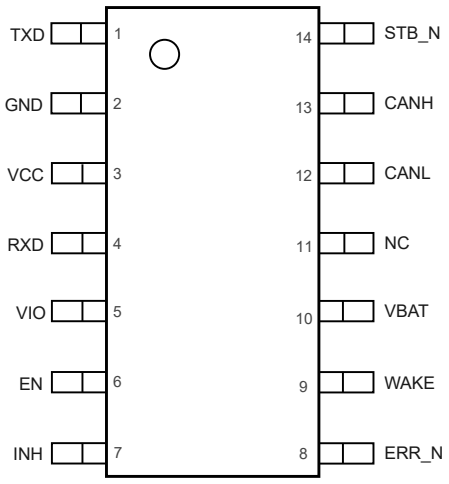
Order Number	VCC (V)	VIO (V)	BUS Protection (V)	Package
TPT1043AQ-SO2R-S	4.5 to 5.5	1.7 to 5.5	±45	SOP14
TPT1043AQ-DFKR-S	4.5 to 5.5	1.7 to 5.5	±45	DFN4.5X3-14

Revision History

Date	Revision	Notes
2025-05-29	Rev.Pre.0	Initial version
2025-07-02	Rev.A.0	Released version
2025-11-18	Rev.A.1	Updated the values for I_{BAT} and the test conditions for some parameters Updated thermal information Updated application information Updated feature description Updated typical application The actual product remains unchanged
2025-12-19	Rev.A.2	Corrected the typos of parameters $V_{HYS\_RX\_DIF}$, V_{SYM}, V_{HYS_UVVCC} Added Example Board Layout The actual product remains unchanged

Pin Configuration and Functions

TPT1043A
SOP14 Package
Top View



TPT1043A
DFN4.5X3 Package
Top View

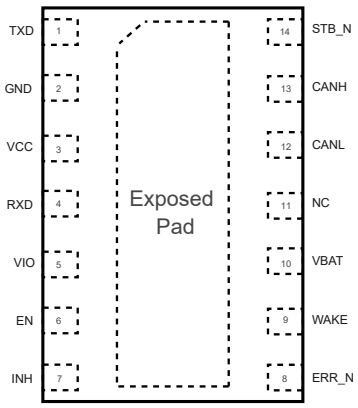


Table 1. Pin Functions: TPT1043A

Pin		I/O	Description
No.	Name		
1	TXD	Input	CAN transmit data input (low for dominant and high for recessive bus states)
2	GND	GND	Ground connection
3	VCC	Power	5-V CAN bus supply voltage
4	RXD	Output	CAN receive data output (low for dominant and high for recessive bus states), tri-state
5	VIO	Power	I/O supply voltage
6	EN	Input	Enable input for mode control, integrated pull down
7	INH	Output	Can be used to control system voltage regulators
8	ERR_N	Output	Fault output, inverted logic
9	WAKE	Input	Wake input terminal, high voltage input
10	VBAT	Power	Reverse-blocked battery supply input
11	NC	-	No connect (not internally connected)
12	CANL	Bus I/O	Low-level CAN bus input/output line
13	CANH	Bus I/O	High-level CAN bus input/output line
14	STB_N	Input	Standby input for mode control, integrated pull down
	Exposed pad	GND	Thermal pad of the DFN package, required to connect the exposed pad to Ground

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{BAT}	Battery Supply Voltage Range	−0.3	45	V
V_{CC}	Supply Voltage Range	−0.3	7	V
V_{IO}	I/O Level-Shifting Voltage Range	−0.3	7	V
V_{BUS}	CAN Bus I/O Voltage Range (CANH, CANL)	−45	45	V
V_{BUS_DIFF}	Differential Voltage of CAN Bus, CANH − CANL	−45	45	V
V_{LOGIC_IN}	Logic Input Terminal Voltage Range	−0.3	7	V
V_{LOGIC_OUT}	Logic Output Terminal Voltage Range	−0.3	V_{IO} + 0.3	V
V_{WAKE}	WAKE Input Pin Voltage Range	−45	45	V
V_{INH}	INH Output Pin Voltage Range	−0.3	V_{BAT} + 0.3	V
T_J	Junction Temperature	−55	150	°C
T_{STG}	Storage Temperature Range	−55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD (Electrostatic Discharge Protection)

Parameter		Condition	Minimum Level	Unit
V_{ESD}	Electrostatics Discharge	Contact discharge on bus pins (CANH, CANL); VBAT pin with 100-nF capacitor; WAKE pin with 33 kΩ resistor, per IEC61000-4-2 (150 pF, 330-Ω discharge circuit)	±8	kV
		Human Body Model (HBM) on all pins, per AEC Q100-002	±8	kV
		Human Body Model (HBM) on bus pins (CANH, CANL), per AEC Q100-002	±15	kV
		Charged Device Model (CDM) on all pins, per AEC Q100-011	±1.5	kV
V_{TRAN}	ISO7637-2 transients per IEC 62228-3, CANH, CANL, WAKE, VBAT	Pulse 1	−100	V
		Pulse 2a	75	V
		Pulse 3a	−150	V
		Pulse 3b	100	V

Recommended Operating Conditions

Description		Min	Max	Unit
V_{BAT}	Battery Supply Voltage Range	4.5	40	V
V_{IO}	Input/output Voltage TXD, RXD, STB_N, ERR_N, EN	1.7	5.5	V
V_{CC}	Power Supply	4.5	5.5	V
I_{OH_RXD}	RXD Terminal High-Level Output Current	−4	-	mA
I_{OL_RXD}	RXD Terminal Low-Level Output Current	-	4	mA
I_{O_INH}	INH Output Current	-	1	mA
T_A	Operating Ambient Temperature	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
SOP14	79.65	38.22	41.5	°C/W
DFN4.5x3-14	35.26	14.98	36.56	°C/W

Electrical Characteristics

All test conditions: V_{CC} = 4.5 V to 5.5 V, V_{IO} = 1.7 V to 5.5 V, V_{BAT} = 4.5 V to 40 V, R_L = 60 Ω, T_A = −40°C to 125°C, unless otherwise noted.

Parameter		Test Conditions	Min	Typ	Max	Unit
Pin VCC (Power Supply)						
V_{CC}	Supply Voltage		4.5	-	5.5	V
UV_{VCC_R}	Undervoltage Recovery on V_{CC}	V_{CC} Rising	-	3.6	4.3	V
UV_{VCC_F}	Undervoltage Detection on V_{CC}	V_{CC} Falling	3	3.4	-	V
V_{HYS_UVVCC}	Hysteresis Voltage on UV_{VCC}		50	100	-	mV
I_{CC}	Supply Current	Normal mode (dominant), V_{TXD} = 0 V; t < t_{TXD_DTO}	-	42	65	mA
		Dominant bus fault, V_{TXD} = 0 V; short circuit on bus lines; −40 V < (V_{CANH} = V_{CANL}) < +40 V	-	-	100	mA
		Normal mode (recessive), V_{TXD} = V_{IO}	-	7	9	mA
		Silent mode	-	5	8	mA
		Standby/Sleep mode	-	-	2	μA
Pin VIO (I/O Supply)						
V_{IO}	Supply Voltage on V_{IO} Pin		1.7	-	5.5	V
UV_{VIO_R}	Undervoltage Recovery on V_{IO}	V_{IO} Rising	-	-	1.65	V
UV_{VIO_F}	Undervoltage Detection on V_{IO}	V_{IO} Falling	1.35	-	-	V
V_{HYS_UVVIO}	Hysteresis Voltage on UV_{VIO}		-	50	-	mV
I_{IO}	Supply Current from VIO	Normal mode, V_{TXD} = 0 V, dominant	-	110	500	μA
		Normal/Silent mode, V_{TXD} = V_{IO}, recessive	-	-	3	μA
		Standby/Sleep mode	-	-	2	μA
Pin VBAT (Supply from Battery)						
V_{BAT}	Battery Supply Voltage		4.5	-	40	V
UV_{BAT_R}	Undervoltage Recovery on VBAT	VBAT rising	-	3.65	4.3	V
UV_{BAT_F}	Undervoltage Detection on VBAT	VBAT falling	3	3.45	-	V
V_{HYS_UVBAT}	Hysteresis Voltage on UV_{BAT}		-	100	-	mV
I_{BAT}	Battery Supply Current	Normal/Silent mode; pin INH left open	-	60	100	μA
		Standby mode; pin INH left open; V_{WAKE} = V_{BAT}	-	13	30	μA
		Sleep mode; V_{WAKE} = V_{BAT};	-	13	30	μA

Parameter			Test Conditions	Min	Typ	Max	Unit
Pin TXD (CAN Transmit Data Input)							
V_{IH_TXD}	High-level Input Voltage			0.7 x V_{IO}	-	-	V
V_{IL_TXD}	Low-level Input Voltage			-	-	0.3 x V_{IO}	V
V_{HYS_TXD}	Hysteresis Voltage on TXD Inputs			50	500	-	mV
I_{IH_TXD}	High-level Input Current			-5	-	5	μA
I_{IL_TXD}	Low-level Input Current			-300	-	-30	μA
C_I	Input Capacitance (1)			-	-	10	pF
Pin RXD (CAN Receive Data Output)							
I_{OH_RXD}	High-level Output Current		V_{RXD} = V_{IO} – 0.4 V	−10	-	−1	mA
I_{OL_RXD}	Low-level Output Current		V_{RXD} = 0.4 V; Bus dominant	1	-	35	mA
Pin STB_N, EN (Standby and Enable Control Input)							
V_{IH}	High-level Input Voltage			0.7 x V_{IO}	-	-	V
V_{IL}	Low-level Input Voltage			-	-	0.3 x V_{IO}	V
V_{HYS}	Hysteresis Voltage on STB, EN Input			50	500	-	mV
I_{IH}	High-level Input Current			1	-	10	μA
I_{IL}	Low-level Input Current			-1	-	1	μA
C_{IN}	Input Capacitance (1)			-	-	10	pF
Pin ERR_N (Error and Power-on Indication Output)							
$I_{OH\_ERR\_N}$	High-level Output Current		V_{ERR_N} = V_{IO} – 0.4 V	−50	-	−4	μA
$I_{OL\_ERR\_N}$	Low-level Output Current		V_{ERR_N} = 0.4 V	0.1	-	2	mA
Pin WAKE (Local Wake-up Pin)							
R_{PU_WAKE}	WAKE Pin Pull-up Resistance			100	-	400	kΩ
R_{PD_WKAE}	WAKE Pin Pull-down Resistance			100	-	400	kΩ
V_{IH_WAKE}	Wake-up High-Level Input Voltage		Sleep or Standby mode	2.6	-	-	V
V_{IL_WAKE}	Wake-up Low-Level Input Voltage		Sleep or Standby mode	-	-	1.8	V
V_{HYS_WAKE}	Hysteresis Voltage on WAKE			90	200	-	mV
Pin INH (Inhibit High Voltage Output)							
ΔV_H	High-level Voltage Drop		ΔV_H = V_{BAT} - V_{INH}; I_{INH} = −1 mA	0	-	1	V
			ΔV_H = V_{BAT} - V_{INH}; I_{INH} = −2 mA	0	-	2	V
I_{L_INH}	Leakage Current		Sleep mode	−2	-	2	μA
I_{OS_INH}	Short-Circuit Output Current		V_{INH} = 0 V	−30	-	-	mA
Pin CANH, CANL (CAN Bus Lines)							
V_{O_DOM}	Dominant Bus Output Voltage	CANH	Dominant; 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{TXD} = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, t < t_{TXD_DTO}	2.89	3.5	4.26	V
		CANL		0.77	1.5	2.13	V

Parameter		Test Conditions	Min	Typ	Max	Unit
$V_{DOM\_TX\_SYM}$	Transmitter Dominant Voltage Symmetry (1)	$V_{DOM\_TX\_SYM} = V_{CC} - V_{CANH} - V_{CANL}$	−300	-	300	mV
V_{SYM}	Transient Symmetry (dominant or recessive) $(V_{O(CANH)} + V_{O(CANL)}) / V_{CC}$ (1)	4.75 V ≤ V_{CC} ≤ 5.25 V, R_L = 60 Ω, C_L = open, C_{SPLIT} = 4.7 nF, T_{XD} = 250 kHz, 1 MHz, 2.5 MHz	0.9	-	1.1	V/V
V_{OD_DOM}	Differential Output Voltage (dominant)	CAN active mode, t < t_{TXD_DTO}, 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{TXD} = 0 V, 50 Ω ≤ R_L < 65 Ω, C_L = open	1.5	-	2.75	V
		CAN active mode, t < t_{TXD_DTO}, 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{TXD} = 0 V, 45 Ω ≤ R_L ≤ 70 Ω, C_L = open	1.4	-	3.3	V
		CAN active mode, t < t_{TXD_DTO}, 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{TXD} = 0 V, R_L = 2240 Ω, C_L = open	1.5	-	5.0	V
V_{OD_REC}	Differential Output Voltage (recessive)	Normal/Silent mode, V_{TXD} = V_{IO}, no load	−50	-	50	mV
		Standby/Sleep mode	−0.2	-	0.2	V
V_{O_REC}	Recessive Output Voltage	Normal/Silent mode, V_{TXD} = V_{IO}, no load	2	2.5	3	V
		Standby/Sleep mode	−0.1	-	0.1	V
$I_{O\_SC\_DOM}$	Dominant Short-Circuit Output Current	−40 V ≤ V_{CANH} / V_{CANL} ≤ 40 V	-	-	100	mA
$I_{O\_SC\_REC}$	Recessive Short-Circuit Output Current	−40 V ≤ V_{CANH}/ V_{CANL} ≤ 40 V	−3	-	3	mA
$V_{TH\_RX\_DIF}$	Differential Receiver Threshold Voltage	Normal or Silent mode, −12 V ≤ V_{CANH}/ V_{CANL} ≤ 12 V	0.5	-	0.9	V
		Standby or Sleep mode, −12V ≤ V_{CANH}/ V_{CANL}≤ 12 V	0.4	-	1.1	V
V_{REC_RX}	Receiver Recessive Voltage	Normal or Silent mode, −12 V ≤ V_{CANH}/ V_{CANL} ≤ 12 V	−4	-	0.5	V
		Standby or Sleep mode, −12 V ≤ V_{CANH}/ V_{CANL} ≤ 12 V	−4	-	0.4	V
V_{DOM_RX}	Receiver Dominant Voltage	Normal or Silent mode, −12 V ≤ V_{CANH}/ V_{CANL} ≤ 12 V	0.9	-	9	V
		Standby or Sleep mode, −12 V ≤ V_{CANH}/ V_{CANL} ≤ 12 V	1.1	-	9	V
$V_{HYS\_RX\_DIF}$	Differential Receiver Hysteresis Voltage	Normal or Silent mode, −12 V ≤ V_{CANH}/ V_{CANL} ≤ 12 V	100	150	-	mV
		Standby or Sleep mode, −12 V ≤ V_{CANH}/ V_{CANL} ≤ 12 V (1)	100	150	-	mV

Parameter		Test Conditions	Min	Typ	Max	Unit
I_L	Leakage Current	V_{BAT} = V_{CC} = 0 V or pins shorted to ground via 47 kΩ; V_{CANH} = 5 V, V_{CANL} = 5 V	−10	-	10	μA
R_{IN}	Input Resistance (CANH or CANL)	−2 V ≤ V_{CANH}/V_{CANL} ≤ 7 V	9	17	28	kΩ
ΔR_{IN}	Input Resistance Deviation	0 V ≤ V_{CANH}/V_{CANL} ≤ 5 V	−3	-	3	%
R_{IN_DIF}	Differential Input Resistance	−2 V ≤ V_{CANH}/V_{CANL} ≤ 7 V	19	30	52	kΩ
C_{IN}	Input Capacitance to Ground (CANH or CANL) (1)		-	-	30	pF
C_{IN_DIF}	Differential Input Capacitance (1)		-	-	15	pF
Temperature Detection						
T_{J_SD}	Shutdown Junction Temperature (1)		160	180	200	℃
$T_{J\_SD\_HYS}$	Shutdown Temperature Hysteresis (1)		-	20	-	℃

(1) The data is based on bench tests and design simulations.

AC Timing Requirements

All test conditions: V_{CC} = 4.5 V to 5.5 V, V_{IO} = 1.7 V to 5.5 V, V_{BAT} = 4.5 V to 40 V, R_L = 60 Ω, T_A = −40°C to 125°C, unless otherwise noted.

Parameter		Test Conditions	Min	Typ	Max	Unit
Transceiver Switching Characteristics						
$t_{D\_TXD\_BUSDOM}$	Delay Time from TXD to Bus Dominant	Normal mode	-	-	90	ns
$t_{D\_TXD\_BUSREC}$	Delay Time from TXD to Bus recessive		-	-	90	ns
$t_{D\_BUSREC\_RXD}$	Delay Time from Bus Recessive to RXD	Normal mode	-	-	110	ns
$t_{D\_BUSDOM\_RXD}$	Delay Time from Bus Dominant to RXD		-	-	110	ns
$t_{D\_TXDL\_RXDL}$	Loop Delay Time from TXD Low to RXD Low	Normal mode	-	-	200	ns
$t_{D\_TXDH\_RXDH}$	Loop delay time from TXD High to RXD High		-	-	200	ns
CAN FD Timing Parameters						
t_{BIT_BUS}	Transmitted Recessive Bit Width	2 Mbps, t_{BIT_TXD} = 500 ns	435	-	530	ns
		5 Mbps, t_{BIT_TXD} = 200 ns	155	-	210	ns
		8 Mbps, t_{BIT_TXD} = 125 ns (1)	95	-	135	ns
t_{BIT_RXD}	RXD Bit Width	2 Mbps, t_{BIT_TXD} = 500 ns	400	-	550	ns
		5 Mbps, t_{BIT_TXD} = 200 ns	150	-	220	ns
		8 Mbps, t_{BIT_TXD} = 125 ns (1)	75	-	145	ns
Δt_{REC}	Receiver Timing Symmetry	2 Mbps, 4.5 V ≤ V_{CC} ≤ 5.5 V	−65	-	40	ns
		5 Mbps, 4.5 V ≤ V_{CC} ≤ 5.5 V	−45	-	15	ns
		8 Mbps, 4.5 V ≤ V_{CC} ≤ 5.5 V (1)	−30	-	15	ns
Device Timing Parameters						
t_{TXD_DTO}	TXD Dominant Time-out Time (1)	Normal mode; V_{TXD} = 0 V	0.8	-	3	ms
t_{BUS_DTO}	BUS Dominant Time-out Time (1)	Normal mode or Silent mode; V_{O_DIF} > 0.9 V	0.8	-	3	ms
t_{WAKE_BUSDOM}	Bus Wake-up Time (dominant)	Standby/Sleep mode	0.5	-	1.8	μs
t_{WAKE_BUSREC}	Bus Wake-up Time (recessive)	Standby/Sleep mode	0.5	-	1.8	μs
$t_{WAKE\_BUS\_TO}$	Bus Wake-up Time-out Time (1)	Standby/Sleep mode	0.8	-	3	ms
$t_{H\_GOTOSLEEP}$	Go-to-sleep Hold Time (1)	STB_N = low and EN = high hold time for entering Sleep mode	24	-	50	μs

Parameter		Test Conditions	Min	Typ	Max	Unit
t_{WAKE}	Wake-up Time (1)	In response to a falling or rising edge on WAKE pin; Standby or Sleep mode	20	-	50	μs
t_{UVD}	Undervoltage Detection Time (1)	Pin VCC	100	-	350	ms
		Pin VIO	100	-	350	ms
t_{UVR}	Undervoltage Recovery Time (1)	Pin VCC	-	-	5	ms
		Pin VIO	-	-	5	ms

(1) The test data is based on bench tests and design simulations.

Parameter Measurement Information

Test Circuit

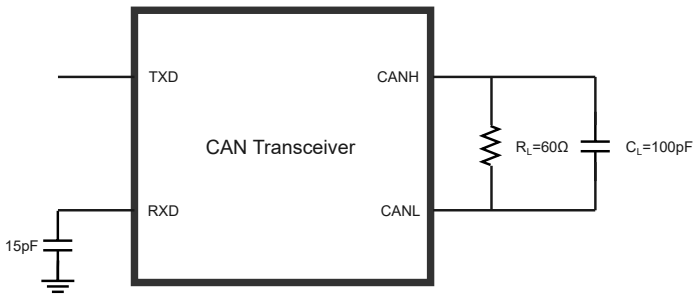


Figure 1. CAN Transceiver Timing Parameter Test Circuit

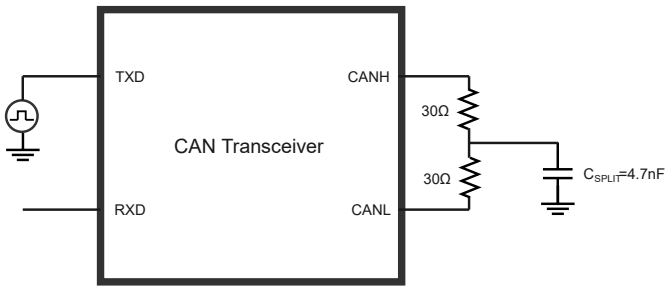


Figure 2. CAN Transceiver Driver Symmetry Test Circuit

Parameter Diagram

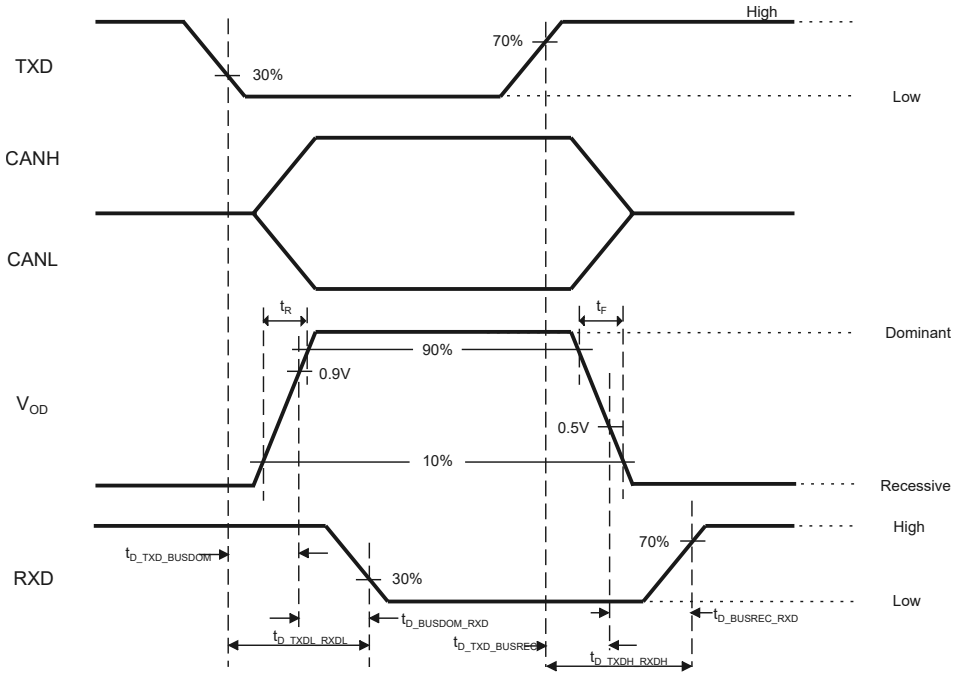


Figure 3. CAN Transceiver Timing Diagram

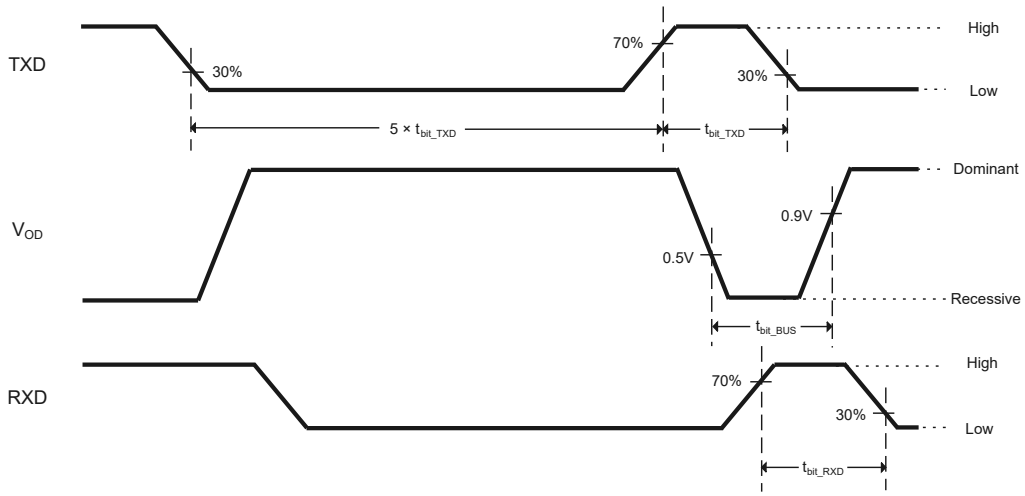


Figure 4. CAN FD Timing Parameter Diagram

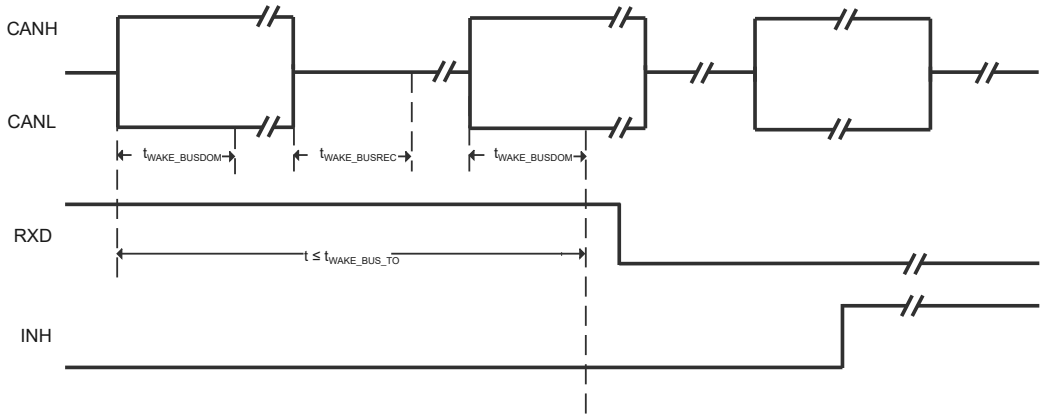


Figure 5. Wake-up Timing Diagram

Detailed Description

Overview

The TPT1043AQ is a CAN transceiver that meets the ISO11898-2:2024, SAEJ2284-1 to SAE J2284-5 high-speed CAN (Controller Area Network) physical layer standard. The devices are designed to be used in CAN FD networks up to 5 Mbps with enhanced timing margin and higher data rates in long and highly loaded networks, and support up to 8-Mbps data rates in simple CAN bus networks. The TPT1043AQ has a secondary power supply input VIO pin for I/O level shifting to support 1.8-V, 2.5-V, 3.3-V, and 5-V MCU logic levels directly. The device has low-current standby and sleep mode with CAN bus wake-up capability via wake-up pattern (WUP) which is defined in ISO11898-2:2024. The device supports ultra-low power management to power down the entire node and enables the power supply by the INH pin through the local or remote wake-up with wake-up source recognition capability. As designed, the devices feature bus fault protection from −45 V to +45 V, TXD dominant time-out (DTO), and over-temperature shutdown (TSD). Additionally, all devices include power-off ideal passive behavior fail-safe features to enhance the network robustness.

Functional Block Diagram

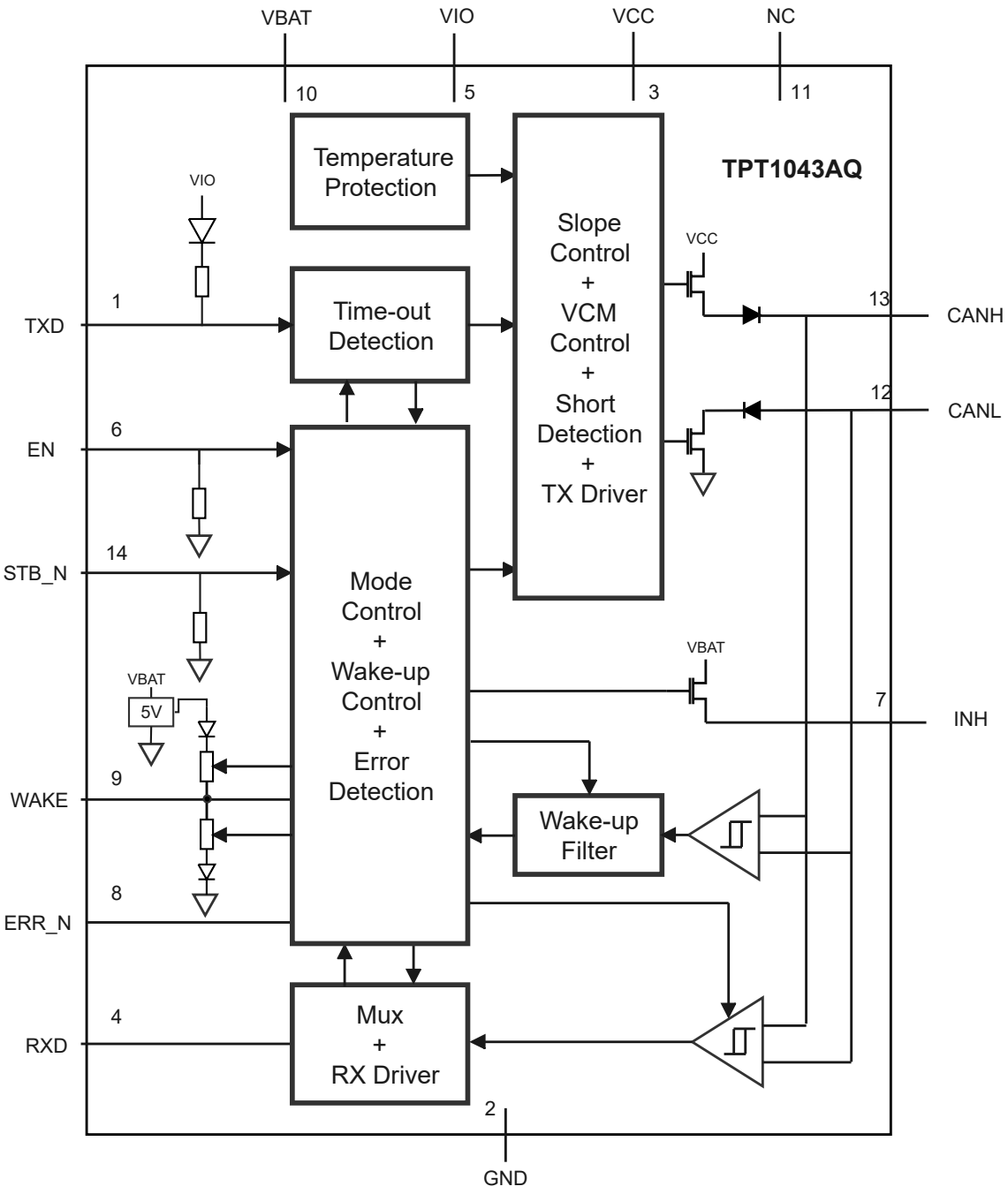


Figure 6. Functional Block Diagram

Feature Description

Table 2. Driver Function Table

Device Mode	Inputs	Outputs		Driven BUS State
	TXD	CANH	CANL	
Normal	L	H	L	Dominant
	H or Open	Z	Z	Bus biased to VCC/2
Silent	X	Z	Z	Bus biased to VCC/2
Standby	X	Z	Z	Bus biased to GND
Go-to-Sleep	X	Z	Z	Bus biased to GND
Sleep	X	Z	Z	Bus biased to GND

Table 3. Receiver Function Table

Device Mode	CAN Differential Inputs $VID = V_{CANH} - V_{CANL}$	BUS State	RXD Terminal
Normal or Silent	$V_{ID} \geq V_{TH\_RX\_DIF+(MAX)}$	Dominant	L
	$V_{TH\_RX\_DIF-(MIN)} < V_{ID} < V_{TH\_RX\_DIF+(MAX)}$	Indeterminate	Indeterminate
	$V_{ID} \leq V_{TH\_RX\_DIF-(MIN)}$	Recessive	H
	Open ($V_{ID} \approx 0$ V)	Open	H
Standby or Sleep	$V_{ID} \geq V_{TH\_RX\_DIF+(MAX)}$	Dominant	H, transition to L if the wake flag has been set
	$V_{TH\_RX\_DIF-(MIN)} < V_{ID} < V_{TH\_RX\_DIF+(MAX)}$	Indeterminate	
	$V_{ID} \leq V_{TH\_RX\_DIF-(MIN)}$	Recessive	
	Open ($V_{ID} \approx 0$ V)	Open	

Device Operating Modes

The device has 5 operating modes: normal mode, standby mode, silent mode, go-to-sleep mode, and sleep mode. Operating mode selection is made via the EN pin and the STB_N pin and wake-up events when the power supply is valid.

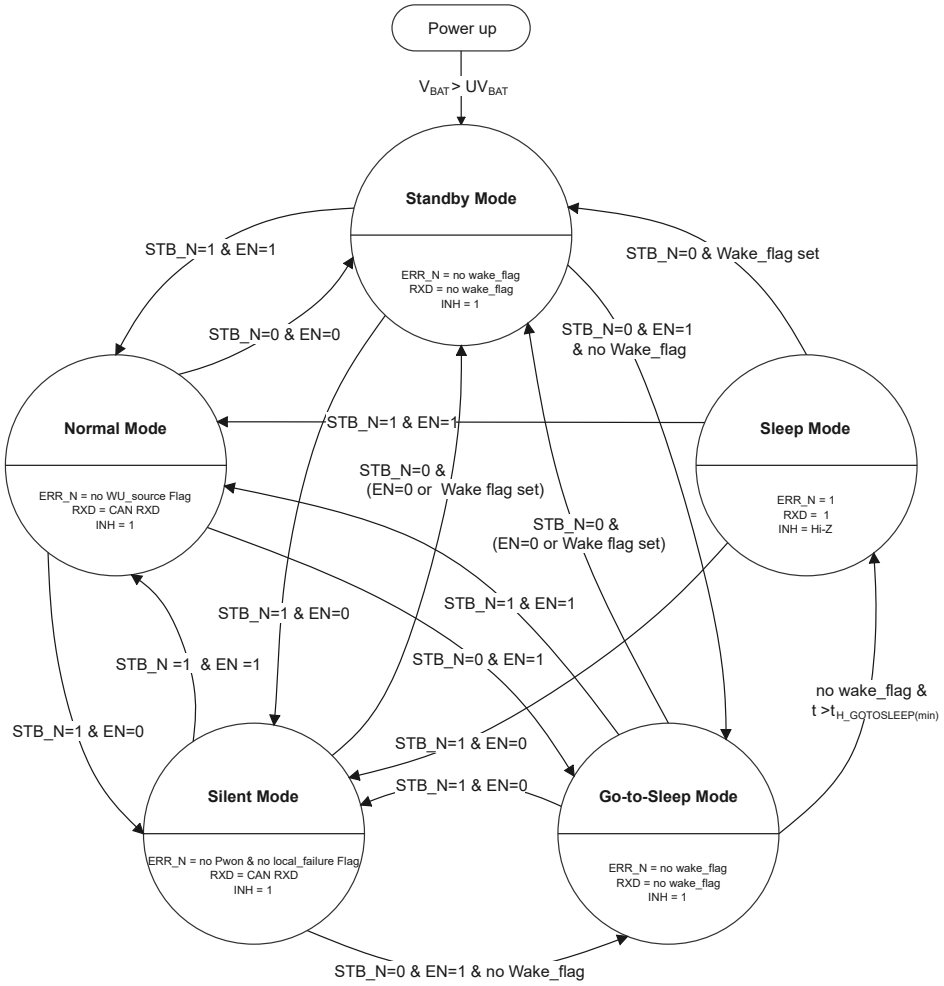


Figure 7. Mode Transition State Diagram

Normal Mode

This is the normal operating mode of the device. In the normal mode, the CAN driver and receiver blocks are fully operational. The transceiver transmits and receives data via the bus lines CANH and CANL. The driver translates the digital input data on the TXD pin to differential analog output on the CAN bus. The receiver translates the differential analog data on the CAN bus to digital data output to the RXD pin. The slopes of the CAN bus output signals are controlled by an internal circuit that optimizes the Electro Magnetic Emission (EME) performance. The CAN bus pin is biased to the 1/2 VCC voltage. The INH pin is active to enable the voltage regulated controlled by the INH pin.

Silent Mode

This is the listen-only mode and receive-only mode of the device. In the silent mode, the driver is disabled, releasing the bus pins to a recessive state. All other blocks, including the receiver, continue to operate in the normal mode. The silent mode can be used to prevent a faulty CAN controller from disrupting CAN bus network communications. The CAN bus pin is biased to the 1/2 VCC voltage. The INH pin is active to enable the voltage regulated controlled by the INH pin.

Standby Mode

This is the first level of the low-power mode. In the standby mode, the driver and receiver of the CAN transceiver are disabled, and the device is unable to transmit or receive data. The low-power receiver monitors bus activity for valid wake-up requirements. The CAN bus pin is biased to the ground. The INH pin is active to enable the voltage regulator controlled by the INH pin. The pin RXD reflects active wake-up requests as that V_{IO} and V_{BAT} are powered.

Go-to-Sleep Mode

This is the transitional mode between any mode and sleep mode. In the go-to-sleep mode, the driver and receiver of CAN transceiver are disabled, and the device is unable to transmit or receive data. The device transitions to sleep mode and the INH pin floats if the device is in the go-to sleep mode longer than $t_{H\_GOTOSLEEP}$. The device does not enter sleep mode if the wake flag is set.

Sleep Mode

This is the second level of low-power mode as well as the lowest power mode. Sleep mode is entered via Go-to-Sleep mode, and the device also enters sleep mode if VIO remains below UV_{VIO} for t_{UVD} or VCC remains below UV_{VCC} for t_{UVD}. In the sleep mode, the driver and receiver of the CAN transceiver are disabled, and the device is unable to transmit or receive data. The low-power receiver is monitoring bus activity for valid wake-up requirements. The CAN bus pin is biased to the ground. The INH pin is floating to disable the voltage regulator controlled by the INH pin for additional system-level power saving. The EN and STB_N pins can be used to change modes.

Internal Flags

The TPT1043A has 6 Internal flags to support system diagnosis, 4 of these flags can output via ERR_N to allow the MCU to determine the status of the device and the system.

Table 4. Internal flags via ERR_N

Internal Flag	Description	Available on ERR_N	Flag is cleared
UV_{NOM}	UV_{NOM} is the V_{CC} and V_{IO} under-voltage detection flag	No	Setting the Pwon or Wake flags, by a LOW-to-HIGH transition on STB_N or when both V_{IO} and V_{CC} have recovered.
UV_{BAT}	UV_{BAT} is the V_{BAT} under-voltage detection flag	No	V_{BAT} has recovered
P_{WON}	P_{WON} is the V_{BAT} power-on flag	In silent mode	Entering normal mode
Wake	The Wake flag is set when the transceiver detects a local or remote wake-up request.	In standby mode, go-to-sleep mode, and sleep mode	Entering normal mode or by setting the UV_{NOM} flag
Wake-up source	Wake-up source recognition is provided via the wake-up source flag, which is set when the wake flag is set by a local wake-up request via the wake pin.	In normal mode	Leaving normal mode

Internal Flag	Description	Available on ERR_N	Flag is cleared
Local failure	The four local failure events cause the local failure flag to be set: TXD dominant clamping, TXD-to-RXD short circuit, bus dominant clamping, and an overtemperature event.	In silent mode	Entering the normal mode or when RXD is dominant while TXD is recessive or by setting the P_{WON} flag

Remote Wake-up

A dedicated wake-up pattern (ISO11898-2:2024) wakes up the TPT1043A from standby mode or sleep mode. This filtering prevents the device from being woken up by noise or spikes on the bus.

The wake-up pattern consists of the following:

- a dominant phase of at least t_{WAKE_BUSDOM} followed by
- a recessive phase of at least t_{WAKE_BUSREC} followed by
- a dominant phase of at least t_{WAKE_BUSDOM}

The complete wake-up pattern must be received within $t_{WAKE\_BUS\_TO}$, otherwise, the wake-up logic will be reset to wait for the next valid wake-up pattern.

Device Local Faults

TXD Dominant Time-out

The device is featured with the TXD dominant time-out detection function. This function prevents a permanent low on the TXD pin, resulting in the CAN bus being driven into permanent dominance, which causes the CAN bus network communication to be blocked. If the TXD remains low for longer than t_{TXD_DTO}, the transmitter is disabled until the fault flag has been cleared.

TXD Shorted to RXD Detection

The device is featured with the function of a short circuit between TXD and RXD detection. This function prevents the CAN bus from being locked in permanent dominance, which results in the CAN bus network communication being blocked. The transmitter is disabled until the fault flag has been cleared.

Bus Dominant Time-out

The device features the bus-dominant time-out detection function. This function prevents the CAN bus from being locked in permanent dominance, which results in the CAN bus network communication being blocked. The fault flag is set if the CAN bus remains dominant for longer than t_{BUS_DTO}, and is released as soon as the bus returns to recessive.

Over-Temperature Protection (OTP)

The device integrates over-temperature protection circuit to prevent the device from over-heated induced damage. When the junction temperature is higher than the over-temperature protection threshold T_{OTP}, the device shuts down until the junction temperature T_J drops below the recovery threshold.

Under-Voltage Lockout (UVLO)

The device integrates an under-voltage detect and lockout circuit of the supply terminal to keep the device in the protected mode if the supply voltage drops below the threshold until the supply voltage is higher than the UVLO threshold. This protects the device and system during under-voltage events on supply terminals.

- UV_{NOM} is the VCC and VIO under-voltage detection flag. This flag is set when VCC falls below UV_{VCC} for t > t_{UVD}, or VIO falls below UV_{VIO} for t > t_{UVD}. When triggered, the device enters Sleep mode to conserve power and to ensure the bus is not disturbed. The flag is cleared when the Pwon or Wake flags are set by a LOW-to-HIGH transition on STB_N or when both VIO and VCC have recovered for t >t_{UVR}.
- UV_{BAT} is the VBAT under-voltage detection flag. When triggered, the transceiver attempts to enter Standby mode to conserve power. The flag is cleared when VBAT has recovered.

These Flags are internal and not reported via the ERR_N pin.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT1043A device is a CAN transceiver to support CAN FD function up to 8 Mbps, with BUS protection voltage from –45 V to +45 V, over-temperature shutdown. The VIO of the TPT1043A can support the voltage level of TXD and RXD from 1.7 V to 5.5 V, and V_{BAT} is from the battery power supply. The following sections show a typical application of the TPT1043A.

Typical Application

Figure 8 shows the typical application schematic of the TPT1043A.

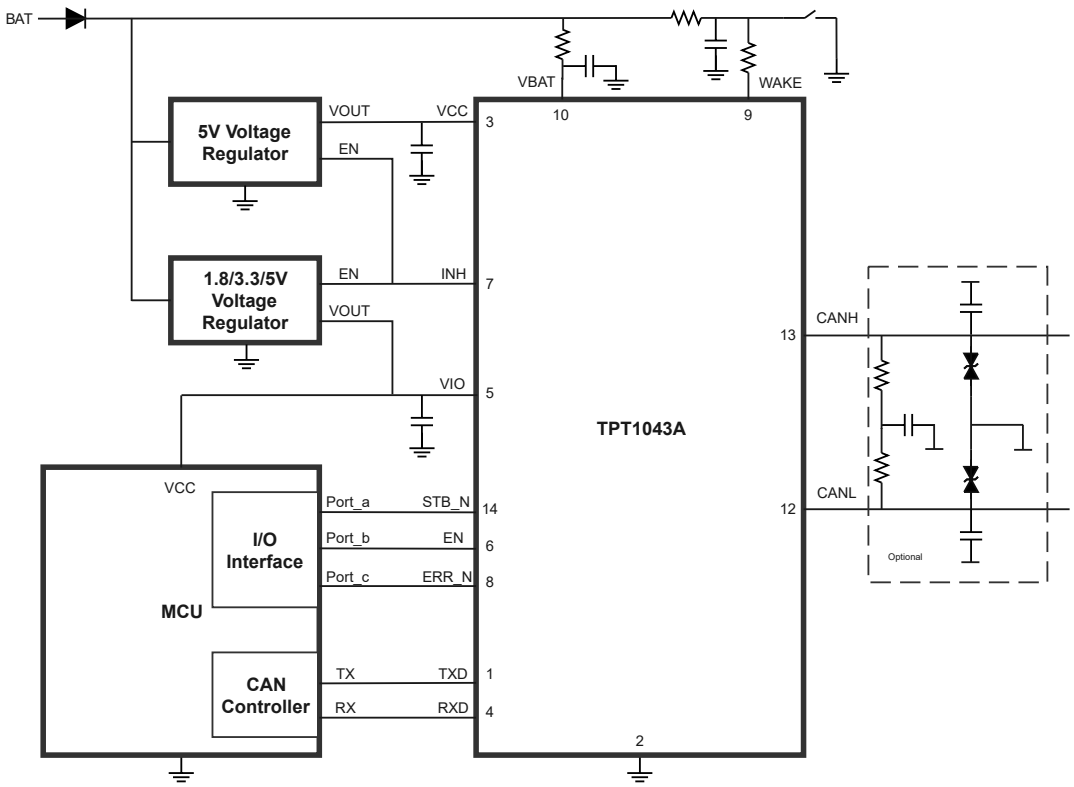
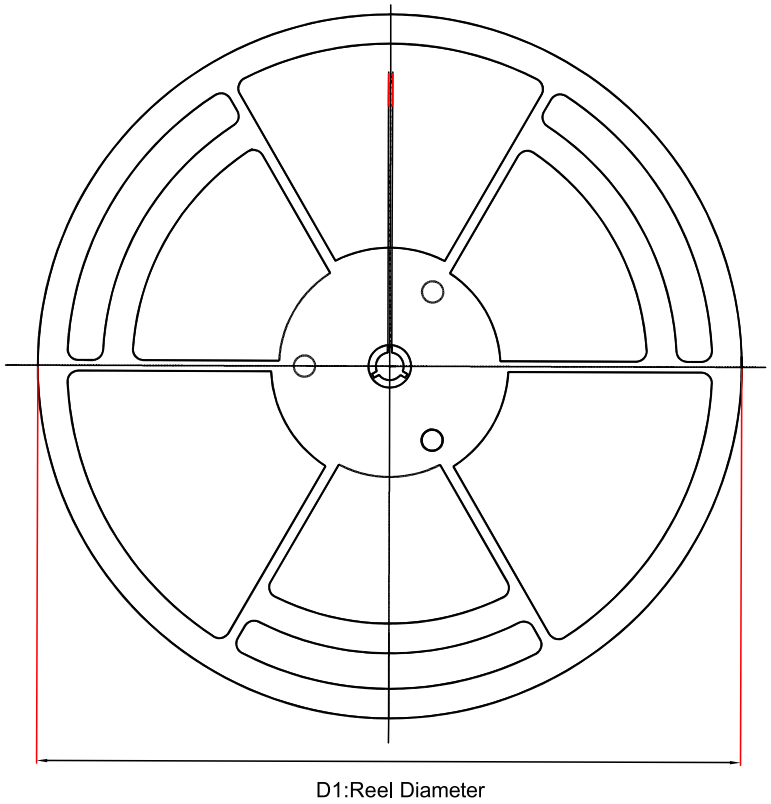
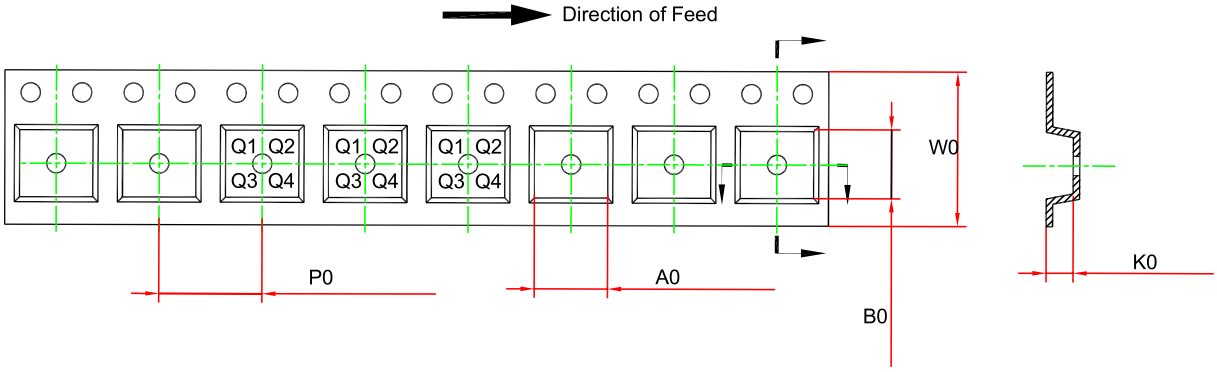


Figure 8. Typical Application Circuit

Tape and Reel Information



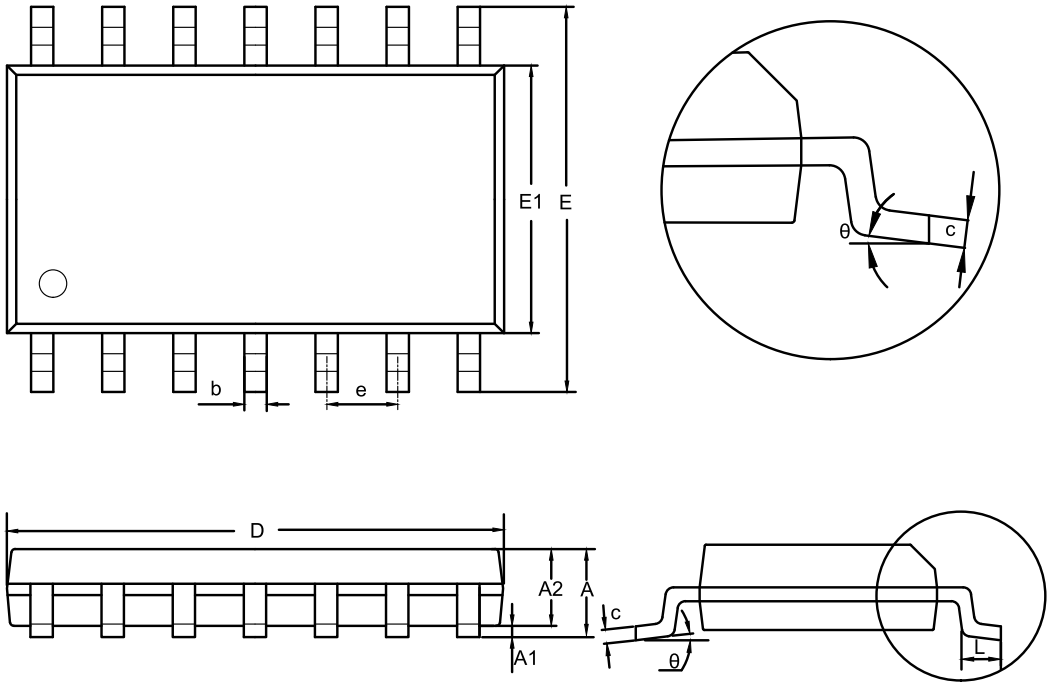


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT1043AQ-SO2R-S	SOP14	330	21.6	6.5	9.0	2.1	8.0	16	Q1
TPT1043AQ-DFKR-S	DFN4.5X3-14	330	17.6	3.3	4.8	1.1	8.0	12	Q1

Package Outline Dimensions

SOP14

Package Outline Dimensions SO2(SOP-14-A)



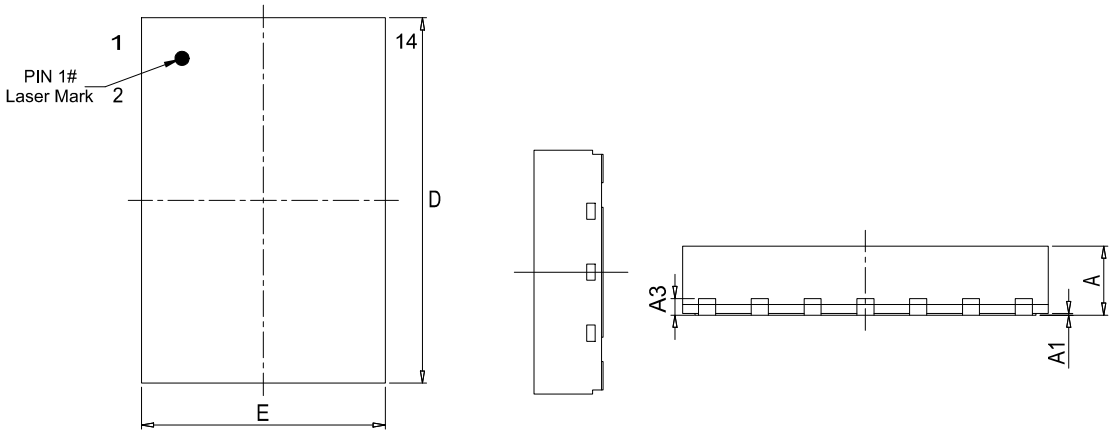
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0	8°	0	8°

NOTES

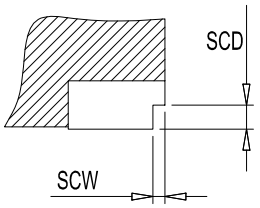
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN4.5X3-14

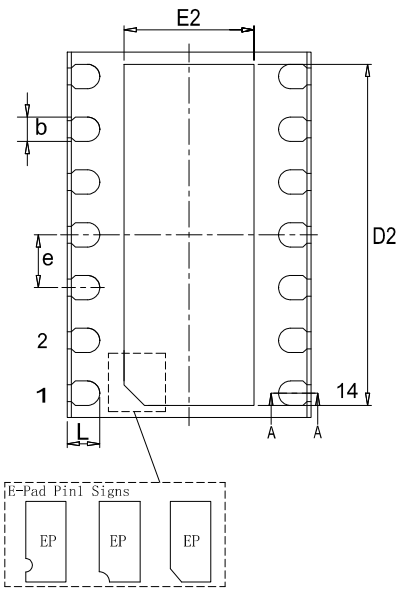
Package Outline Dimensions DFK(DFN4.5X3-14-WET-B)



TOP VIEW SIDE VIEW SIDE VIEW



DETAIL A



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.250	0.350	0.010	0.014
A3	0.203 REF		0.008 REF	
D	4.400	4.600	0.173	0.181
E	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.300	0.500	0.012	0.020
D2	4.100	4.300	0.161	0.169
E2	1.500	1.700	0.059	0.067
SCW	0.010	0.090	0.0004	0.004
SCD	0.080	0.180	0.003	0.007

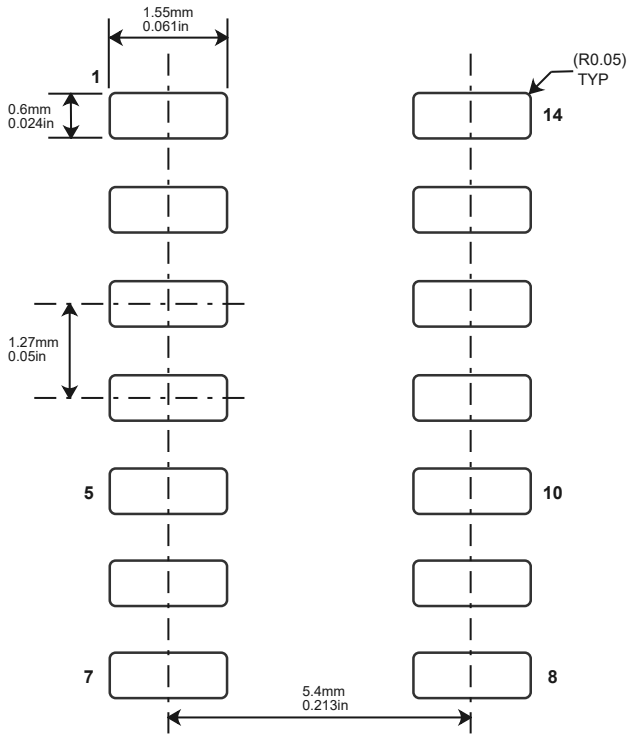
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Example Board Layout

SOP14

EXAMPLE BOARD LAYOUT **SOP14**

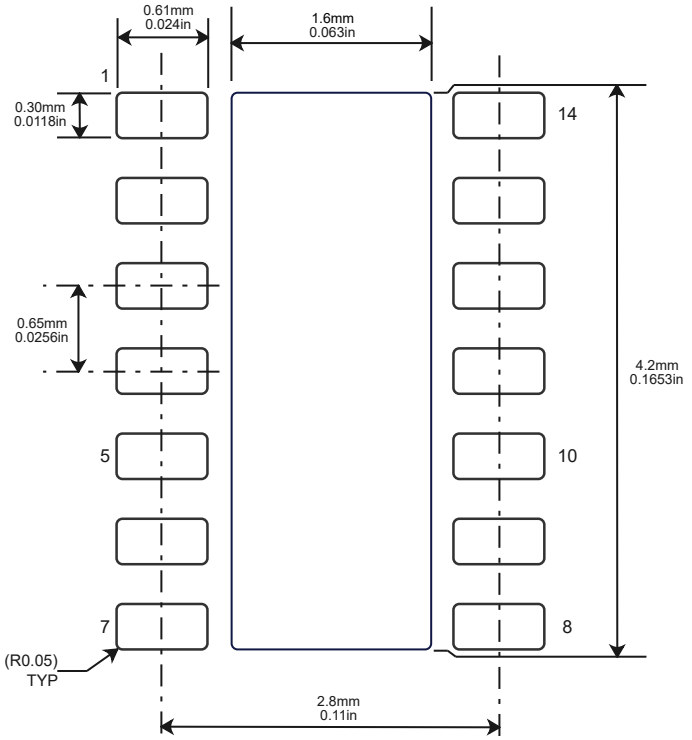


LAND PATTERN EXAMPLE

NOTES
1.This drawing is for design reference only.
2.This drawing is subject to change without notice.

DFN4.5X3-14

EXAMPLE BOARD LAYOUT **DFN4.5X3-14**



LAND PATTERN EXAMPLE

NOTES
1.This drawing is for design reference only.
2.This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT1043AQ-SO2R-S	−40 to 125°C	SOP14	T143AQ	MSL1	Tape and Reel, 2500	Green
TPT1043AQ-DFKR-S	−40 to 125°C	DFN4.5X3-14	T143AQ	MSL1	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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