Automotive Fault Protected LIN Transceiver with TXD Dominant Timeout

Features

- Compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO 17987-4 Electrical Physical Layer (EPL) Specification
- Compliant to SAE J2602 LIN Network for Vehicle Applications
- Support LIN Data Rates up to 20 Kbps
- Wide V_{BAT} Input Voltage Range Supports 5.5 V to 40 V
- Low-current Standby Mode and Sleep Mode with Bus Wake-up Capability
- Input Levels Compatible with 3.3 V and 5 V MCU Interface
- Ideal Passive Behavior to LIN Bus when Unpowered
- Integrated Pull-up Resistor for LIN Slave Applications
- Protection Feature：
  - Bus Pin IEC 61000-4-2 ESD Protection ±15 kV
  - Bus Fault Tolerant ±45 V
  - V_{BAT} Undervoltage Protection
  - TXD Dominant Time-out Function
  - Thermal Shutdown Protection
- Available in SOP8 Package and Leadless DFN3X3-8 Package with Improved Automated Optical Inspection (AOI) Capability
- AEC-Q100 Qualified for Automotive Applications, Grade 1

Applications

- Automotive and Transportation
- Body Electronics / Lighting
- Power Train / Chassis
- Infotainment / Cluster
- ADAS / Safety

Description

The TPT1029Q is a local interconnect network (LIN) physical layer transceiver that is compliant with the ISO 17987-4, SAE J2602 and LIN 2.0, LIN 2.1, LIN 2.2, and LIN 2.2-A physical layer standard. LIN is a low-speed universal asynchronous receiver transmitter (UART) communication protocol that supports automotive in-vehicle sub-networks.

The device supports LIN networks up to 20 Kbps with an enhanced timing margin. The device converts the transmitted data received at the TXD with the optimized slew rate to minimize the electro-magnetic emission (EME) and reports the state of the LIN bus at the RXD.

As designed, the device features overvoltage and loss of ground protection from −45 V to +45 V, overtemperature shutdown. The device has low-current standby and sleep mode with LIN BUS wake-up capability. The device integrates a pull-high resistor for LIN slave applications and ESD protection which allows applications to operate with a reduced dependence on external components. Additionally, all devices include many protection features to enhance the device and network robustness.

The TPT1029Q is available in SOP8 and DFN3X3-8 packages and is AEC-Q100 qualified for automotive applications.

Typical Application Circuit

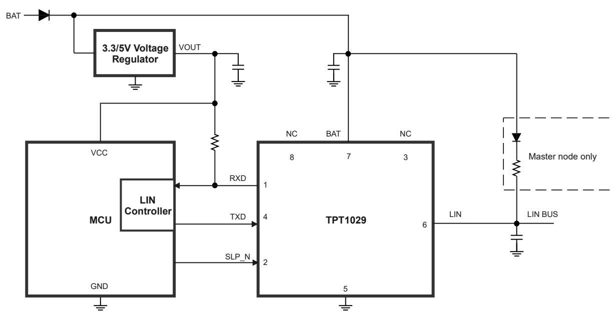


Table of Contents

Features 1
Applications 1
Description 1
Typical Application Circuit 1
Revision History 3
Pin Configuration and Functions 4
Specifications 5
- Absolute Maximum Ratings 5
- ESD (Electrostatic Discharge Protection) 5
- Recommended Operating Conditions 6
- Thermal Information 6
- Electrical Characteristics 7
- Duty Cycles 9
- AC Timing Requirements 10

Parameter Measurement Information 11
- Test Circuit 11
- Parameter Diagram 11

Detailed Description 13
- Overview 13
- Functional Block Diagram 13
- Feature Description 13
  - Device Operating Modes 13
  - Protection Features 15

Application and Implementation 16
- Typical Application 16

Tape and Reel Information 17
Package Outline Dimensions 18
- SOP8 18
- DFN3X3-8 19

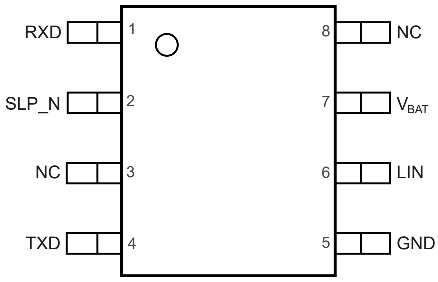
Order Information 20
IMPORTANT NOTICE AND DISCLAIMER 21

Revision History

Date	Revision	Notes
2022-12-05	Rev.Pre.0	Initial version
2024-9-26	Rev.A.0	Release version

Pin Configuration and Functions

TPT1029Q
SOP8 Package
Top View



TPT1029Q
DFN3X3-8 Package
Top View

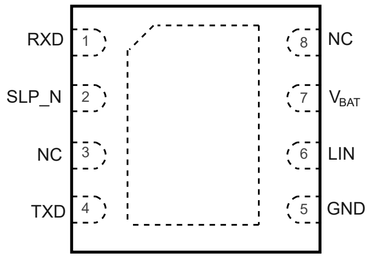


Table 1. Pin Functions: TPT1029

Pin		I/O	Description
No.	Name		
1	RXD	Output	LIN receives data output
2	SLP_N	Input	Sleep mode control input, active low
3	NC	NC	Not connected
4	TXD	Input	LIN transmits data input
5	GND	GND	Ground
6	LIN	BUS I/O	LIN Bus input/output line
7	VBAT	Power	High voltage power supply from the battery
8	NC	NC	Not connected

Specifications

Absolute Maximum Ratings

Parameter		Conditions	Min	Max	Unit
V_{BAT}	Battery Supply Voltage Range		−0.3	45	V
V_{TXD}	Pin TXD Voltage Range		−0.3	7	V
V_{RXD}	Pin RXD Voltage Range		−0.3	7	V
V_{SLP_N}	Pin SLP_N Voltage Range		−0.3	7	V
V_{LIN}	Pin LIN Voltage Range	With respect to GND	−45	45	V
T_J	Junction Temperature (2)		−40	150	°C
T_{STG}	Storage Temperature		−55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC standard multilayer test boards.

ESD (Electrostatic Discharge Protection)

Parameter		Condition	Min	Max	Unit
V_{ESD}	Electrostatics Discharge (1)(2)	IEC61000-4-2 (150 pF, 330 Ω discharge circuit), contact discharge on LIN bus pin	−15	15	kV
		Human Body Model (HBM) on LIN bus pin	−15	15	kV
		Human Body Model (HBM) on any other pins	−6	6	kV
		Charged Device Model (CDM) on all pins	−1.5	1.5	kV
V_{TRAN}	Transient Immunity ISO 7637-2 on Bus Pins	Pulse1	−100		V
		Pulse2a		75	V
		Pulse3a	-150		V
		Pulse3b		100	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

	Parameter	Min	Max	Unit
V_{BAT}	Battery Power Supply	5.5	40	V
V_{LIN}	LIN Bus Input Voltage	0	40	V
V_{LOGIC}	Logic Pin Voltage	0	5.25	V
T_J	Operating Virtual Junction Temperature Range	−40	150	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8	118	48	°C/W
DFN3x3-8	51	23	°C/W

Electrical Characteristics

All test conditions: V_{BAT}= 5.5 V to 40 V, R_L= 500 Ω, T_A= −40°C to 125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Pin VBAT						
$V_{TH\_VBAT\_L}$	Low Level of VBAT UVLO Threshold Voltage		3.50	4.30		V
$V_{TH\_VBAT\_H}$	High Level of VBAT UVLO Threshold Voltage			4.45	5.20	V
V_{HYS_VBAT}	Hysteresis Voltage on Power-on Reset (1)			0.15		V
I_{BAT}	Sleep Mode Supply Current	V_{LIN} = V_{BAT}; V_{TXD} = 0 V; V_{SLP_N} = 0 V		5.9	11	μA
	Standby Mode Supply Current	Recessive; V_{LIN} = V_{BAT}; V_{TXD}= 5 V; V_{SLP_N} = 0 V		21	30	μA
		Dominant; V_{LIN} =0 V; V_{TXD} = 0 V; V_{SLP_N} = 0 V		0.44	1.9	mA
	Normal Mode Supply Current	Recessive; V_{LIN} =V_{BAT}; V_{TXD} = 5 V; V_{SLP_N} = 5 V		157	300	μA
		Dominant; V_{LIN}=0 V; V_{TXD}= 0 V; V_{SLP_N} = 5 V		1.6	6.4	mA
Pin TXD						
V_{IH}	High-Level Input Voltage		2		7	V
V_{IL}	Low-Level Input Voltage		−0.3		0.8	V
V_{HYS_TXD}	Hysteresis Voltage on Pin TXD		50	200	400	mV
R_{PD_TXD}	Pin TXD Pull down Resistance	V_{TXD} = 5 V	140	500	1200	kΩ
I_{IL}	Low-Level Input Current	V_{TXD} = 0 V	−5		5	μA
Pin SLP_N						
V_{IH}	High-Level Input Voltage		2		7	V
V_{IL}	Low-Level Input Voltage		−0.3		0.8	V
$V_{HYS\_SLP\_N}$	Hysteresis Voltage on Pin SLP_N		50	200	400	mV
$R_{PD\_SLP\_N}$	Pin SLP_N Pull-down Resistance	V_{SLP_N} = 5 V	140	500	1200	kΩ
I_{IL}	Low-Level Input Current	V_{SLP_N} = 0 V	−5		5	μA
Pin RXD						
I_{OL}	Low-Level Output Current	Normal mode; V_{LIN} = 0 V, V_{RXD} = 0.4 V	1.5	4.2		mA
I_{LH}	High-Level Leakage Current	Normal mode; V_{LIN} = V_{BAT}, V_{RXD} = 5 V	−5	0	5	μA

Parameter		Conditions	Min	Typ	Max	Unit
Pin LIN						
I_{BUS_LIM}	Dominant Output Current Limitation	V_{BAT} = V_{LIN} = 18 V; V_{TXD} = 0 V	40		170	mA
$I_{BUS\_PAS\_REC}$	Receiver Recessive Input Leakage Current	V_{BAT} = 5.5 V; V_{LIN} = 27 V; V_{TXD} = 5 V			20	μA
$I_{BUS\_PAS\_DOM}$	Receiver Dominant Input Leakage Current	Normal mode; V_{BAT} = 12 V; V_{LIN} = 0 V; V_{TXD} = 5 V	−600			μA
$V_{SerDiode}$	Voltage Drop at the Serial Diode (1)	Pull-up path with R_{SLAVE}; $I_{SerDiode}$ = 10 μA	0.4		1	V
$I_{BUS\_NO\_GND}$	Ground Loss Bus Current	V_{BAT} = 12 V; V_{LIN} = 0 V	−850		10	μA
$I_{BUS\_NO\_BAT}$	Battery Loss Bus Current	V_{BAT} = 0 V; V_{LIN} = 40 V			20	μA
V_{BUS_DOM}	Receiver Dominant				0.4 x V_{BAT}	V
V_{BUS_REC}	Receiver Recessive		0.6 x V_{BAT}			V
V_{BUS_CNT}	Receiver Center Voltage		0.475 x V_{BAT}	0.5 x V_{BAT}	0.525 x V_{BAT}	V
V_{HYS}	Receiver Hysteresis Voltage				0.175 x V_{BAT}	V
R_{SLAVE}	Slave Resistance	Between LIN and V_{BAT}; V_{BAT} = 12 V; V_{LIN} = 0 V	20	30	47	kΩ
C_{LIN}	Pin LIN Capacitance (1)				20	pF
V_{O_REC}	Recessive Output Voltage	Normal mode; V_{TXD} = V_{CC}	0.85 x V_{BAT}			
V_{O_DOM}	Dominant Output Voltage	Normal mode; V_{TXD} = 0 V			1.4	V
Temperature Detection						
T_{J_SD}	Shutdown Junction Temperature		160	180	200	℃
$T_{J\_SD\_R}$	Recover Shutdown Junction Temperature		125		160	℃

Duty Cycles

All test conditions: V_{BAT} = 5.5 V to 40 V, R_L = 500 Ω, T_A = −40°C to 125°C, see Figure 2, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
D1	Duty cycle 1; D1 = $t_{BUS\_REC\_MIN}$/ 2 x t_{BIT}	$V_{TH\_REC\_MAX}$ = 0.744 x V_{BAT}; $V_{TH\_DOM\_MAX}$ = 0.581 x V_{BAT}; 20 kbps; t_{BIT} = 50 µs; 7 V ≤ V_{BAT} ≤ 40 V	0.396			
D1	Duty cycle 1; D1 = $t_{BUS\_REC\_MIN}$/ 2 x t_{BIT}	$V_{TH\_REC\_MAX}$ = 0.744 x V_{BAT}; $V_{TH\_DOM\_MAX}$ = 0.581 x V_{BAT}; 20 kbps; t_{BIT} = 50 µs; 5.5 V ≤ V_{BAT} < 7 V	0.396			
D2	Duty cycle 2; D2 = $t_{BUS\_REC\_MAX}$/ 2 x t_{BIT}	$V_{TH\_REC\_MIN}$ = 0.422 x V_{BAT}; $V_{TH\_DOM\_MIN}$ = 0.284 x V_{BAT}; 20 kbps; t_{BIT} = 50 µs; 7.6 V ≤ V_{BAT} ≤ 40 V			0.581	
D2	Duty cycle 2; D2 = $t_{BUS\_REC\_MAX}$/ 2 x t_{BIT}	$V_{TH\_REC\_MIN}$ = 0.464 x V_{BAT}; $V_{TH\_DOM\_MIN}$ = 0.312 x V_{BAT}; 20 kbps; t_{BIT}= 50 µs; 5.5 V ≤ V_{BAT} < 7.6 V			0.581	
D3	Duty cycle 3; D3 = $t_{BUS\_REC\_MIN}$/ 2 x t_{BIT}	$V_{TH\_REC\_MAX}$ = 0.778 x V_{BAT}; $V_{TH\_DOM\_MAX}$ = 0.616 x V_{BAT}; 10.4 kbps; t_{BIT} = 96 µs; 7 V ≤ V_{BAT} ≤ 40 V	0.417			
D3	Duty cycle 3; D3 = $t_{BUS\_REC\_MIN}$/ 2 x t_{BIT}	$V_{TH\_REC\_MAX}$ = 0.778 x V_{BAT}; $V_{TH\_DOM\_MAX}$ = 0.616 x V_{BAT}; 10.4 kbps; t_{BIT} = 96 µs; 5.5 V ≤ V_{BAT} < 7 V	0.417			
D4	Duty cycle 4; D4 = $t_{BUS\_REC\_MAX}$/ 2 x t_{BIT}	$V_{TH\_REC\_MIN}$ = 0.389 x V_{BAT}; $V_{TH\_DOM\_MIN}$ = 0.251 x V_{BAT}; 10.4 kbps; t_{BIT} = 96 µs; 7.6 V ≤ V_{BAT} ≤ 40V			0.590	
D4	Duty cycle 4; D4 = $t_{BUS\_REC\_MAX}$/ 2 x t_{BIT}	$V_{TH\_REC\_MIN}$ = 0.389 x V_{BAT}; $V_{TH\_DOM\_MIN}$ = 0.251 x V_{BAT}; 10.4 kbps; t_{BIT} = 96 µs; 5.5 V ≤ V_{BAT} < 7.6 V			0.590	

AC Timing Requirements

All test conditions: V_{BAT} = 5.5 V to 40 V, R_L = 500 Ω, T_A = −40°C to 125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
t_F	Fall Time	C_{BUS} = 1 nF, R_{BUS} = 1 kΩ; C_{BUS} = 6.8 nF, R_{BUS} = 660 Ω; C_{BUS} = 10 nF, R_{BUS} = 500 Ω;			22.5	μs
t_R	Rise Time	C_{BUS} = 1 nF, R_{BUS} = 1 kΩ; C_{BUS} = 6.8 nF, R_{BUS} = 660 Ω, C_{BUS} = 10 nF, R_{BUS} = 500 Ω;			22.5	μs
$\Delta t_{(R-F)}$	Difference between Rise-and-Fall Time	V_{BAT} = 7.3 V	−5		5	μs
t_{TX_PD}	Transmitter Propagation Delay	Rising and falling			6	μs
t_{TX_SYM}	Transmitter Propagation Delay Symmetry	Rising edge with respect to falling edge	−3		3	μs
t_{RX_PD}	Receiver Propagation Delay	Rising and falling			6	μs
t_{RX_SYM}	Receiver Propagation Delay Symmetry	Rising edge with respect to falling edge	−2		2	μs
$t_{WAKE\_DOM\_LIN}$	LIN Dominant Wake-up Time	Sleep mode	30	80	150	μs
$t_{GOTONORM}$	Go-to-Normal Time	Mode change time from Sleep, Standby mode into Normal mode	2	5	10	μs
$t_{INITNORM}$	Normal Mode Initialization Time		5	12	20	μs
$t_{GOTOSLEEP}$	Go-to-Sleep Time	Mode change time from Normal into the Sleep mode	2	5	10	μs
$t_{TO\_DOM\_TXD}$	TXD dominant time-out time	V_{TXD} = 0 V	21	43	90	ms

(1) The data is based on bench tests and design simulations.

Parameter Measurement Information

Test Circuit

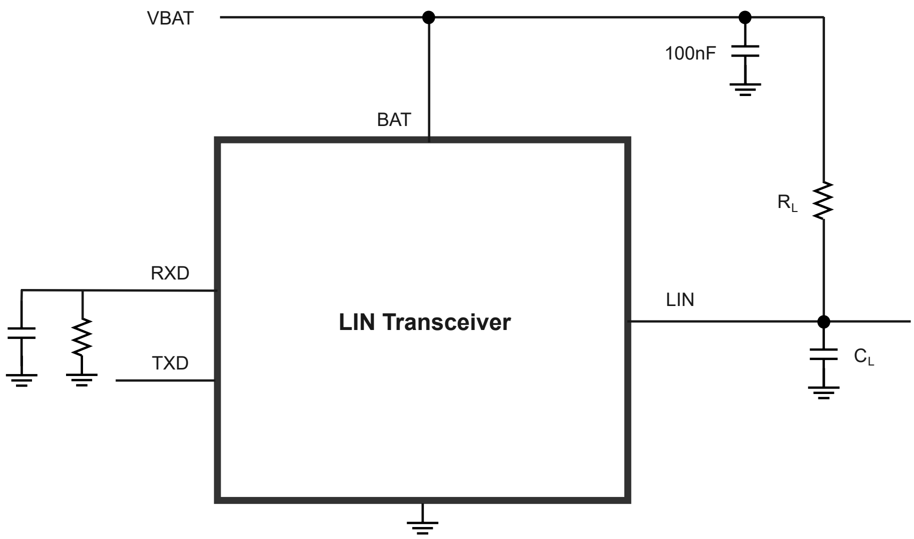


Figure 1. LIN Transceiver Timing Parameter Test Circuit

Parameter Diagram

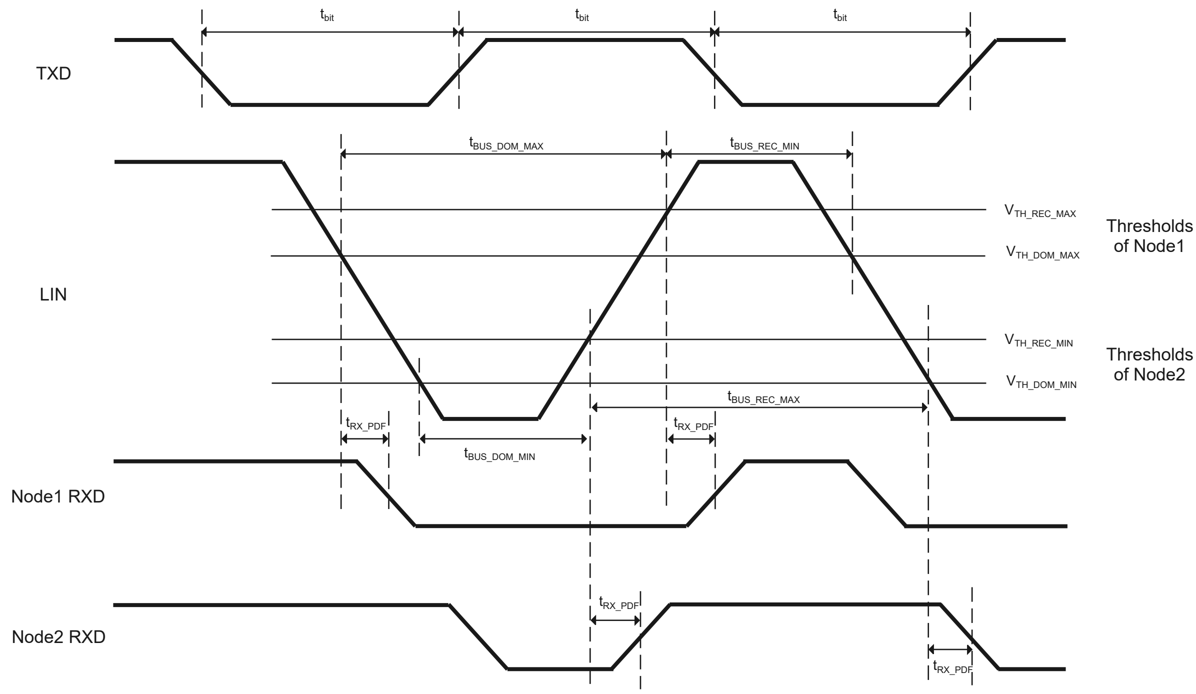


Figure 2. LIN Transceiver Timing Diagram

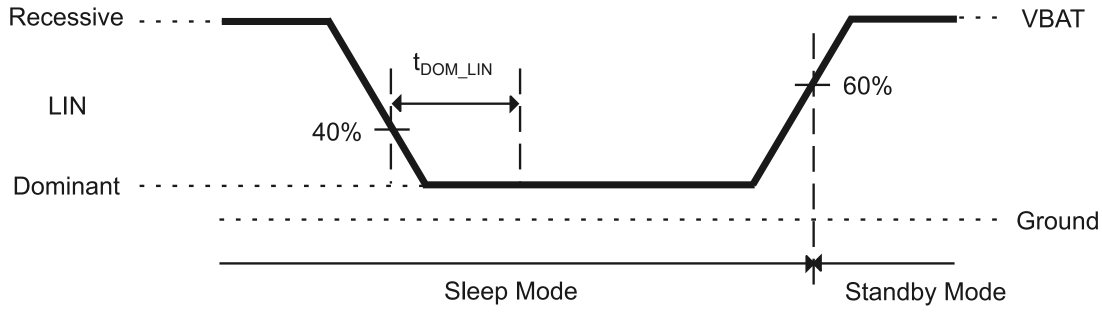


Figure 3. Remote Wake-up Diagram

Detailed Description

Overview

The TPT1029Q is a local interconnect network (LIN) physical layer transceiver that is compliant with the ISO 17987-4, SAE J2602 and LIN 2.0, LIN 2.1, LIN 2.2, and LIN 2.2-A physical layer standards. LIN is a low-speed universal asynchronous receiver transmitter (UART) communication protocol that supports automotive in-vehicle sub-networks. The device supports LIN networks up to 20 Kbps with an enhanced timing margin. The device converts the transmitted data received at the TXD with an optimized slew rate to minimize the electro-magnetic emission (EME) and reports the state of the LIN bus at the RXD. As designed, the device features overvoltage and loss of ground protection from −45 V to +45 V, overtemperature shutdown. The device has low-current standby and sleep mode with LIN BUS wake-up capability. The device integrates a pull-high resistor for LIN slave applications and ESD protection which allows applications to operate with reduced dependence on external components. Additionally, all devices include many protection features to enhance the device and network robustness. The TPT1029Q is available in SOP-8 and DFN3X3-8L packages and is AEC-Q100 qualified for automotive applications.

Functional Block Diagram

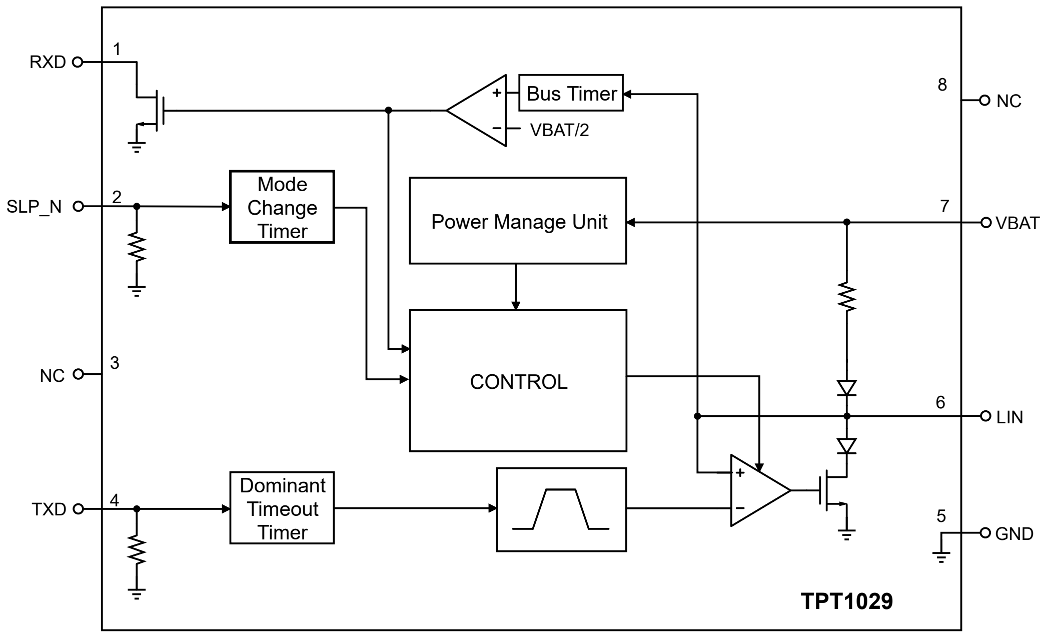


Figure 4. Functional Block Diagram

Feature Description

Device Operating Modes

The TPT1029Q supports modes for normal mode, power-on mode, standby mode, and sleep mode. The figure below shows the state diagram.

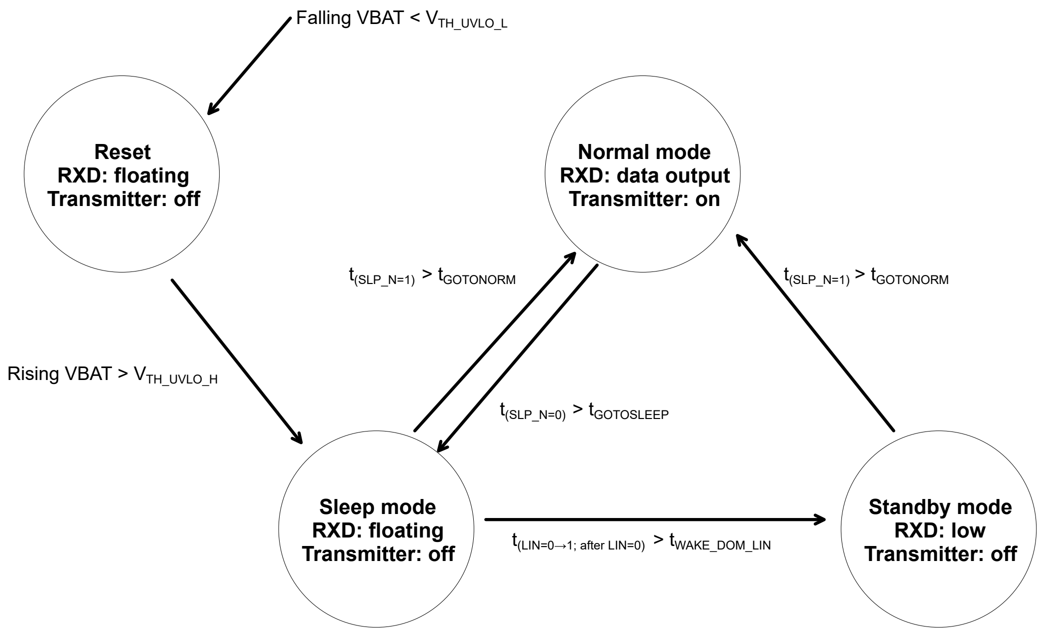


Figure 5. State Diagram

Table 2. Operation Mode Table

Mode	SLP_N	TXD	RXD	Transmitter	Comments
Normal	High	High: recessive state Low: dominant state	High: recessive state Low: dominant state	Normal	
Sleep	Low	Weak pull-down	Floating	Off	No wake-up event detected
Standby	Low	Weak pull-down	Low	Off	Wake-up event detected

Normal Mode

In Normal mode, the device can transmit and receive data through the LIN bus line. The receiver detects the data stream at the LIN bus input pin and transfers it to the microcontroller via the RXD pin. On the bus, a HIGH level corresponds to a recessive state, while a LOW level represents a dominant state. The receiver incorporates a voltage-dependent threshold with hysteresis and an integrated filter to suppress noise on the bus.

The transmit data stream from the protocol controller at the TXD input is converted by the transmitter into a bus signal with optimized slew rate and wave shaping, aiming to minimize electromagnetic emissions (EME). The LIN bus output pin is pulled HIGH through an internal slave termination resistor. For master applications, an external resistor in series with a diode should be connected between pin VBAT and pin LIN.

Sleep Mode

The device offers an energy-efficient mode known as the power-saving mode. Despite its extremely low current consumption, the device retains the capability to be remotely awakened via the LIN pin or directly activated through the SLP_N pin. Input filters are incorporated at the receiver (LIN), and SLP_N pin to prevent undesired wake-up events caused by automotive transients or electromagnetic interference (EMI).

To initiate Sleep mode from Normal mode, a falling edge on the SLP_N pin is required. In order to successfully enter Sleep mode, the sleep command (SLP_N pin set to LOW) must be sustained for a minimum duration of $t_{gotosleep}$.

During Sleep mode, the internal slave termination between the LIN and VBAT pins is disabled to minimize power dissipation if the LIN pin is short-circuited to ground. Only a weak pull-up is present between the LIN and VBAT pins.

When VBAT voltage drops below the undervoltage threshold, the device transitions into Sleep mode.

Standby Mode

Standby mode is indicated by a low level on the RXD pin, which can serve as an interrupt for the microcontroller.

Wake-up

When VBAT voltage exceeds the undervoltage threshold voltage, the device transitions into Sleep mode. In this mode, both the transmitter and receiver remain inactive. If SLP_N is HIGH for a duration greater than t_gotonorm, the device enters Normal mode.

To wake up a device that is in Sleep mode, there are two methods:

Remote wake-up through the LIN bus by receiving a dominant bus state that is sustained for a duration of at least $t_{WAKE_DOM_LIN}$then followed by a rising edge.

Mode change by setting the SLP_N pin to a HIGH level. This change in pin state signals the device to exit Sleep mode and enter Normal mode.

Protection Features

TXD Dominant Time-out

The device will detect TXD dominant time-out and prevent a permanent low on pin TXD driving the LIN bus into permanent dominant blocking the LIN bus network. If the TXD remains low for longer than t_{TXD_DTO} the transmitter will be disabled until the fault flag has been cleared.

Under-voltage Lockout (UVLO)

The device integrated under-voltage detect and lockout circuit of the supply terminal to keep the device in protected mode if the supply voltage drops below the threshold until the supply voltage is higher than the UVLO threshold. This protects the device and system during undervoltage events on supply terminals.

Over-Temperature Protection (OTP)

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{J_SD}, the output drivers will be disabled until the virtual junction temperature falls below $T_{J\_SD\_R}$ and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillation due to temperature drift is avoided.

Fail-safe Features

An internal pull-down to GND on the TXD pin to establish a predetermined level in case the TXD pin is disconnected.

An internal pull-down to GND on the SLP_N pin to establish a predetermined level in case the SLP_N pin is disconnected.

RXD pin is set floating when the VBAT pin is unpowered.

The current limit is applied to LIN transmitter output to protect LIN bus short circuits to VBAT or GND

VBAT and GND loss will not impact the LIN bus or the MCU. No reverse current flow from the bus into pin LIN. The internal integrated LIN slave termination resistor remains to keep the current path from VBAT to LIN. Disconnecting the LIN transceiver from the power supply does not affect the LIN bus.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

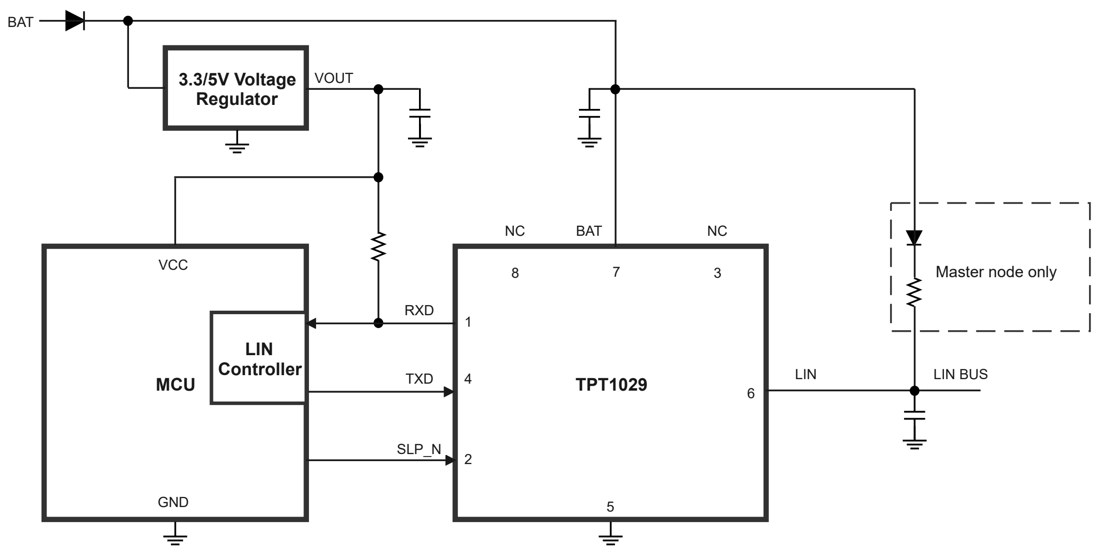
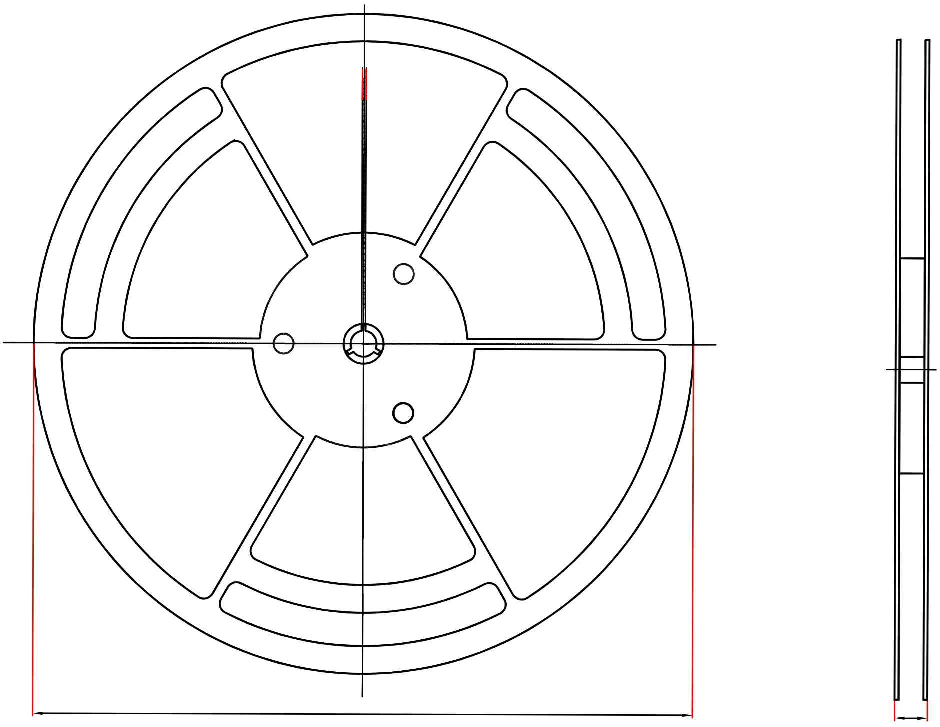
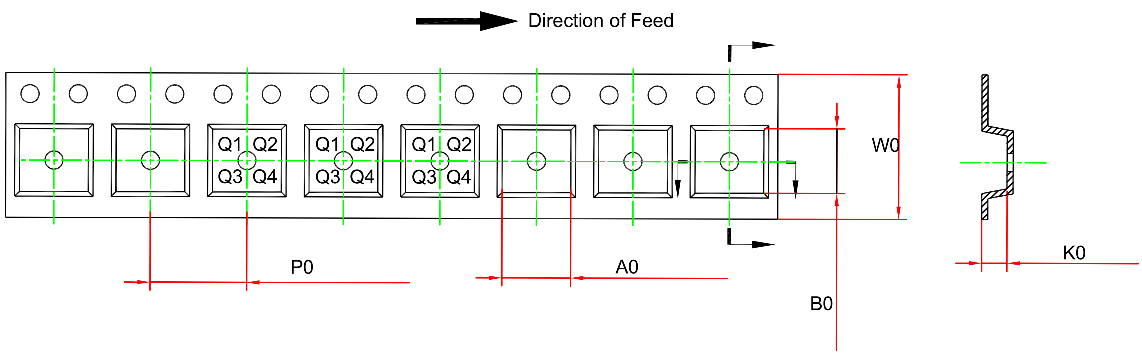


Figure 6. Typical Application Circuit

Tape and Reel Information



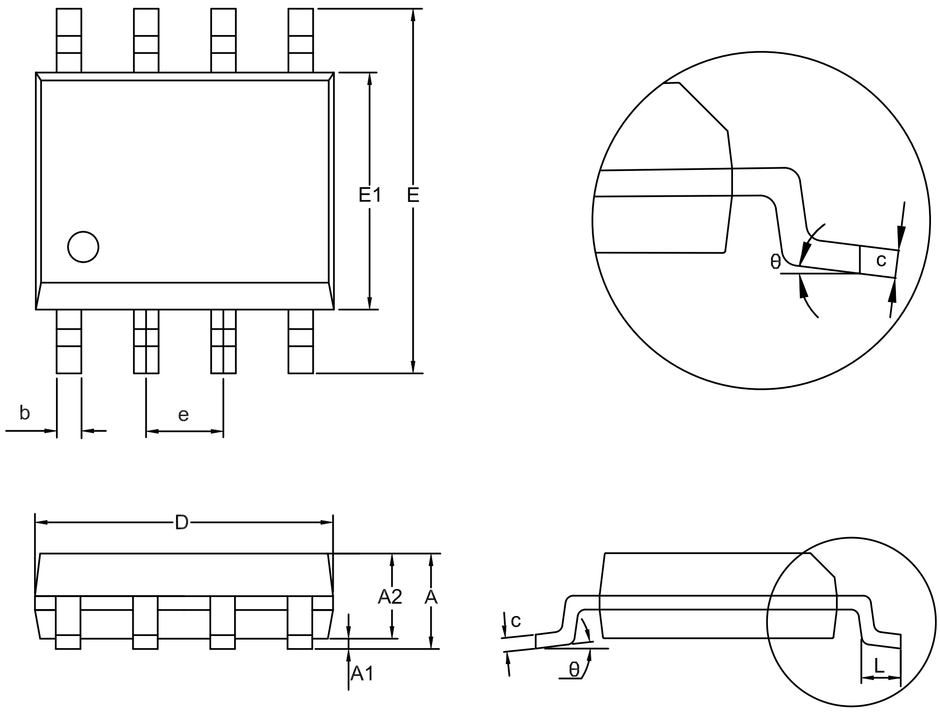


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPT1029Q-SO1R-S	SOP8	330.0	6.5	2.0	12.0	17.6	5.4	8.0	Q1
TPT1029Q-DFCR-S	DFN3x3-8	330.0	3.3	1.1	12.0	17.6	3.3	8.0	Q1

Package Outline Dimensions

SOP8

Package Outline Dimensions SO1(SOP-8-A)



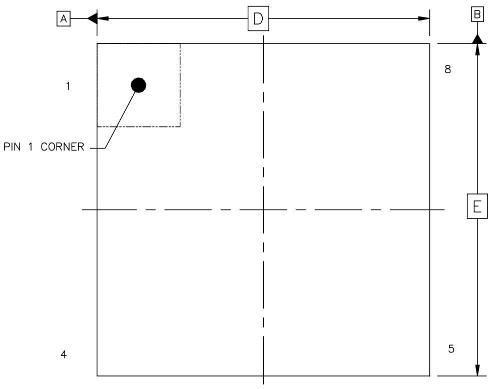
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

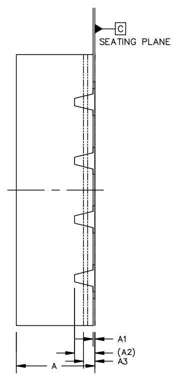
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN3X3-8

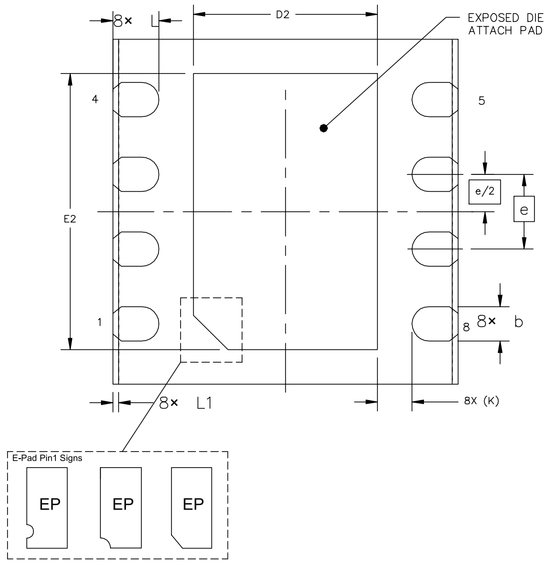
Package Outline Dimensions DFC(DFN3X3-8-WET-H)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
A2	0.150	0.250	0.006	0.010
A3	0.080	0.180	0.003	0.007
D	2.900	3.100	0.114	0.122
D2	1.500	1.700	0.059	0.067
E	2.900	3.100	0.114	0.122
b	0.250	0.350	0.010	0.014
E2	2.300	2.500	0.091	0.098
e	0.650 BSC		0.026 BSC	
L	0.350	0.450	0.014	0.018
L1	0.010	0.090	0.0004	0.004
K	0.300 REF		0.012 REF	

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT1029Q-SO1R-S	−40 to 125°C	SOP8	1029Q	MSL1	Tape and Reel, 4000	Green
TPT1029Q-DFCR-S	−40 to 125°C	DFN3x3-8	1029Q	MSL1	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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