Automotive Fault Protected 125mA LIN System Basis Chip (SBC)

Features

- Compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, and ISO 17987-4 Electrical Physical Layer (EPL) Specification
- Compliant to SAE J2602 LIN Network for Vehicle Applications
- Support LIN Data Rates up to 20 Kbps
- Support Wide V_{BAT} Input Voltage Range: 4.5 V to 40 V
- Low-current Standby Mode and Sleep Mode with Bus and Local Wake-up Capability
- Input Levels Compatible with 3.3-V and 5-V MCU Interface
- ±2% Accuracy 5-V or 3.3-V Voltage Regulator with up to 125-mA (DFN, ESOP) Capability
- Ideal Passive Behavior to LIN Bus when Unpowered
- Integrated Pull-up Resistor for LIN Slave Applications
- Protection Feature：
  - IEC 61000-4-2 ESD Protection up to ±15 kV
  - Bus Fault Protection: ±45 V
  - V_{BAT} and V_{CC} Undervoltage Protection
  - Voltage Regulator Short to Ground Protection
  - TXD Dominant Time-out Function
  - Thermal Shutdown Protection
- Available in SOP8 Package, ESOP8 Package, and Leadless DFN3X3-8 Package with Improved Automated Optical Inspection (AOI) Capability
- AEC-Q100 Qualified for Automotive Applications, Grade 1

Applications

- Automotive and Transportation
- Body Electronics / Lighting
- Power Train / Chassis
- Infotainment / Cluster
- ADAS / Safety

Description

The TPT1028xQ is a local interconnect network (LIN) system basis chip (SBC), which includes a LIN transceiver, compliant to the ISO 17987-4, SAE J2602 and LIN 2.0, LIN 2.1, LIN 2.2, and LIN 2.2-A physical layer standard, and an integrated low drop out (LDO) voltage regulator. LIN is a low-speed Universal Asynchronous Receiver Transmitter (UART) communication protocol that supports automotive in-vehicle sub-networks.

The LIN SBC is designed in LIN networks up to 20 Kbps and reduces system complexity by providing a 5-V or 3.3-V LDO to power microprocessors, sensors, and other devices. The device supports Sleep mode, in which the LDO and LIN transceivers are shut down while still able to be woken up via the LIN bus. The device integrates a pull high resistor for LIN slave applications and ESD protection, which allows applications to operate with a reduced dependence on external components. With an optimized circuit design, the TPT1028xQ exhibits very low electromagnetic emission (EME) and high electromagnetic immunity (EMI) capabilities.

As designed, the device features overvoltage and loss of ground protection from −45 V to +45 V, over-temperature shutdown, under voltage and short to ground protections, and other protection features to enhance the device and network robustness.

The TPT1028xQ is available in SOP-8, ESOP-8, and DFN3X3-8 packages and is AEC-Q100 qualified for automotive applications.

Typical Application Circuit

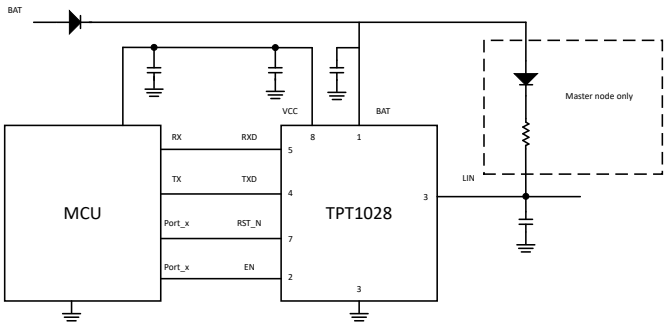


Table of Contents

Product Family Table

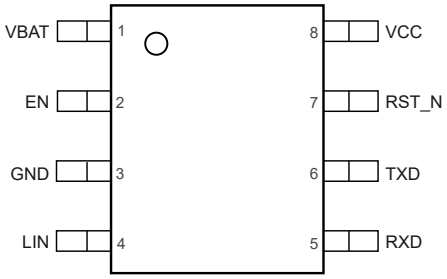
Order Number	VCC (V)	ICC (mA)	Bus Fault Protection (V)	Package
TPT10283Q-DFCR-S	3.3	125	45	DFN3X3-8
TPT10283Q-SO1R-S	3.3	100	45	SOP-8
TPT10283Q-ES1R-S	3.3	125	45	ESOP-8
TPT10285Q-DFCR-S	5	125	45	DFN3X3-8
TPT10285Q-SO1R-S	5	100	45	SOP-8
TPT10285Q-ES1R-S	5	125	45	ESOP-8

Revision History

Date	Revision	Notes
2022-12-05	Rev.P.0	Initial version
2024-11-30	Rev.A.0	Released version

Pin Configuration and Functions

TPT1028xQ
SOP8/ESOP8 Package
Top View



TPT1028xQ
DFN3X3-8 Package
Top View

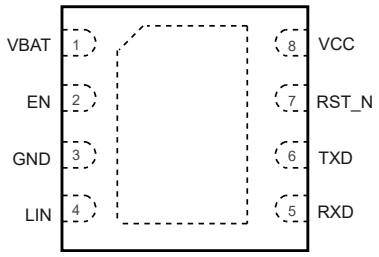


Table 1. Pin Functions: TPT1028xQ

Pin		I/O	Description
No.	Name		
1	VBAT	HV Power Input	High voltage power supply from the battery
2	EN	Input	Enable input
3	GND	GND	Ground
4	LIN	HV I/O	LIN bus input/output line
5	RXD	Output	LIN receive data output
6	TXD	Input	LIN transmit data input
7	RST_N	Output	Reset output (active low)
8	VCC	Power Output	Integrated voltage regulator output

Specifications

Absolute Maximum Ratings (1)

Parameter		Conditions	Min	Max	Unit
V_{BAT}	Battery Supply Voltage Range		−0.3	45	V
V_{CC}	Pin VCC Voltage Range		−0.3	7	V
V_{TXD}	Pin TXD Voltage Range		−0.3	V_{CC} + 0.3	V
V_{RXD}	Pin RXD Voltage Range		−0.3	V_{CC} + 0.3	V
V_{RST_N}	Pin RST_N Voltage Range		−0.3	V_{CC} + 0.3	V
V_{EN}	Pin EN Voltage Range	I_{EN} < 500 μA	−0.3	V_{CC} + 0.3	V
V_{LIN}	Pin LIN Voltage Range	With respect to GND, V_{BAT}, and V_{EN}	−45	45	V
T_J	Junction Temperature (2)		−55	150	°C
T_{STG}	Storage Temperature		−55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC standard multilayer test boards.

ESD (Electrostatic Discharge Protection)

Parameter		Condition	Mini	Typ	Max	Unit
V_{ESD}	Electrostatics Discharge (1)(2)	IEC61000-4-2(150 pF, 330 Ω discharge circuit), contact discharge on LIN bus pins	−15	-	15	kV
		Human Body Model (HBM) on LIN bus pins	−15	-	15	kV
		Human Body Model (HBM) on any other pins	−6	-	6	kV
		Charged Device Model (CDM) on all pins	−750	-	750	V
V_{TRAN}	Transient Immunity ISO 7637-2 on Bus Pins	Pulse1	−100	-	-	V
		Pulse2a	-	-	75	V
		Pulse3a	−150	-	-	V
		Pulse3b	-	-	100	V

Recommended Operating Conditions

	Parameter	Min	Max	Unit
V_{BAT}	Battery Power Supply	5.5	40	V
V_{LIN}	LIN Bus Input Voltage	0	40	V
V_{LOGIC}	Logic Pin Voltage	0	5.25	V
T_J	Operating Virtual Junction Temperature Range	−40	150	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8	114.82	47.81	°C/W
DFN3x3-8	40.41	53.02	°C/W
ESOP8	32.88	45.13	°C/W

Electrical Characteristics

All test conditions: V_{BAT} = 5.5 V to 40 V, R_L = 500 Ω, T_A = −40°C to 125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Pin VBAT						
V_{BAT}	Supply Voltage		5.5		40	V
$V_{TH\_DET\_PON}$	Power-on Detection Threshold		3.4	3.9	4.4	V
$V_{TH\_DET\_POFF}$	Power-off Detection Threshold		3	3.5	4	V
$V_{HYS\_DET\_PON}$	Hysteresis Voltage on Power-on Detection (1)		50	300		mV
I_{BAT}	Standby Mode Supply Current	$V_{LIN} = V_{BAT}$		25	75	μA
	Sleep Mode Supply Current	$V_{LIN} = V_{BAT}$ = 12 V		7.8	23	μA
		$V_{LIN} = V_{BAT}$		12	50	μA
	Normal Mode Supply Current	Recessive; $V_{LIN} = V_{BAT}$; $V_{RXD} = V_{CC}$; V_{RST_N} = High		167	300	μA
		Dominant; $V_{LIN} = V_{BAT}$; V_{RXD} = 0 V; V_{RST_N} = High		1.6	6.5	mA
Pin VCC						
V_{CC}	Supply Voltage	14 V > V_{BAT} > 6 V; V_{CC} = 5 V; I_{CC} = −125 mA to 0 mA (DFN and ESOP); I_{CC} = −100 mA to 0 mA (SOP)	4.9	5	5.1	V
V_{CC}	Supply Voltage	14 V > V_{BAT} > 4.5 V; V_{CC} = 3.3 V; I_{CC}= −125 mA to 0 mA (DFN and ESOP); I_{CC} = −100 mA to 0 mA (SOP)	3.234	3.3	3.366	V
ΔV_{CC_LINE}	Line Regulation	I_{CC} = 10 mA			50	mV
ΔV_{CC_LOAD}	Load Regulation	I_{CC} = 1 to 100 mA; V_{BAT} = 14 V			40	mV
V_{DROP}	Dropout Voltage	$V_{DROP} = V_{BAT} - V_{CC}$; I_{CC} = 100 mA; V_{CC} = 5 V version		300	600	mV
I_{O_LIMIT}	Output Current Limit	V_{CC} short to ground			310	mA
V_{UVD}	Undervoltage Detection Voltage	V_{CC} = 5 V	3.6	4.55	4.6	V
V_{UVD}	Undervoltage Detection Voltage (1)	V_{CC} = 3.3 V	2.7	2.9	3.0	V
V_{UVR}	Undervoltage Recovery Voltage	V_{CC} = 5 V	4.0	4.25	4.9	V
V_{UVR}	Undervoltage Recovery Voltage (1)	V_{CC} = 3.3 V	2.9	2.75	3.1	V
$R_{VBAT-VCC}$	Resistance between Pin V_{BAT} and V_{CC} (1)	V_{CC} = 5 V, V_{BAT} = 4.5 V to 5.5 V; I_{CC} = 5 mA to 70 mA, Tj = 85℃			4	Ω

Parameter		Conditions	Min	Typ	Max	Unit
$R_{VBAT-VCC}$	Resistance between Pin V_{BAT} and V_{CC} (1)	V_{CC} = 5 V, V_{BAT} = 4.5V to 5.5V; I_{CC} = 5 mA to 70 mA, Tj = 150℃			5	Ω
C_O	Output Capacitance (1)	Equivalent series resistance < 2 Ω	1	10	-	μF
PSRR	Power Supply Rejection Ratio (1)	V_{AC} = 0.5 V_{P-P}, I_{CC} = 10 mA， f = 100 Hz，C_{OUT} = 10 μF	-	85		dB
Pin TXD						
V_{IH}	High-level Input Voltage	2.97 V < V_{CC} < 5.5 V	0.7 x V_{CC}			V
V_{IL}	Low-level Input Voltage	2.97 V < V_{CC} < 5.5 V			0.3 x V_{CC}	V
V_{HYS_TXD}	Hysteresis Voltage on Pin TXD		200			mV
R_{PU_TXD}	Pin TXD Pull-up Resistance		250	350	500	kΩ
Pin RXD						
I_{OH}	High-level Output Current	Normal mode; V_{LIN} = V_{BAT}, V_{RXD} = V_{CC} − 0.4 V			-0.4	mA
I_{OL}	Low-level Output Current	Normal mode; V_{LIN} = 0 V, V_{RXD} = 0.4 V	0.4			mA
Pin EN						
V_{IH}	High-level Input Voltage		2			V
V_{IL}	Low-level Input Voltage				0.8	V
R_{PD}	Pull-down Resistance		250	350	500	kΩ
Pin RST_N						
R_{PU}	Pull-up Resistance	V_{RST_N} = V_{CC} − 0.4 V; V_{CC} = 2.97 V to 5.5 V	3	5.5	12	kΩ
I_{OL}	Low-level Output Current	V_{RST_N} = 0.4 V; V_{CC} = 2.97 V to 5.5 V;	2.5			mA
V_{OL}	Low-level Output Voltage	V_{RST_N} = 0.4 V; V_{CC} = 2.97 V to 5.5 V;			0.8	V
V_{OH}	High-level Output Voltage		0.8 x V_{CC}		V_{CC} + 0.3	V
Pin LIN						
I_{BUS_LIM}	Dominant Output Current Limiation	V_{BAT} = V_{LIN} = 18 V; V_{TXD} = 0 V	40	135	200	mA
R_{PU}	Pull-up Resistance	Sleep mode; V_{SLP_N} = 0 V	50	150	250	kΩ
I_{BUS_REC}	Receiver Recessive Input Leakage Current	V_{BAT} = 5.5 V; V_{LIN} = 18 V; V_{TXD} = 5 V			20	μA
I_{BUS_DOM}	Receiver Dominant Input Leakage Current	Normal mode; V_{BAT} = 12 V; V_{LIN} = 0 V; V_{TXD} = 5 V	−500			μA

Parameter		Conditions	Min	Typ	Max	Unit
$V_{SerDiode}$	Voltage Drop at the Serial Diode (1)	Pull-up path with R_{SLAVE}; $I_{SerDiode}$ = 10 μA	0.4		1	V
$I_{BUS\_NO\_GND}$	Ground Loss Bus Current	V_{BAT} = 40 V; V_{LIN} = 0 V	−850		10	μA
$I_{BUS\_NO\_BAT}$	Battery Loss Bus Current	V_{BAT} = 0 V; V_{LIN} = 40 V			20	μA
$V_{BUS\_PAS\_DOM}$	Receiver Dominant				0.4 x V_{BAT}	V
$V_{BUS\_PAS\_REC}$	Receiver Recessive		0.6 x V_{BAT}			V
V_{BUS_CNT}	Receiver Center Voltage		0.475 x V_{BAT}	0.5 x V_{BAT}	0.525 x V_{BAT}	V
V_{HYS}	Receiver Hysteresis Voltage		0.05 x V_{BAT}	0.15 x V_{BAT}	0.175 x V_{BAT}	V
R_{SLAVE}	Slave Resistance	Between LIN and V_{BAT}; V_{BAT} = 12 V; V_{LIN} = 0 V	20	30	60	kΩ
C_{LIN}	Pin LIN Capacitance (1)				30	pF
V_{O_DOM}	Dominant Output Voltage	Normal mode; V_{TXD} = 0 V			0.2 x V_{BAT}	V
V_{O_REC}	Recessive Output Voltage	Normal mode; V_{TXD} = V_{CC}	0.85 x V_{BAT}			V
Thermal shutdown						
T_{J_SD}	Shutdown Junction Temperature (1)		165	175	185	℃
$T_{J\_SD\_HYS}$	Thermal Shutdown Hysteresis (1)			20		℃

(1) The data is based on bench tests and design simulation.

Duty Cycles

All test conditions: V_{BAT}= 5.5 V to 40 V, R_L= 500 Ω, T_A= −40°C to 125°C, see Figure 2, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
D1	Duty cycle 1; D1 = $t_{BUS\_REC\_MIN}$/ 2 x t_{BIT}	$V_{TH\_REC\_MAX}$ = 0.744 x V_{BAT}; $V_{TH\_DOM\_MAX}$ = 0.581 x V_{BAT}; 20 kbps; t_{BIT} = 50 µs; 7 V ≤ V_{BAT} ≤ 40 V	0.396			
D1	Duty cycle 1; D1 = $t_{BUS\_REC\_MIN}$/ 2 x t_{BIT}	$V_{TH\_REC\_MAX}$ = 0.744 x V_{BAT}; $V_{TH\_DOM\_MAX}$ = 0.581 x V_{BAT}; 20 kbps; t_{BIT} = 50 µs; 5.5 V ≤ V_{BAT} < 7 V	0.396			
D2	Duty cycle 2; D2 = $t_{BUS\_REC\_MAX}$/ 2 x t_{BIT}	$V_{TH\_REC\_MIN}$ = 0.422 x V_{BAT}; $V_{TH\_DOM\_MIN}$ = 0.284 x V_{BAT}; 20 kbps; t_{BIT} = 50 µs; 7.6 V ≤ V_{BAT} ≤ 40 V			0.581	
D2	Duty cycle 2; D2 = $t_{BUS\_REC\_MAX}$/ 2 x t_{BIT}	$V_{TH\_REC\_MIN}$ = 0.464 x V_{BAT}; $V_{TH\_DOM\_MIN}$ = 0.312 x V_{BAT}; 20 kbps; t_{BIT} = 50 µs; 5.5 V ≤ V_{BAT} < 7.6 V			0.581	
D3	Duty cycle 3; D3 = $t_{BUS\_REC\_MIN}$/ 2 x t_{BIT}	$V_{TH\_REC\_MAX}$ = 0.778 x V_{BAT}; $V_{TH\_DOM\_MAX}$ = 0.616 x V_{BAT}; 10.4 kbps; t_{BIT} = 96 µs; 7 V ≤ V_{BAT} ≤ 40 V	0.417			
D3	Duty cycle 3; D3 = $t_{BUS\_REC\_MIN}$/ 2 x t_{BIT}	$V_{TH\_REC\_MAX}$ = 0.778 x V_{BAT}; $V_{TH\_DOM\_MAX}$ = 0.616 x V_{BAT}; 10.4 kbps; t_{BIT} = 96 µs; 5.5 V ≤ V_{BAT} < 7 V	0.417			
D4	Duty cycle 4; D4 = $t_{BUS\_REC\_MAX}$/ 2 x t_{BIT}	$V_{TH\_REC\_MIN}$ = 0.389 x V_{BAT}; $V_{TH\_DOM\_MIN}$ = 0.251 x V_{BAT}; 10.4 kbps; t_{BIT} = 96 µs; 7.6 V ≤ V_{BAT} ≤ 40 V			0.590	
D4	Duty cycle 4; D4 = $t_{BUS\_REC\_MAX}$/ 2 x t_{BIT}	$V_{TH\_REC\_MIN}$ = 0.389 x V_{BAT}; $V_{TH\_DOM\_MIN}$ = 0.251 x V_{BAT}; 10.4 kbps; t_{BIT} = 96 µs; 5.5 V ≤ V_{BAT} < 7.6 V			0.590	

AC Timing Requirements

All test conditions: V_{BAT} = 5.5 V to 40 V, R_L = 500 Ω, T_A = −40°C to 125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
t_{RX_PD}	Receiver propagation delay	Rising and falling			6	µs
t_{RX_SYM}	Receiver propagation delay symmetry		−2		2	µs
$t_{WAKE\_DOM\_LIN}$	LIN dominant wake-up time	Sleep mode	30	80	150	µs
$t_{TO\_DOM\_TXD}$	TXD dominant time-out time	V_{TXD} = 0 V	6	12	20	ms
t_{MODE}	Mode select time (1)		3		16	µs
t_{EN-TXD}	Delay time from EN to TXD (1)		0		1	µs
t_{DET_UVVCC}	Undervoltage detection time on VCC pin (1)		1	7.4	15	µs
t_{RST}	Reset time		2	4.3	8	ms

(1) The test data is based on bench test and design simulation.

Parameter Measurement Information

Test Circuit

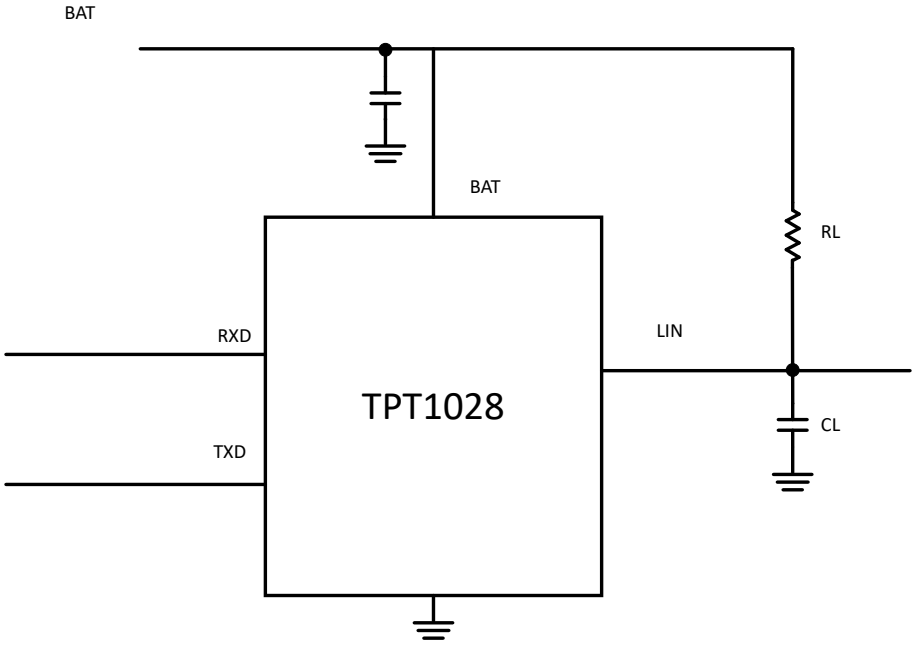


Figure 1. LIN Transceiver Timing Parameter Test Circuit

Parameter Diagram

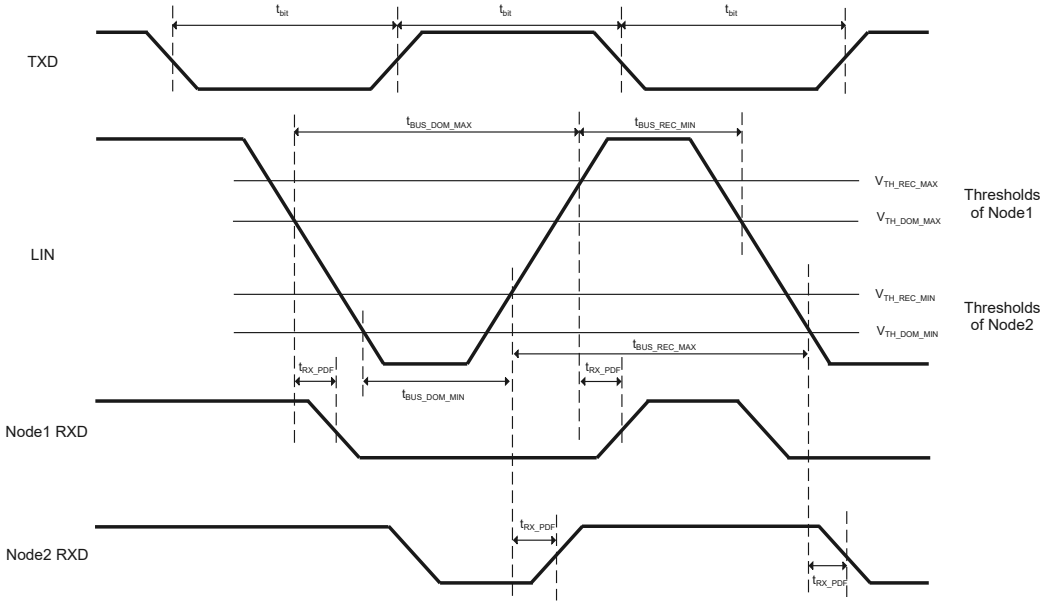


Figure 2. LIN Transceiver Timing Diagram

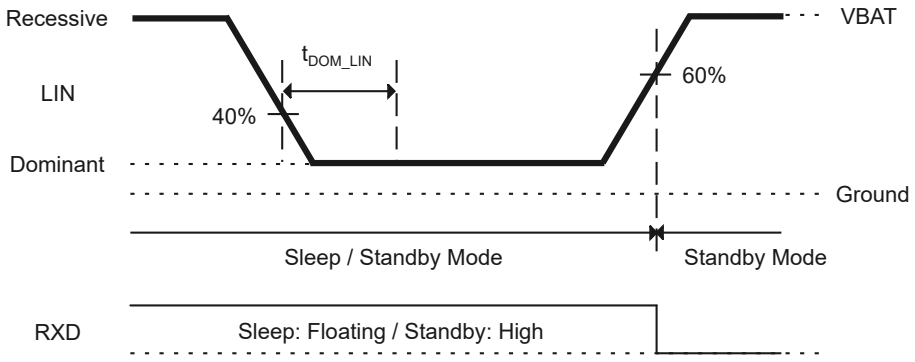


Figure 3. Remote Wake-up Diagram

Detailed Description

Overview

The TPT1028xQ is a local interconnect network (LIN) system basis chip (SBC), which includes a LIN transceiver, compliant to the ISO 17987-4, SAE J2602 and LIN 2.0, LIN 2.1, LIN 2.2, and LIN 2.2-A physical layer standard, and an integrated low drop out (LDO) voltage regulator. LIN is a low-speed Universal Asynchronous Receiver Transmitter (UART) communication protocol that supports automotive in-vehicle sub-networks. The LIN SBC is designed in LIN networks up to 20 Kbps and reduces system complexity by providing a 5-V or 3.3-V LDO to power the microprocessors, sensors, and other devices. The device supports Sleep mode, in which the LDO and LIN transceivers are shut down while still able to be waken-up via the LIN bus. The device integrates a pull high resistor for LIN slave applications and ESD protection which allows applications to operate with a reduced dependence on external components. With an optimized circuit design, the TPT1028xQ exhibits very low electromagnetic emission (EME) and high electromagnetic immunity (EMI) capabilities. As designed, the device features overvoltage and loss of ground protection from −45 V to +45 V, over-temperature shutdown, under voltage and short to ground protection, and other protection features to enhance the device and network robustness. The TPT1028xQ is available in SOP-8, ESOP-8, and DFN3X3-8 packages and is AEC-Q100 qualified for automotive applications.

Functional Block Diagram

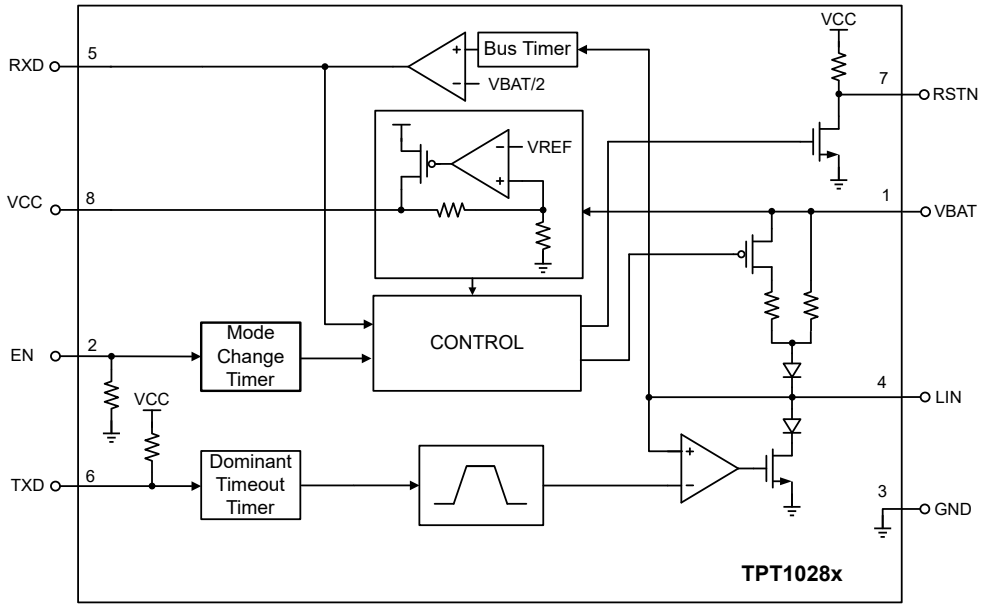


Figure 4. Functional Block Diagram

Feature Description

Device Operating Modes

The TPT1028xQ supports modes for Normal mode, Power-on mode, Standby mode, and Sleep mode. The figure below shows the state diagram.

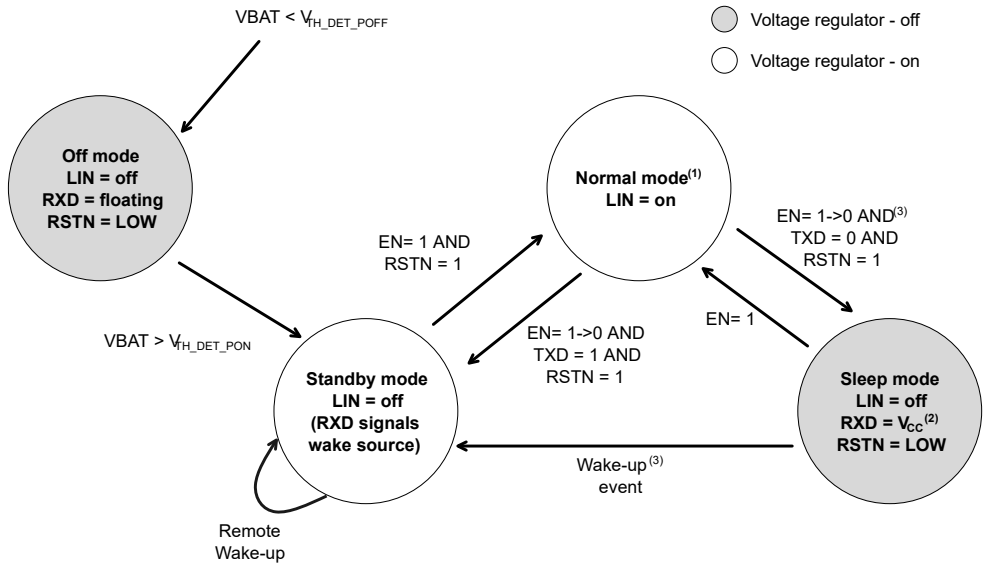


Figure 5. Functional Block Diagram

1. The LIN transmitter is enabled in Normal mode when EN and RST_N are high. If EN and/or RST_N go low, the LIN transmitter is disabled. The device can be remotely woken-up via the LIN bus.
2. Until V_{CC} drops below 2 V.
3. The device switches to Standby mode without initiating a reset if a wake-up event and a go-to-sleep event occur simultaneously.

Table 2. Function Table

Mode	EN	RXD	RST_N	Transmitter	LIN BUS Termination
Normal	High	High: recessive state Low: dominant state	V_{CC}	Normal	30 kΩ
Sleep	Low	Floating	GND	Off	Weak current pull-up
Standby	Low	Low (Remote wake-up)	V_{CC}	Off	30 kΩ
		High			
Off	/	Floating	GND	Off	Weak current pull-up

Off Mode

The device switches to Off mode if the battery supply voltage drops below the under-voltage protection threshold or the junction temperature exceeds the overtemperature protection activation threshold.

The LDO and LIN transceiver are disabled in Off mode, the RST_N pin keeps low.

Normal Mode

The device switches to Normal mode from Standby mode or Sleep mode if the EN pin is pulled high.

In Normal mode, the LDO is enabled, and the LIN transceiver can transmit and receive data through the LIN bus line. The receiver detects the data stream at the LIN bus input pin and transfers it to the microcontroller via the RXD pin. On the bus,

a HIGH level corresponds to a recessive state, while a LOW level represents a dominant state. The receiver incorporates a voltage-dependent threshold with hysteresis and an integrated filter to suppress noise on the bus.

The transmit data stream from the protocol controller at the TXD input is converted by the transmitter into a bus signal with an optimized slew rate and wave shaping, aiming to minimize electromagnetic emissions (EME). The LIN bus output pin is pulled HIGH through an internal slave termination resistor. For master applications, an external resistor in series with a diode should be connected between pin VBAT and pin LIN.

Standby Mode

Standby mode is a low-power mode for power- saving applications. The device switches to Standby mode from Off mode if the battery supply voltage rises above the power-on detection threshold.

The device switches to Standby mode from Normal mode if pin TXD is high and pin EN is low during the mode select window.

Standby mode is automatically activated whenever wake-up occurs while the device is in Sleep mode. The remote wake-up event is indicated by a low level on the RXD pin, which can serve as an interrupt for the microcontroller.

The LDO is enabled in Standby mode, and the LIN transceiver is disabled and is capable of being remote wake-up. The wake-up source is indicated by the level on RXD.

Sleep Mode

The Sleep mode offers an extremely low power mode that guarantees extremely low current consumption.

The device switches to Sleep mode from Normal mode if pin TXD and pin EN are both low during the mode select window. The LDO are LIN transceiver are disabled in Sleep mode and pin RST_N is forced low. The device is capable of being remote wake-up via the LIN bus. Input filters are incorporated at the receiver to prevent undesired wake-up events caused by automotive transients or electromagnetic interference (EMI).

Wake-up

A remote wake-up event triggers a transition to Standby mode from Sleep mode.

Remote wake-up through the LIN bus by transmitting a dominant bus state that is sustained for a duration of at least $t_{WAKE\_DOM\_LIN}$, then followed by a rising edge.

Power Supply

Battery Supply Input

The battery supply, V_{BAT} pin, operating range is from 5.5 V to 40 V, the maximum voltage device can handle is 45 V. If the V_{BAT} input voltage drops below $V_{TH\_DET\_POFF}$, the device switches to Off mode, the LDO and LIN transceiver is disabled. The device exits Off mode as soon as the battery supply voltage rises above the $V_{TH\_DET\_PON}$. An external diode is needed in series to protect the device against negative voltage.

Voltage Regulator Output

The device integrated a low-dropout voltage regulator supplied via V_{BAT} pin, the V_{CC} output current up to 100 mA. There are two output voltage versions for different power supply voltage microcontroller: the TPT10285 output voltage is 5 V, and the TPT10283 output voltage is 3.3 V.

Reset

The VCC voltage is monitored continuously; if VCC drops below V_{UVD} for $t_{DET\_UV\_VCC}$, an undervoltage event is detected, and the RST_N pin sets low. When VCC exceeds the undervoltage recovery threshold V_{UVR} for T_{RST}, the RST_N pin goes back to high again.

Protection Features

TXD Dominant Time-out

The device detects TXD dominant time-out and prevents a permanent low on the TXD pin driving the LIN bus into permanent dominant blocking the LIN bus network. If the TXD remains low for longer than t_{TXD_DTO} , the transmitter is disabled until the fault flag has been cleared.

Under-voltage Lockout (UVLO)

The device integrates under-voltage detection and lockout circuit of the supply terminal to keep the device in protected mode if the supply voltage drops below the threshold until the supply voltage is higher than the UVLO threshold. This protects the device and system during undervoltage events on supply terminals.

Over-Temperature Protection (OTP)

The device is protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{J_SD}, the device switches to Off mode. The voltage regulator and the LIN transmitter is switched off, and the pin RST_N is driven low. When the virtual junction temperature falls below $T_{J\_SD\_R}$, the device switches to normal mode.

Fail-safe Features

An internal pull-down to GND on the TXD pin to establish a predetermined level in case the TXD pin is disconnected.

RXD pin is set floating when the VBAT pin is unpowered.

The LIN transmitter is disabled when either EN or RST_N is low

LIN transmitter is only enabled if a recessive level is present on pin TXD after switching to Normal mode.

The current limit is applied to the LIN transmitter output to protect the LIN bus short circuits to VBAT or GND.

VBAT and GND loss does not impact the LIN bus or the MCU. No reverse current flows from the bus into the LIN pin. The internal integrated LIN slave termination resistor keeps the current path from VBAT to LIN. Disconnecting the LIN transceiver from the power supply does not affect the LIN bus.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

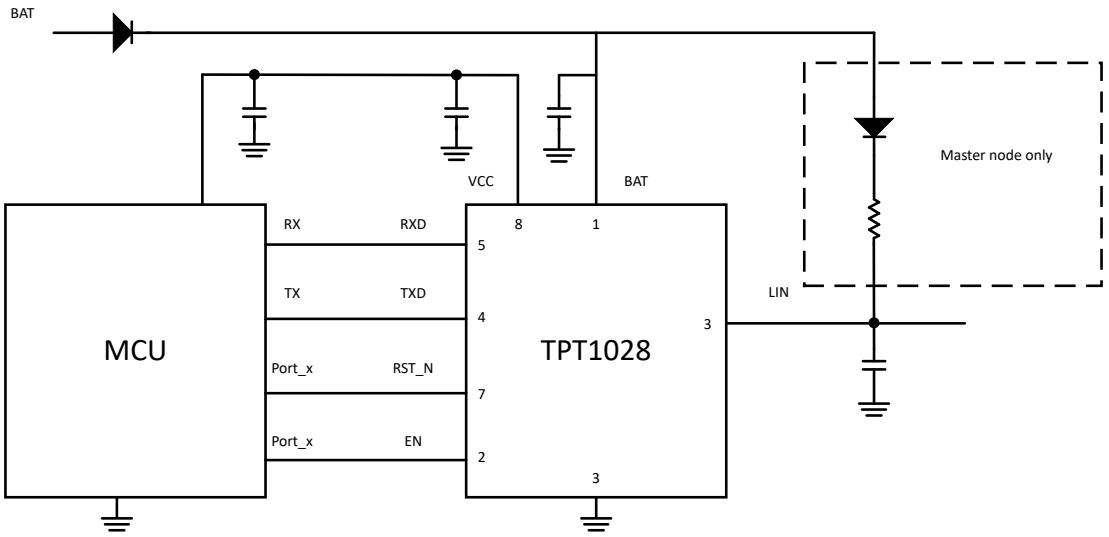
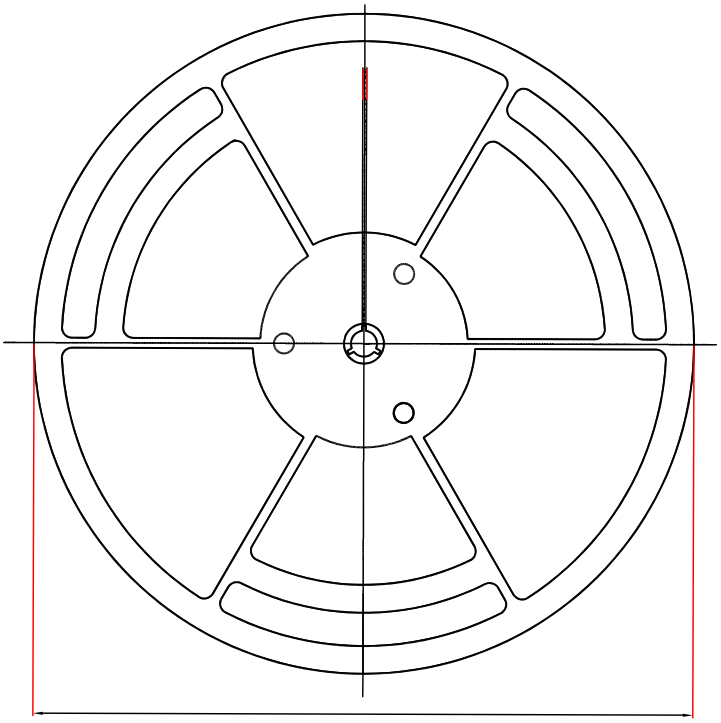
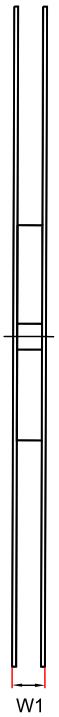
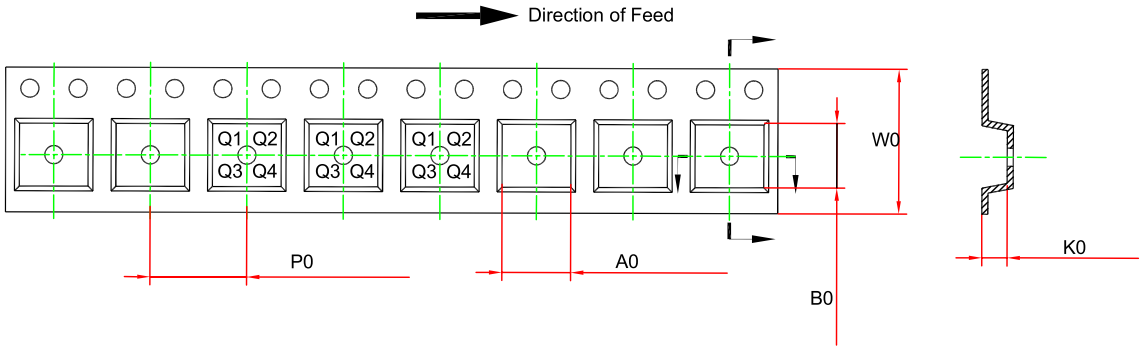


Figure 6. Typical Application Circuit

Tape and Reel Information





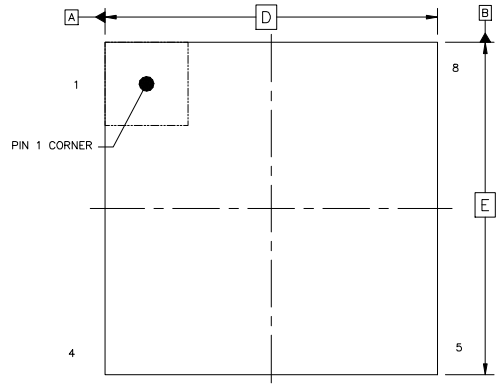


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT10283Q-DFCR-S	DFN3X3-8	330	17.6	3.3	3.3	1.1	8	12	Q1
TPT10283Q-SO1R-S	SOP-8	330	17.6	6.5	5.4	2	8	12	Q1
TPT10283Q-ES1R-S	ESOP-8	330	17.6	6.4	5.4	2.1	8	12	Q1
TPT10285Q-DFCR-S	DFN3X3-8	330	17.6	3.3	3.3	1.1	8	12	Q1
TPT10285Q-SO1R-S	SOP-8	330	17.6	6.5	5.4	2	8	12	Q1
TPT10285Q-ES1R-S	ESOP-8	330	17.6	6.4	5.4	2.1	8	12	Q1

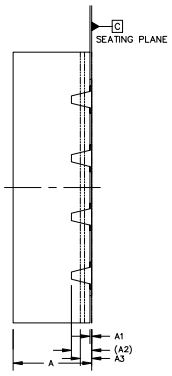
Package Outline Dimensions

DFN3X3-8

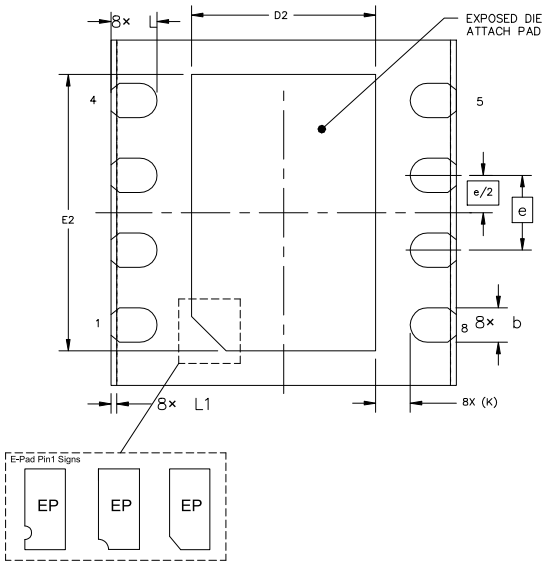
Package Outline Dimensions DFC(DFN3X3-8-WET-H)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

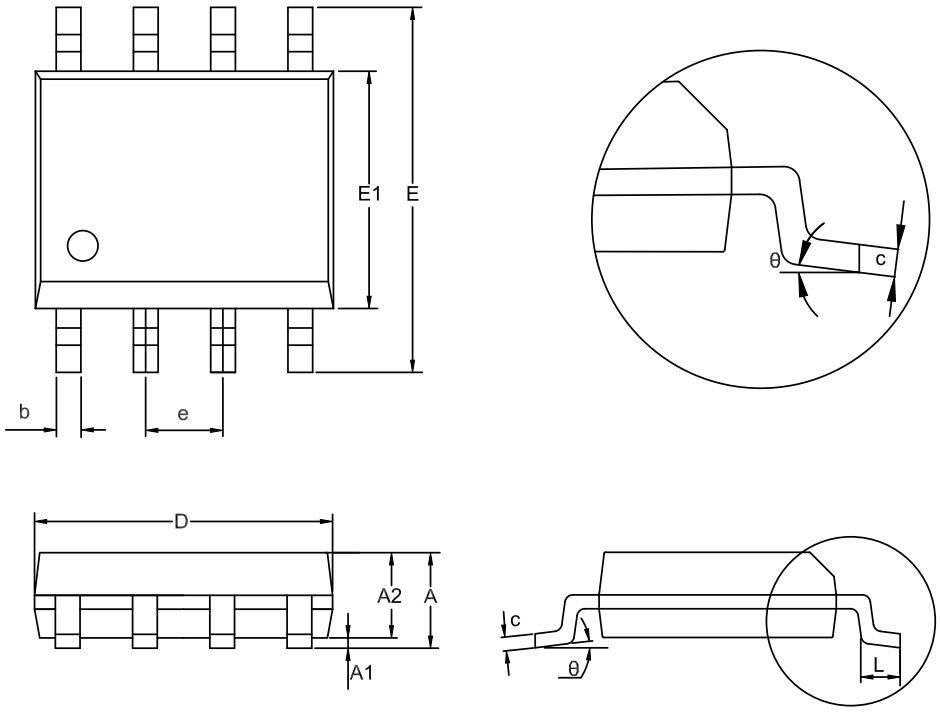
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
A2	0.150	0.250	0.006	0.010
A3	0.080	0.180	0.003	0.007
D	2.900	3.100	0.114	0.122
D2	1.500	1.700	0.059	0.067
E	2.900	3.100	0.114	0.122
b	0.250	0.350	0.010	0.014
E2	2.300	2.500	0.091	0.098
e	0.650 BSC		0.026 BSC	
L	0.350	0.450	0.014	0.018
L1	0.010	0.090	0.0004	0.004
K	0.300 REF		0.012 REF	

SOP8

Package Outline Dimensions SO1(SOP-8-A)



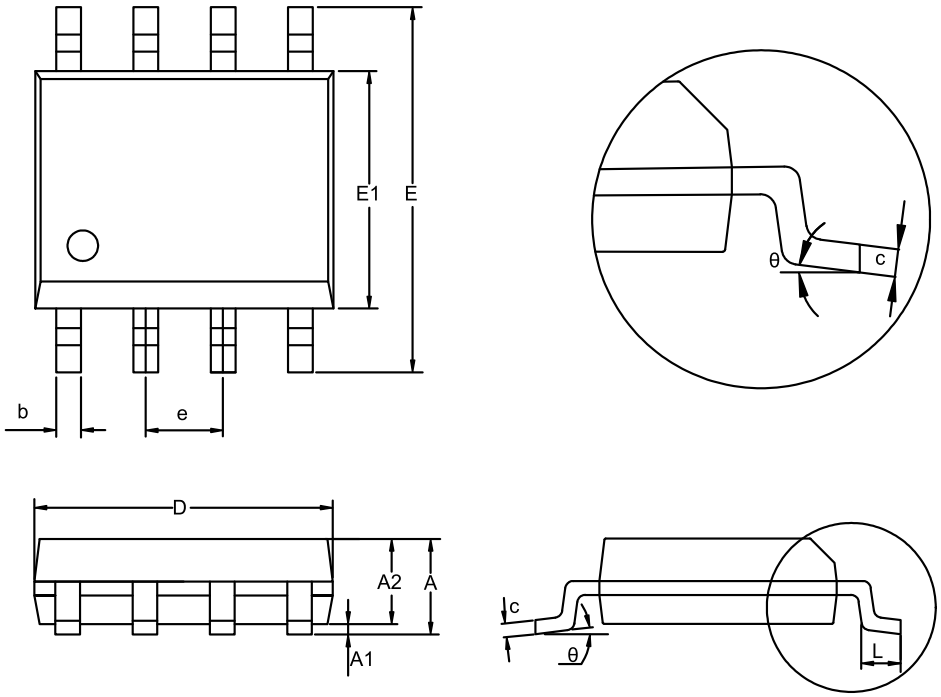
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

ESOP8

Package Outline Dimensions ES1(ESOP-8-F)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	2.850	3.250	0.112	0.128
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
E2	1.950	2.360	0.077	0.093
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT10283Q-DFCR-S	−40 to 125°C	DFN3X3-8	T283Q	MSL1	Tape and Reel,4000	Green
TPT10283Q-SO1R-S	−40 to 125°C	SOP-8	T283Q	MSL1	Tape and Reel,4000	Green
TPT10283Q-ES1R-S	−40 to 125°C	ESOP-8	T283Q	MSL1	Tape and Reel,4000	Green
TPT10285Q-DFCR-S	−40 to 125°C	DFN3X3-8	T285Q	MSL1	Tape and Reel,4000	Green
TPT10285Q-SO1R-S	−40 to 125°C	SOP-8	T285Q	MSL1	Tape and Reel,4000	Green
TPT10285Q-ES1R-S	−40 to 125°C	ESOP-8	T285Q	MSL1	Tape and Reel,4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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