Automotive Fault Protected Dual LIN Transceiver with TXD Dominant Timeout

Features

- Compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO 17987-4 Electrical Physical Layer (EPL) Specification
- Compliant to SAE J2602 LIN Network for Vehicle Applications
- Support LIN Data Rates up to 20 Kbps
- Wide V_{BAT} Input Voltage Range Supports 5.5 V to 40 V
- Low-current Standby Mode and Sleep Mode with Bus Wake-up Capability
- Input Levels Compatible with 3.3 V and 5 V MCU Interface
- Ideal Passive Behavior to LIN Bus when Unpowered
- Integrated Pull-up Resistor for LIN Slave Applications
- Protection Feature：
  - Bus Pin IEC 61000-4-2 ESD Protection ±10 kV
  - Bus Fault-Tolerant: ±45 V
  - V_{BAT} Undervoltage Protection
  - TXD Dominant Time-out Function
  - Thermal Shutdown Protection
- Available in the SOP14 Package and Leadless DFN3X4.5-14L Package with Improved Automated Optical Inspection (AOI) Capability
- AEC-Q100 Qualified for Automotive Applications, Grade 1

Applications

- Automotive and Transportation
- Body Electronics / Lighting
- Power Train / Chassis
- Infotainment / Cluster
- ADAS / Safety

Description

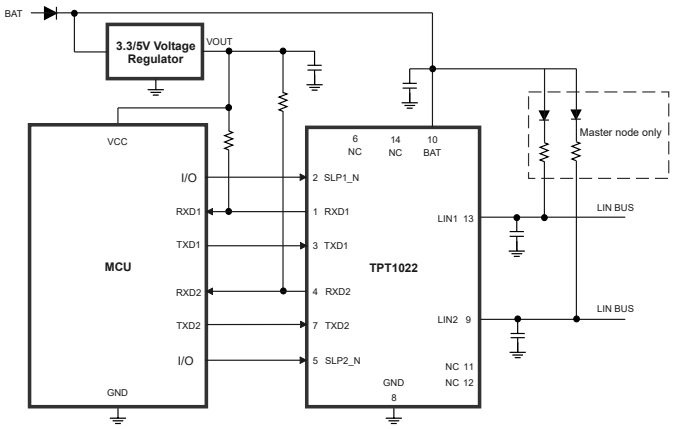
The TPT1022Q is a dual local interconnect network (LIN) physical layer transceiver that is compliant with the ISO 17987-4, SAE J2602 and LIN 2.0, LIN 2.1, LIN 2.2, and LIN 2.2-A physical layer standard. LIN is a low-speed Universal Asynchronous Receiver Transmitter (UART) communication protocol that supports automotive in-vehicle sub-networks.

The device supports LIN networks up to 20 Kbps with an enhanced timing margin. The device converts the transmitted data received at the TXD with an optimized slew rate to minimize the electro-magnetic emission (EME) and reports the state of the LIN bus at the RXD.

As designed, the device features overvoltage and loss of ground protection from −45 V to +45 V, over-temperature shutdown. The device has low-current standby and sleep mode with LIN BUS wake-up capability. The device integrates a pull high resistor for LIN slave applications and ESD protection which allows applications to operate with a reduced dependence on external components. Additionally, all devices include many protection features to enhance the device and network robustness.

The TPT1022Q is available in SOP-14 and DFN3X4.5-14L packages and is AEC-Q100 qualified for automotive applications.

Typical Application Circuit



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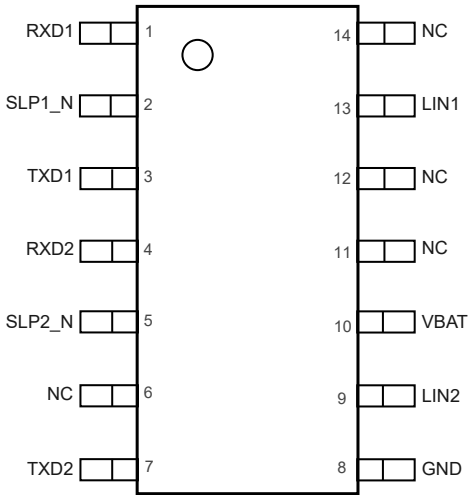
Revision History

Date	Revision	Notes
2022-12-05	Rev.Pre.0	Initial version
2024-2-25	Rev.A.0	Released version
2024-7-30	Rev.A.1	Typo correction

Pin Configuration and Functions

TPT1022Q
SOP14 Package
Top View



TPT1022Q
DFN4.5X3-14
Top View

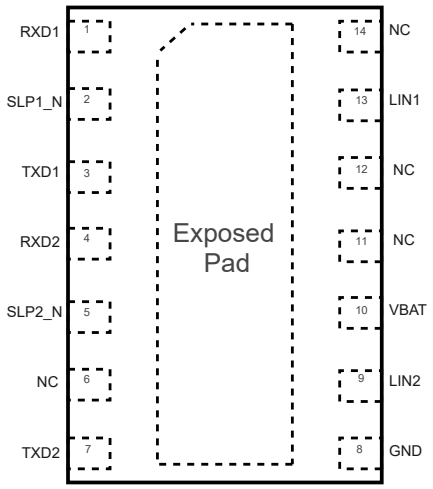


Table 1. Pin Functions: TPT1024Q

Pin		I/O	Description
No.	Name		
1	RXD1	Output	LIN1 receive data output
2	SLP1_N	Input	LIN1 sleep mode control input, active low
3	TXD1	Input	LIN1 transmit data input
4	RXD2	Output	LIN2 receive data output
5	SLP2_N	Input	LIN2 sleep mode control input, active low
6	NC	NC	Not connected
7	TXD2	Input	LIN2 transmit data input
8	GND	Ground	Ground
9	LIN2	Bus I/O	LIN2 bus input/output line
10	VBAT	Power	High voltage power supply from the battery
11	NC	NC	Not connected
12	NC	NC	Not connected
13	LIN1	Bus I/O	LIN1 bus input/output line
14	NC	NC	Not connected

Specifications

Absolute Maximum Ratings (1)

Parameter		Conditions	Min	Max	Unit
V_{BAT}	Battery Supply Voltage Range		−0.3	45	V
V_{TXD}	Pin TXD Voltage Range	Pin TXDx	−0.3	7	V
V_{RXD}	Pin RXD Voltage Range	Pin RXDx	−0.3	7	V
V_{SLP_N}	Pin SLP_N Voltage Range	Pin SLPx_N	−0.3	7	V
V_{LIN}	Pin LIN Voltage Range	Pin LINx, with respect to GND and V_{BAT}	−45	45	V
$\lvert\Delta V_{LIN1-LIN2}\rvert$	Voltage between Pin LIN1 and LIN2		-	45	V
T_J	Junction Temperature (2)		−55	150	°C
T_{STG}	Storage Temperature		−55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC standard multilayer test boards.

ESD (Electrostatic Discharge Protection)

Parameter		Condition	Min	Max	Unit
V_{ESD}	Electrostatics Discharge (1)(2)	IEC61000-4-2(150pF, 330Ω discharge circuit), contact discharge on LIN bus LINx pins	−10	10	kV
		Human Body Model (HBM) on LIN bus LINx pins	−10	10	kV
		Human Body Model (HBM) on any other pins	−6	6	kV
		Charged Device Model (CDM) on all pins	−1.5	1.5	kV
V_{TRAN}	Transient Immunity ISO 7637-2 on Bus Pins	Pulse1	−100	-	V
		Pulse2a	-	75	V
		Pulse3a	−150	-	V
		Pulse3b	-	100	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

	Parameter	Min	Max	Unit
V_{BAT}	Battery Power Supply	5.5	40	V
V_{LIN}	LIN Bus Input Voltage	0	40	V
V_{LOGIC}	Logic Pin Voltage	0	5.25	V
T_J	Operating Virtual Junction Temperature Range	−40	150	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP14	85.6	34.24	°C/W
DFN4.5x3-14	40.07	39.49	°C/W

Electrical Characteristics

All test conditions: V_{BAT} = 5.5 V to 40 V, R_L = 500 Ω, T_A = −40°C to 125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Pin VBAT						
$V_{TH\_DET\_POFF}$	Power-off Detection Threshold		1.6	3.1	4.0	V
$V_{TH\_DET\_PON}$	Power-on Detection Threshold		2.3	3.4	4.3	V
$V_{HYS\_DET\_PON}$	Hysteresis Voltage on Power-on Detection (1)		50	300	1000	mV
$V_{TH\_VBAT\_L}$	Low-level VBAT Low Threshold Voltage		3.3	4	4.7	V
$V_{TH\_VBAT\_H}$	High-level VBAT Low Threshold Voltage		3.55	4.2	4.9	V
$V_{HYS\_VBAT\_L}$	VBAT Low Hysteresis Voltage (1)		15	300	600	mV
I_{BAT}	Sleep Mode Supply Current	Recessive; V_{LINx} = V_{BAT}; V_{SLPx_N} = 0 V; both channels		7	12	μA
		Dominant; V_{LINx} = 0 V; V_{BAT} = 12 V; V_{SLPx_N} = 0 V; both channels		18	30	μA
	Standby Mode Supply Current	Recessive; V_{LINx} = V_{BAT}; V_{SLPx_N} = 0 V; both channels		7	20	μA
		Dominant; V_{LINx} = 0 V; V_{BAT} = 12 V; V_{SLPx_N} = 0 V; both channels		0.8	1	mA
	Normal Mode Supply Current	Recessive; V_{LINx} = V_{BAT}; V_{TXD} = 5 V; V_{SLP_N}= 5 V		0.3	0.6	mA
		Dominant; V_{BAT} = 12 V; V_{TXD} = 0 V; V_{SLP_N} = 5 V		4	10	mA
Pin TXDx						
V_{IH}	High-Level Input Voltage		2		7	V
V_{IL}	Low-Level Input Voltage		−0.3		0.8	V
V_{HYS_TXD}	Hysteresis Voltage on Pin TXD (1)		50	200	450	mV
R_{PD_TXD}	Pin TXD Pull-down Resistance	V_{TXD} = 5 V	50	125	325	kΩ
I_{IL}	Low-Level Input Current	V_{TXD} = 0 V	−5		5	μA
Pin SLP_Nx						
V_{IH}	High-level Input Voltage		2		7	V
V_{IL}	Low-level Input Voltage		−0.3		0.8	V
$V_{HYS\_SLP\_N}$	Hysteresis Voltage on Pin SLP_N (1)		50	200	450	mV
$R_{PD\_SLP\_N}$	Pin SLP_N Pull-down Resistance	V_{TXD} = 5 V	125	250	650	kΩ

Parameter		Conditions	Min	Typ	Max	Unit
I_{IL}	Low-level Input Current	V_{TXD} = 0 V	−5		5	μA
Pin RXDx						
I_{OL}	Low-level Output Current	Normal mode; V_{LIN} = 0 V, V_{RXDx} = 0.4 V	2			mA
I_{LH}	High-level Leakage Current (1)	Normal mode; V_{LIN} = V_{BAT}, V_{RXD} = 5 V	−5	0	5	μA
Pin LIN						
I_{BUS_LIN}	Dominant Output Current Limitation	V_{BAT} = V_{LIN} = 18 V; V_{TXDx} = 0 V	40		200	mA
I_{PU_SLP}	Pull-up Current	Sleep mode; V_{SLP_N}= 0 V	−20		-2	μA
$I_{BUS\_PAS\_REC}$	Receiver Recessive Input Leakage Current	V_{BAT} = 5.5 V; V_{LIN} = 40 V; V_{TXD} = 5 V		0	20	μA
$I_{BUS\_PAS\_DOM}$	Receiver Dominant Input Leakage Current	Normal mode; V_{BAT} = 12 V; V_{LIN} = 0 V; V_{TXD} = 5 V	−600			μA
$V_{SerDiode}$	Voltage Drop at the Serial Diode (1)	Pull-up path with R_{SLAVE}; $I_{SerDiode}$ = 10 μA	0.4		1	V
$I_{BUS\_NO\_GND}$	Ground Loss Bus Current	V_{BAT} = 40 V; V_{LIN} = 0 V	−750		10	μA
$I_{BUS\_NO\_BAT}$	Battery Loss Bus Current	V_{BAT} = 0 V; V_{LIN} = 40 V			20	μA
$V_{BUS\_PAS\_DOM}$	Receiver Dominant				0.4 x V_{BAT}	V
$V_{BUS\_PAS\_REC}$	Receiver Recessive		0.6 x V_{BAT}			V
V_{BUS_CNT}	Receiver Center Voltage		0.475 x V_{BAT}	0.5 x V_{BAT}	0.525 x V_{BAT}	V
V_{HYS}	Receiver Hysteresis Voltage				0.175 x V_{BAT}	V
R_{SLAVE}	Slave Resistance	Between LIN and VBAT; V_{BAT} = 12 V; V_{LIN} = 0 V	20	30	60	kΩ
C_{LIN}	Pin LIN Capacitance (1)				20	pF
V_{O_DOM}	Dominant Output Voltage	Normal mode; V_{TXD} = 0 V			1.4	V
Temperature Detection						
T_{J_SD}	Shutdown Junction Temperature (1)		160	180	200	℃
$T_{J\_SD\_R}$	Recover Shutdown Junction Temperature (1)		130	145	160	℃

(1) The data is based on bench tests and design simulation.

Duty Cycles

All test conditions: V_{BAT}= 5.5 V to 40 V, R_L= 500 Ω, T_A= −40°C to 125°C, see Figure 2, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
D1	Duty cycle 1; D1= $t_{BUS\_REC\_MIN}$/ 2 x t_{BIT}	$V_{TH\_REC\_MAX}$= 0.744 x V_{BAT}; $V_{TH\_DOM\_MAX}$= 0.581 x V_{BAT}; 20 kbps; t_{BIT}= 50 µs; 7 V ≤ V_{BAT} ≤ 40 V	0.396			
D1	Duty cycle 1; D1= $t_{BUS\_REC\_MIN}$/ 2 x t_{BIT}	$V_{TH\_REC\_MAX}$= 0.744 x V_{BAT}; $V_{TH\_DOM\_MAX}$= 0.581 x V_{BAT}; 20 kbps; t_{BIT}= 50 µs; 5.5 V ≤ V_{BAT} < 7 V	0.396			
D2	Duty cycle 2; D2= $t_{BUS\_REC\_MAX}$/ 2 x t_{BIT}	$V_{TH\_REC\_MIN}$= 0.422 x V_{BAT}; $V_{TH\_DOM\_MIN}$= 0.284 x V_{BAT}; 20 kbps; t_{BIT}= 50 µs; 7.6 V ≤ V_{BAT} ≤ 40 V			0.581	
D2	Duty cycle 2; D2= $t_{BUS\_REC\_MAX}$/ 2 x t_{BIT}	$V_{TH\_REC\_MIN}$= 0.464 x V_{BAT}; $V_{TH\_DOM\_MIN}$= 0.312 x V_{BAT}; 20 kbps; t_{BIT}= 50 µs; 5.5 V ≤ V_{BAT} < 7.6 V			0.581	
D3	Duty cycle 3; D3= $t_{BUS\_REC\_MIN}$/ 2 x t_{BIT}	$V_{TH\_REC\_MAX}$= 0.778 x V_{BAT}; $V_{TH\_DOM\_MAX}$= 0.616 x V_{BAT}; 10.4 kbps; t_{BIT}= 96 µs; 7 V ≤ V_{BAT} ≤ 40 V	0.417			
D3	Duty cycle 3; D3= $t_{BUS\_REC\_MIN}$/ 2 x t_{BIT}	$V_{TH\_REC\_MAX}$= 0.778 x V_{BAT}; $V_{TH\_DOM\_MAX}$= 0.616 x V_{BAT}; 10.4 kbps; t_{BIT}= 96 µs; 5.5 V ≤ V_{BAT}< 7 V	0.417			
D4	Duty cycle 4; D4= $t_{BUS\_REC\_MAX}$/ 2 x t_{BIT}	$V_{TH\_REC\_MIN}$= 0.389 x V_{BAT}; $V_{TH\_DOM\_MIN}$= 0.251 x V_{BAT}; 10.4 kbps; t_{BIT}= 96 µs; 7.6 V ≤ V_{BAT} ≤ 40V			0.590	
D4	Duty cycle 4; D4= $t_{BUS\_REC\_MAX}$/ 2 x t_{BIT}	$V_{TH\_REC\_MIN}$= 0.389 x V_{BAT}; $V_{TH\_DOM\_MIN}$= 0.251 x V_{BAT}; 10.4 kbps; t_{BIT}= 96 µs; 5.5 V ≤ V_{BAT} < 7.6 V			0.590	

AC Timing Requirements

All test conditions: V_{BAT} = 5.5 V to 40 V, R_L = 500 Ω, T_A = −40°C to 125°C, unless otherwise noted. unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
t_{RX_PD}	Receiver Propagation Delay	Rising and falling			6	μs
t_{RX_SYM}	Receiver Propagation Delay Symmetry	Rising edge with respect to falling edge	−2		2	μs
$t_{WAKE\_DOM\_LIN}$	LIN Dominant Wake-up Time	Sleep mode	30	80	150	μs
$t_{GOTONORM}$	Go-to-Normal Time	Mode change time from Sleep, Standby mode into Normal mode	2	5	10	μs
$t_{INITNORM}$	Normal Mode Initialization Time		7	12	20	μs
$t_{GOTOSLEEP}$	Go-to-Sleep Time	Mode change time from Normal into Sleep mode	2	5	10	μs
$t_{TO\_DOM\_TXD}$	TXD dominant time-out time	V_{TXD} = 0 V	17	30	50	ms

(1) The data is based on bench tests and design simulation.

Parameter Measurement Information

Test Circuit

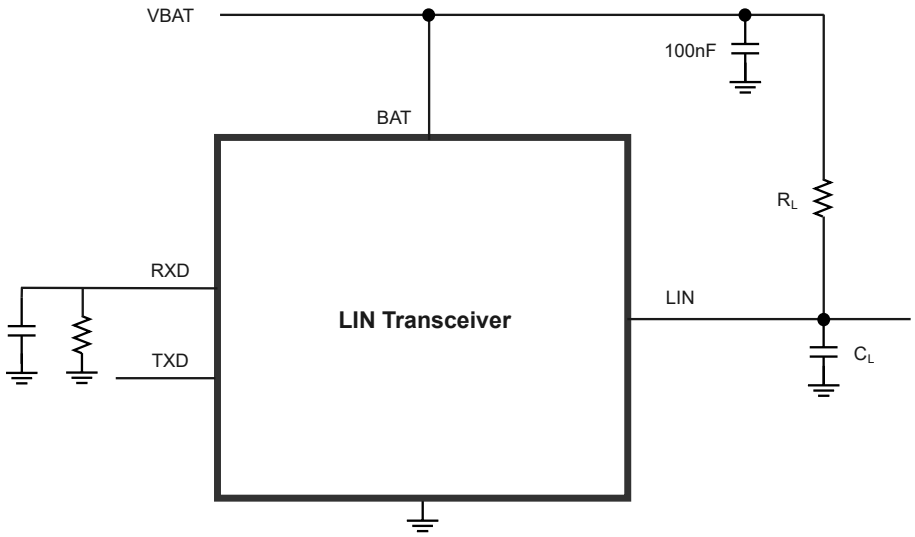


Figure 1. LIN Transceiver Timing Parameter Test Circuit

Parameter Diagram

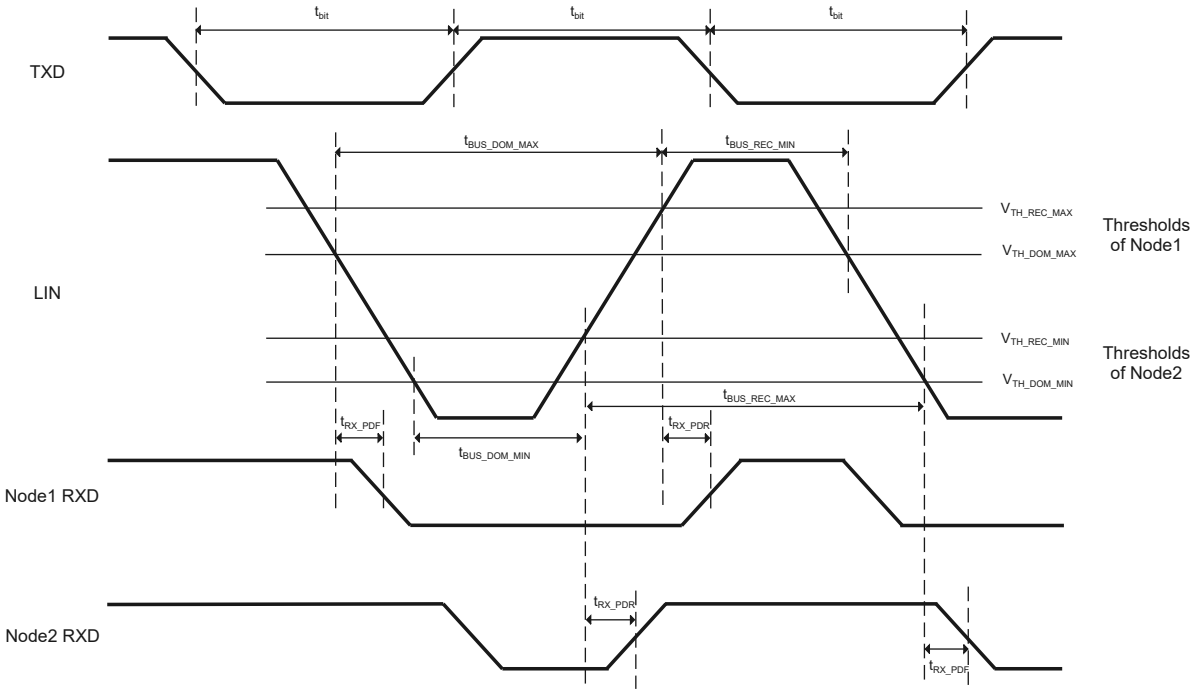


Figure 2. LIN Transceiver Timing Diagram

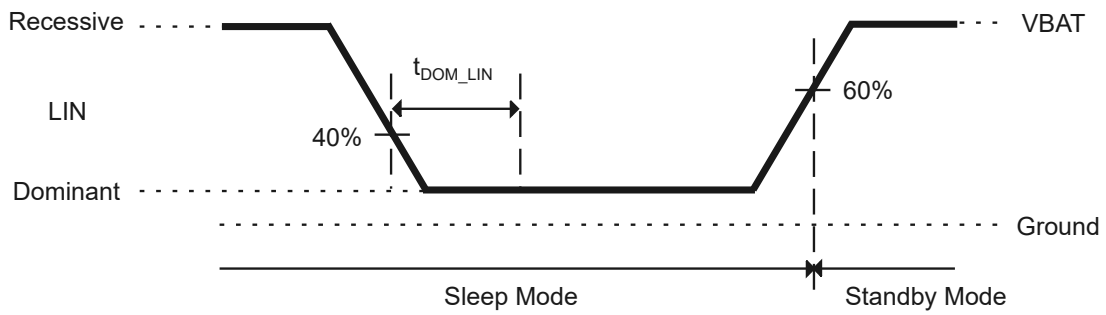


Figure 3. Remote Wake-up Diagram

Detailed Description

Overview

The TPT1022Q is a dual local interconnect network (LIN) physical layer transceiver that is compliant with the ISO 17987-4, SAE J2602 and LIN 2.0, LIN 2.1, LIN 2.2, and LIN 2.2-A physical layer standard. LIN is a low-speed universal asynchronous receiver transmitter (UART) communication protocol that supports automotive in-vehicle sub-networks. The device supports LIN networks up to 20 Kbps with an enhanced timing margin. The device converts the transmitted data received at the TXD with an optimized slew rate to minimize the electro-magnetic emission (EME) and reports the state of the LIN bus at the RXD. As designed, the device features overvoltage and loss of ground protection from −45 V to +45 V, over-temperature shutdown. The device has low-current standby and sleep mode with LIN BUS wake-up capability. The device integrates a pull high resistor for LIN slave applications and ESD protection which allows applications to operate with a reduced dependence on external components. Additionally, all devices include many protection features to enhance the device and network robustness. The TPT1022Q is available in SOP-14 and DFN3X4.5-14L packages and is AEC-Q100 qualified for automotive applications.

Functional Block Diagram

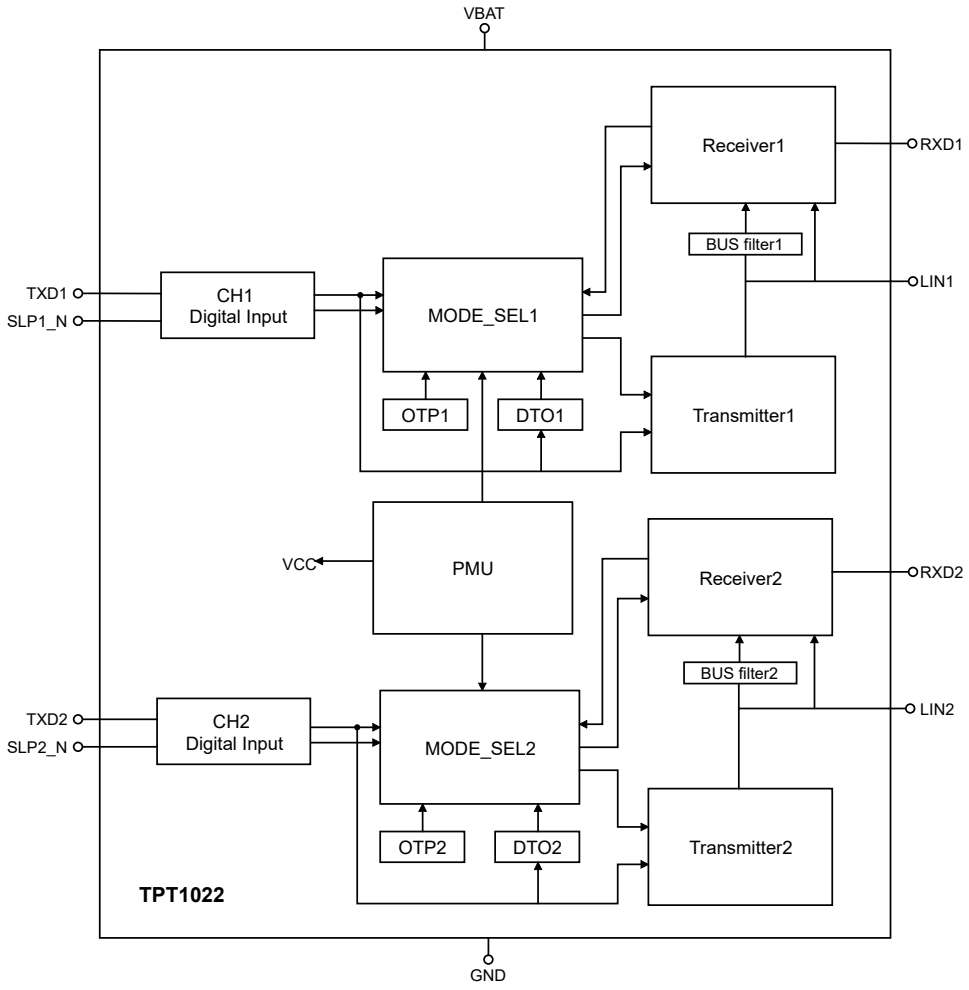


Figure 4. Functional Block Diagram

Feature Description

Device Operating Modes

The TPT1022Q supports modes for normal mode, power-on mode, standby mode, and sleep mode. The figure below shows the state diagram.

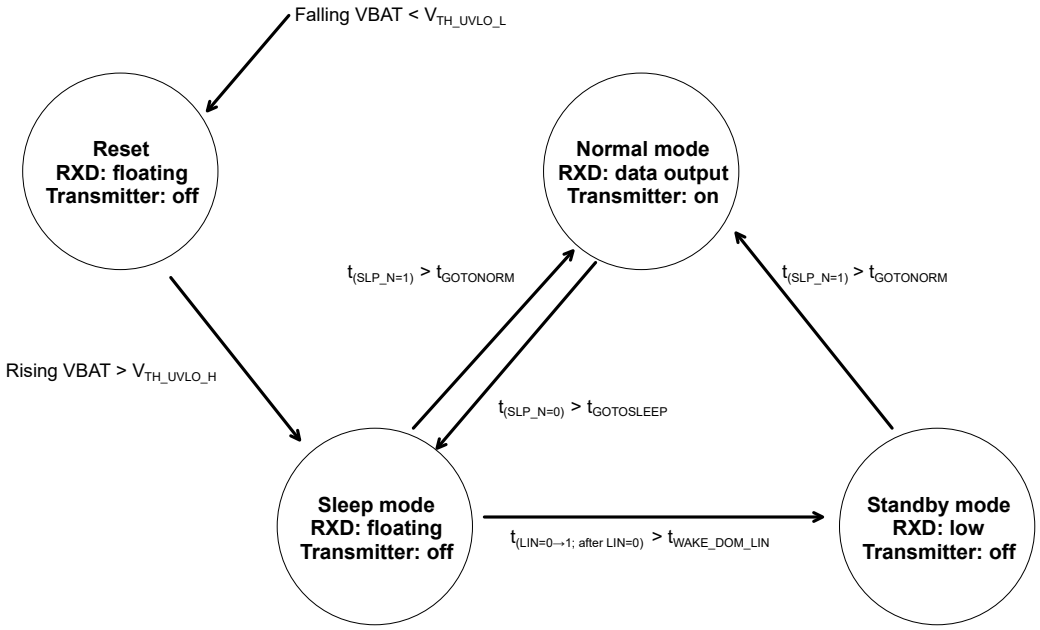


Figure 5. State Diagram

Table 2. Operation Mode Table

Mode	SLP_Nx	TXDx	RXDx	Transmitter	Comments
Normal	High	High: recessive state Low: dominant state	High: recessive state Low: dominant state	Normal	
Sleep	Low	Weak pull-down	Floating	Off	No wake-up event detected
Standby	Low	Weak pull-down	Low	Off	Wake-up event detected

Normal Mode

In Normal mode, the device can transmit and receive data through the LIN bus line. The receiver detects the data stream at the LIN bus input pin and transfers it to the microcontroller via the RXD pin. On the bus, a HIGH level corresponds to a recessive state, while a LOW level represents a dominant state. The receiver incorporates a voltage-dependent threshold with hysteresis and an integrated filter to suppress noise on the bus.

The transmit data stream from the protocol controller at the TXD input is converted by the transmitter into a bus signal with optimized slew rate and wave shaping, aiming to minimize electromagnetic emissions (EME). The LIN bus output pin is pulled HIGH through an internal slave termination resistor. For master applications, an external resistor in series with a diode should be connected between pin VBAT and pin LIN.

Sleep Mode

The device offers an energy-efficient mode known as the power-saving mode. Despite its extremely low current consumption, the device retains the capability to be remotely awakened via the LIN pin or directly activated through the SLP_N pin. Input filters are incorporated at the receiver (LIN), and SLP_N pin to prevent undesired wake-up events caused by automotive transients or electromagnetic interference (EMI).

To initiate Sleep mode from Normal mode, a falling edge on the SLP_N pin is required. In order to successfully enter Sleep mode, the sleep command (SLP_N pin set to LOW) must be sustained for a minimum duration of $t_{gotosleep}$.

During Sleep mode, the internal slave termination between the LIN and VBAT pins is disabled to minimize power dissipation if the LIN pin is short-circuited to ground. Only a weak pull-up is present between the LIN and VBAT pins.

When VBAT voltage drops below the undervoltage threshold, the device transitions into Sleep mode.

Standby Mode

Whenever a local or remote wake-up occurs while the device is in Sleep mode, Standby mode is automatically activated. These wake-up events enable the slave termination resistor at the LIN pin.

Standby mode is indicated by a low level on the RXD pin, which can serve as an interrupt for the microcontroller.

Wake-up

When VBAT voltage exceeds the undervoltage threshold voltage, the device transitions into Sleep mode. In this mode, both the transmitter and receiver remain inactive. If SLP_N is HIGH for a duration greater than t_gotonorm, the device enters Normal mode.

To wake up a device that is in Sleep mode, there are two methods:

Remote wake-up through the LIN bus by receiving a dominant bus state that is sustained for a duration of at least $t_{WAKE\_DOM\_LIN}$ then followed by a rising edge.

Mode change by setting the SLP_N pin to a HIGH level. This change in pin state signals the device to exit Sleep mode and enter Normal mode.

Protection Features

TXD Dominant Time-out

The device will detect TXD dominant time-out and prevent a permanent low on pin TXD driving the LIN bus into permanent dominant blocking the LIN bus network. If the TXD remains low for longer than t_{TXD_DTO} the transmitter will disable until the fault flag has been cleared.

Under-voltage Lockout (UVLO)

The device integrated under-voltage detect and lockout circuit of the supply terminal to keep the device in protected mode if the supply voltage drops below the threshold until the supply voltage is higher than the UVLO threshold. This protects the device and system during undervoltage events on supply terminals.

Over-Temperature Protection (OTP)

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{J_SD}, the output drivers will be disabled until the virtual junction temperature falls below $T_{J\_SD\_R}$ and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillation due to temperature drift is avoided.

Fail-safe Features

An internal pull-down to GND on the TXD pin to establish a predetermined level in case the TXD pin is disconnected.

An internal pull-down to GND on the SLP_N pin to establish a predetermined level in case the SLP_N pin is disconnected.

The RXD pin is set to floating when the VBAT pin is unpowered.

The current limit is applied to LIN transmitter output to protect LIN bus short circuits to VBAT or GND

VBAT and GND loss will not impact the LIN bus or the MCU. No reverse current flow from the bus into pin LIN. The internal integrated LIN slave termination resistor remains to keep the current path from VBAT to LIN. Disconnecting the LIN transceiver from the power supply does not affect the LIN bus.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

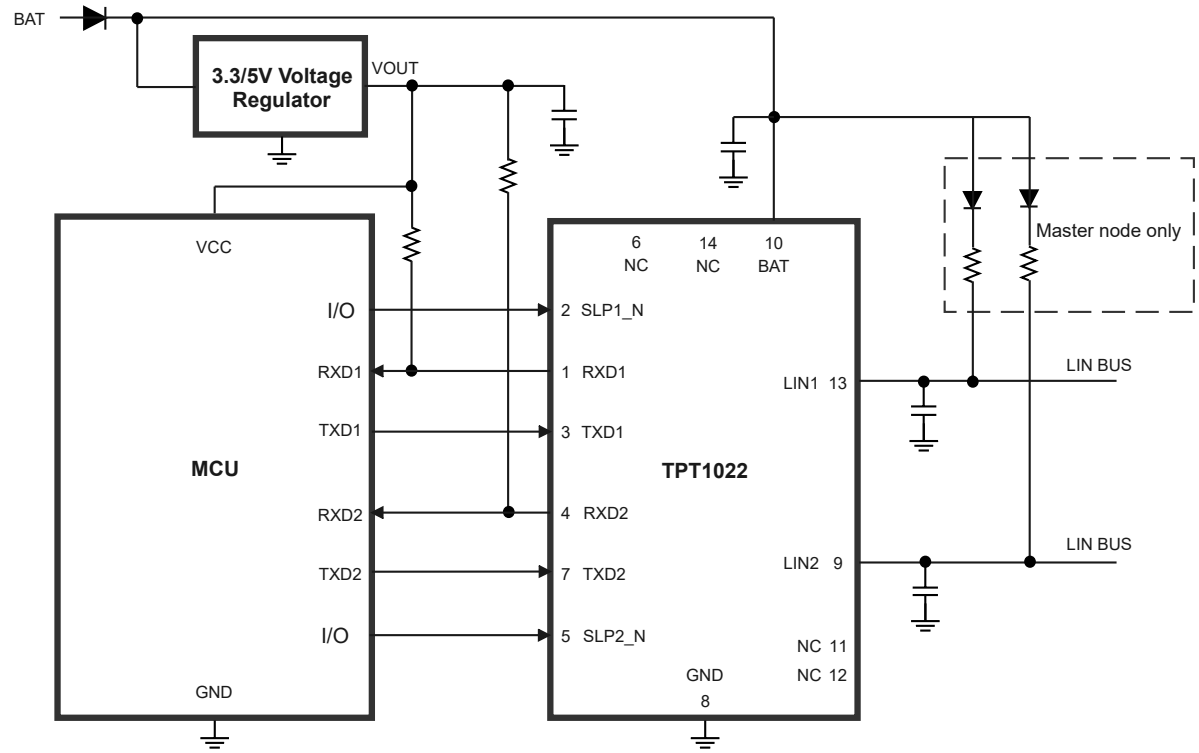
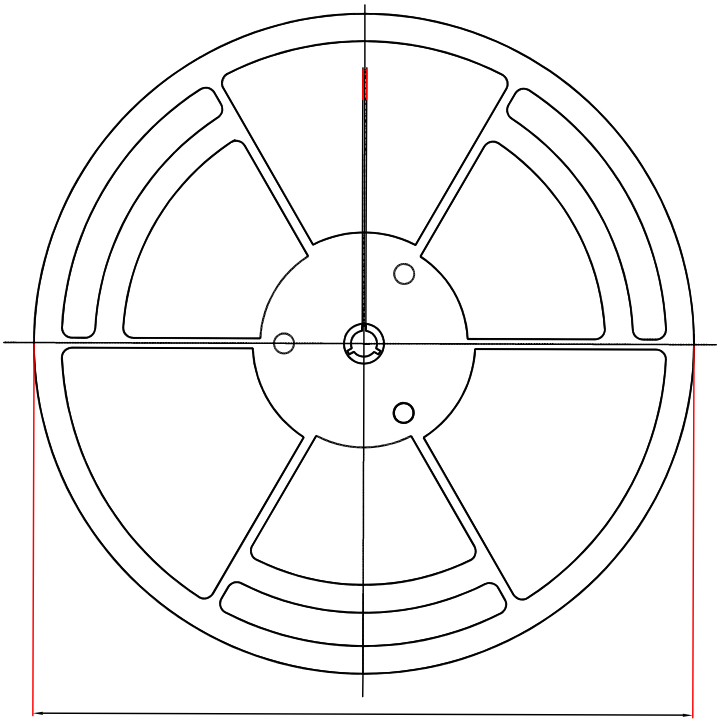
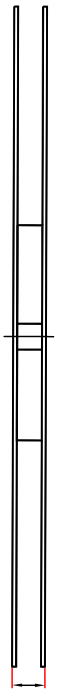
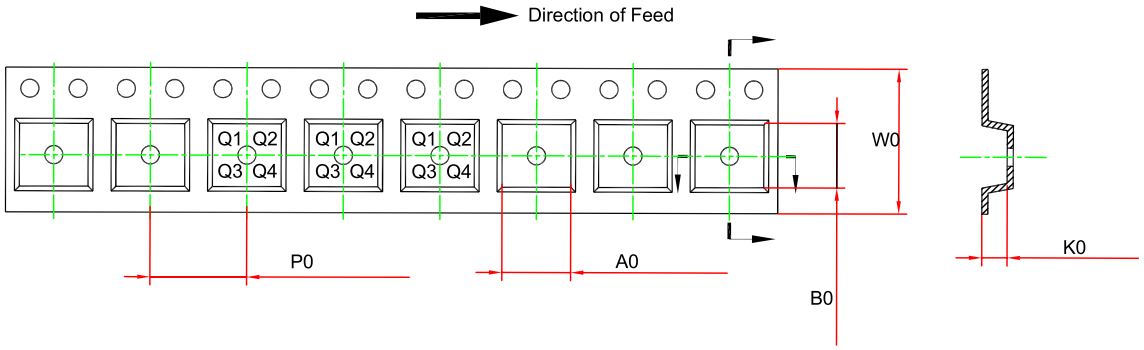


Figure 6. Typical Application Circuit

Tape and Reel Information





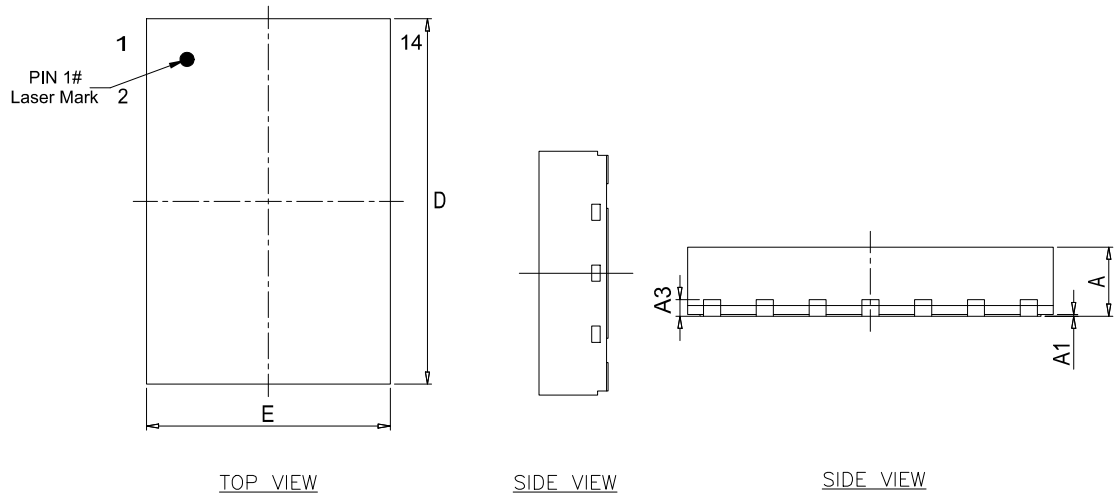


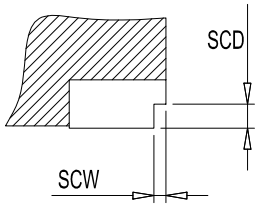
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT1022Q-DFKR-S	DFN4.5X3-14	330	17.6	3.3	4.8	1.1	8	12	Q1
TPT1022Q-SO2R-S	SOP-14	330	21.6	6.5	9.0	2.1	8	16	Q1

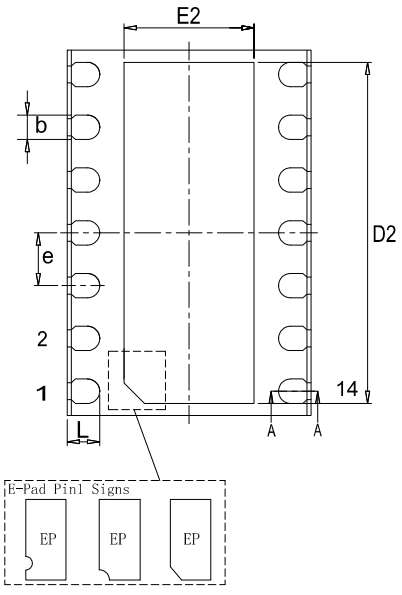
Package Outline Dimensions

DFN4.5X3-14-WET-B

Package Outline Dimensions DFK(DFN4.5X3-14-WET-B)







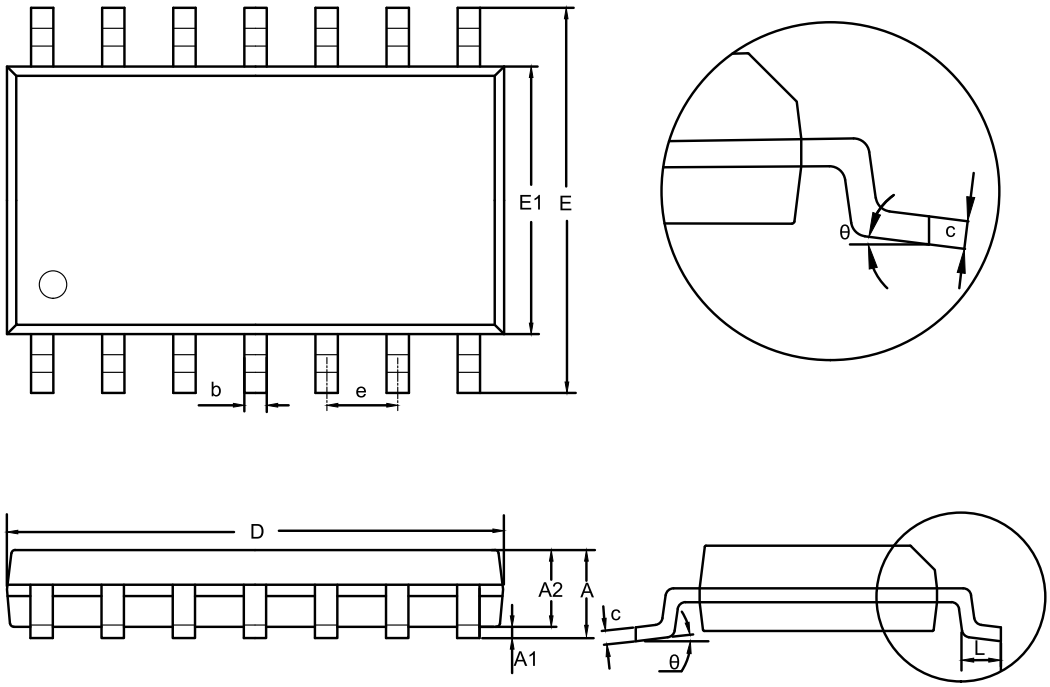
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.250	0.350	0.010	0.014
A3	0.203 REF		0.008 REF	
D	4.400	4.600	0.173	0.181
E	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.300	0.500	0.012	0.020
D2	4.100	4.300	0.161	0.169
E2	1.500	1.700	0.059	0.067
SCW	0.010	0.090	0.0004	0.004
SCD	0.080	0.180	0.003	0.007

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

SOP14

Package Outline Dimensions SO2(SOP-14-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT1022Q-DFKR-S	−40 to 125°C	DFN4.5X3-14	1022Q	MSL1	Tape and Reel,4000	Green
TPT1022Q-SO2R-S	−40 to 125°C	SOP-14	1022Q	MSL1	Tape and Reel,2500	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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