High-Side EFuse Controller with Protection and Diagnosis for Automotive Applications

Features

- Qualified for Automotive Applications
  - AEC-Q100 Grade 1, T_A: −40°C to +125°C
- Wide Input Voltage Range
  - 6 V to 52 V, with 65 V Maximum Rating
- High-Side Gate Driver to Control External N-Channel MOSFET
- 2-Stage Charge Pump Integrated
- Low Standby Current
- ADCs for Current and Voltage Conversion
  - Accurate Output Current Sense
  - Output Voltage and V_{DS} Sense
  - External MOSFET Temperature Sense with NTC Resistor
- External MOSFET Protection:
  - MOSFET Desaturation Shutdown Configurable via SPI
  - Hard Short Circuit Latch-off Configurable via SPI
  - Current-vs-Time Latch-off Configurable via SPI
  - MOSFET Over-Temperature Protection
- SPI Communication Interface
  - 32-bit Compatible with 3.3-V and 5-V CMOS Level
  - SPI slave interface for host control
  - Register Lock-Out by a Dedicated Pin
- Over-Temperature Protection
- Package Option:
  - QFN5X5-32

Applications

- Automotive Power Distribution Applications
- Automotive Zone Control Unit
- Automotive BMS, Automotive EIC system

Description

The TPS60C01Q is an eFuse controller with fault detection and protection for implementing of an intelligent high-side power switch for different automotive applications.

The TPS60C01Q supports operating voltage from 6 V to 52 V. This device provides high-side gate drive to control an external n-channel MOSFET with an integrated 2-stage charge pump. Also, this device can deliver 400-mA bypass current through the internal power path.

The TPS60C01Q integrates four ADCs to monitor the current and voltage, including output current through an external MOSFET, output voltage, and VDS voltage of the MOSFET, and external NTC resistor voltage of the MOSFET temperature.

The TPS60C01Q implements an external MOSFET protection function. Including MOSFET desaturation shutdown, hard short circuit latch-off, current-vs-time latch-off, and MOSFET over-temperature protection.

The TPS60C01Q uses a 32-bit SPI interface for register read/write operation, which is compatible with 3.3-V and 5-V CMOS levels.

The TPS60C01Q provides a thermal-enhanced QFN5X5-32 package and is guaranteed to operate within the ambient temperature range from – 40°C to +125°C.

Typical Application Circuit

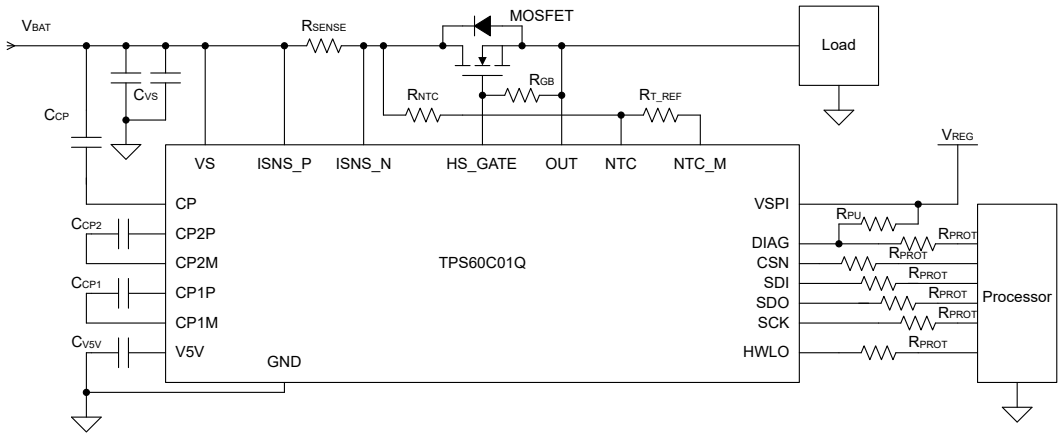


Table of Contents

Product Family Table

Order Number	Operating Voltage Range (V)	Package
TPS60C01Q-QFZR-S	6 to 52	QFN5X5-32

Revision History

Date	Revision	Notes
2023-12-31	Rev.Pre.0	Preliminary datasheet.
2025-04-03	Rev.Pre.1	Updated electrical characteristics.
2025-09-06	Rev.A.0	Initial released.

Pin Configuration and Functions

TPS60C01Q
QFN5X5-32 Package
Top View

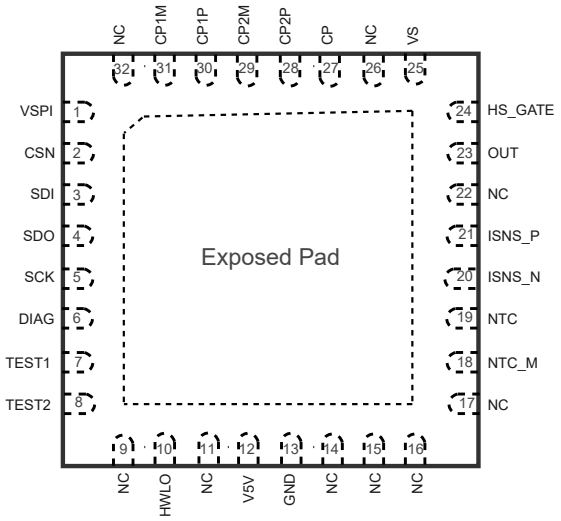


Table 1. Pin Functions: TPS60C01Q

Pin No.	Pin Name	I/O	Description
27	CP	O	Charge pump output.
31	CP1M	O	Charge pump–Negative terminal of the flying capacitor CP1.
30	CP1P	O	Charge pump–Positive terminal of the flying capacitor CP1.
29	CP2M	O	Charge pump–Negative terminal of the flying capacitor CP2.
28	CP2P	O	Charge pump–Positive terminal of the flying capacitor CP2.
2	CSN	I	Chip select not (active low) for SPI communication. It is the selection pin of the device. CMOS-compatible input.
6	DIAG	O	Open drain logic output. Diagnostic feedback. DIAG = '0' if (SR1.WAKEUPM = '1') or (GSB.DIAGS = '1') or (GSB.DE = '1') else '1'
13	GND	-	Ground connection.
24	HS_GATE	O	Output of the gate driver for the external FET.
10	HWLO	I	Active high input pin compatible with 3.3 V and 5 V CMOS; it causes transitions to states where the registers are locked from writing.
20	ISNS_N	I	Current sense amplifier negative input.
21	ISNS_P	I	Current sense amplifier positive input.

Pin No.	Pin Name	I/O	Description
9, 11, 14, 15, 16, 17, 22, 26, 32	NC	–	No internal connection.
19	NTC	I	Positive input pin for external NTC resistor.
18	NTC_M	I	Negative input pin for external NTC resistor.
23	OUT	O	External FET source connection.
5	SCK	I	Serial clock for SPI communication. It is a CMOS-compatible input.
3	SDI	I	Serial data input for SPI communication. Data is transferred serially into the device on the SCK rising edge.
4	SDO	O	Serial data output for SPI communication. Data is transferred serially out of the device on the SCK falling edge.
7	TEST1	–	Test mode pin 1- must be connected to ground.
8	TEST2	–	Test mode pin 2- must be connected to ground.
12	V5V	O	Output of the 5 V internal LDO voltage regulator (logic and I/O supply). Connect a low ESR capacitor (1 μF) close to this pin.
25	VS	I	Input supply pin. Connect to the 12 V, 24 V, and 48 V battery voltage.
1	VSPI	I	DC supply input for the SPI interface. 3.3 V and 5 V compatible.

(1) Thermal Pad **MUST** be connected to PCB ground plane directly.

Specifications

Absolute Maximum Ratings (1) (2) (3)

Parameter		Min	Max	Unit
V_{VS}		−0.3	70	V
V_{OUT}		−0.3	70	V
V_{HS_GATE}		−0.3	90	V
V_{CP}		−0.3	90	V
V_{CP1P}		−0.3	90	V
V_{CP2P}		−0.3	90	V
V_{CP1N}		−0.3	70	V
V_{CP2N}		−0.3	70	V
V_{ISNS_P}		−0.3	70	V
V_{ISNS_N}		−0.3	70	V
V_{NTC}		−0.3	70	V
V_{NTC_M}		−0.3	70	V
V_{VSPI}		−0.3	6	V
V_{CSN}		−0.3	6	V
V_{SCK}		−0.3	6	V
V_{SDI}		−0.3	6	V
V_{SDO}		−0.3	6	V
V_{V5V}		−0.3	6	V
V_{HWLO}		−0.3	6	V
V_{DIAG}		−0.3	6	V
T_J	Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.
(3) Not subject to production test, specified by design.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	AEC Q100-002	±2	kV
CDM	Charged Device Model ESD	AEC Q100-011, all pins	±1	kV

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{VS}		6	14	52	V
V_{VSPI}		3		5.5	V
V_{CSN}		3		5.5	V
V_{SCK}		3		5.5	V
V_{SDI}		3		5.5	V
V_{SDO}		3		5.5	V
V_{HWLO}		0		5.5	V
V_{DIAG}		0		5.5	V
T_A	Ambient Temperature Range	−40		125	°C
T_J	Junction Temperature Range	−40		150	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC,TOP}$	Unit
QFN5X5-32	25.9	4.07	15.2	°C/W

Electrical Characteristics

All test conditions: V_S = 6 V to 52 V, T_A = -40°C to +125°C. All typical values refer to V_S = 14 V, T_J = 25 °C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
VS	Operating Supply Voltage		6	14	52	V
VS_UV	VS Under-Voltage Lockout	VS falling	4.5			V
VS_UV_HYS	VS Under-Voltage Lockout Hysteresis	hysteresis		100		mV
t_{VS_UV}	VS under-Voltage Lockout Deglitch Time			33		μs
I_{VS_Q}	VS Quiescent Current with Logic Operating	VS = 52 V, OUT = VS			80	μA
		VS = 52 V, OUT = GND			80	μA
		VS = 14 V, OUT = VS			70	μA
		VS = 14 V, OUT = GND			70	μA
Is_ON	Supply Current with Logic Operating	f_{PWM} = 1 Hz, Q_G = 250 nC, VS= 48 V, OUT = VS		17		mA
I_{OUT}	Output Current	VS = 48 V, Stand-by mode, OUT = GND, Bypass switch OFF			1	μA
		VS = 14 V, Stand-by mode, OUT = GND, Bypass switch OFF			1	μA
		VS = 48 V, Unlocked mode, OUT=GND, Bypass switch OFF			1	mA
		VS = 13 V, Unlocked mode, OUT=GND, Bypass switch OFF			1	mA
VS_POR_ON	Power-On Reset Threshold.	Device leaves the Reset mode.		2.5		V
VS_POR_OFF	Power-on Shutdown Threshold.	Device enters Reset mode.		2.3		V
VS_POR_HYS	Power-on Reset Hysteresis			0.2		V
t_{PWON}	Time from Power-on to stand-by	VS>VS_POR_ON, V1V8 external capacitor 1 μF			450	μs
SPI Power Supply (SPI)						
V_{SPI}	SPI Interface Supply Voltage		3		5.5	V
I_{SPI}	SPI Interface Supply Current during Communication				3	mA
I_{SPI_STBY}	SPI Interface Supply Current in Standby State	T_A = 25°C			5	μA
SPI Logic Input (CSN, SCK and SDI)						

Parameter		Conditions	Min	Typ	Max	Unit
VIH	High-Level Logic Input Voltage		0.7			×VSPI
VIL	Low-Level Logic Input Voltage				0.3	×VSPI
VI_HYS	Input Hysteresis Voltage			0.4		V
VI_CLM	Input Clamp Voltage (SCK and SDI)			VSPI + 0.6		V
IIH	High-Level Logic Input Current (SCK and SDI)	VIH = 0.7×VSPI	0.5		5	μA
	High-Level Logic Input Current (CSN)	VIH = 0.7×VSPI	-5		-0.5	μA
IIL	Low-Level Logic Input Current (SCK and SDI)	VIL = 0.3×VSPI	0.5		5	μA
	Low-Level Logic Input Current (CSN)	VIL = 0.3×VSPI	-5		-0.5	μA
SPI Logic Output (SDO)						
VOH	High-Level Logic Output Voltage		0.8			×VSPI
VOL	Low-Level Logic Output Voltage				0.2	×VSPI
IOL	Low-Level Logic Output Current		-10		10	μA
SPI Timing						
fSPI	SPI Clock Frequency				8	MHz
tCSN	CSN Low Timeout	VSPI = 3.3 V, RPROT < 1 kΩ	30		70	ms
tWDTB	Watchdog Toggle Bit Timeout.	WD_TIME Configuration: 00	-10%	50	10%	ms
		WD_TIME Configuration: 01	-10%	100	10%	ms
		WD_TIME Configuration: 10	-10%	150	10%	ms
		WD_TIME Configuration: 11	-10%	200	10%	ms
tSTBY_OUT	Minimum time during which CSN must be toggled low to go out of STDBY mode		20		100	μs
HWLO Logic Input(HWLO)						
VIH	High-Level Logic Input Voltage		2.1			V
VIL	Low-Level Logic Input Voltage				0.9	V
VI_HYS	Input Hysteresis Voltage			0.4		V
IIH	High-Level Logic Input Current		0.5		2.5	μA
IIL	Low-Level Logic Input Current		0.5		2.5	μA
tHWLO	HWLO Deglitch Time			33		μs
DIAG Logic Output (DIAG)						
VDIAG_PD	DIAG Pin Low-Level Output Voltage				0.2	V
IDIAG_PD	DIAG Pin Low-Level Sink Current	VDIAG = VDIAG_PD			1	mA

Parameter		Conditions	Min	Typ	Max	Unit
IDIAG_LKG	DIAG Pin Leakage Current	VDIAG = VSPI = 5.5 V	0		1	μA
Charge Pump						
VCP	Charge Pump Output Voltage	VS = 6 V	VS + 7	VS + 11		V
		VS ≥ 10 V	VS + 13.5	VS + 14.5	VS + 15.5	V
VCP_H	Charge Pump Output Under-Voltage High Threshold	Ramp up on VCP	VS + 5.6	VS + 6	VS + 6.7	V
VCP_L	Charge Pump Output Under-Voltage Low Threshold	Ramp down on VCP	VS + 5.3	VS + 5.6	VS + 6.4	V
VCP_HYS	Charge Pump Output Under-Voltage Hysteresis			0.4		V
fCP	Charge Pump Frequency		-5%	450	5%	kHz
tCP_RISE	Charge Pump Low (CP_LOW diagnostic) Rising Edge Deglitch Time		-5%	60	5%	μs
tCP_FALL	Charge Pump Low (CP_LOW diagnostic) Falling Edge Deglitch Time		-10%	2.3	10%	μs
External MOSFET Gate Driver (HS_GATE)						
VGSON	Gate-ON Voltage	VS = 6 V, IG = 50 μA	6			V
		VS ≥ 10 V, IG = 50 μA	12		15	V
VGSOFF	Gate-OFF Voltage				0.5	V
VGSMAX	Maximum Gate Voltage (Internal Limited)				20	V
tON	Gate Turn ON Time	VGS = 0.5 V to VGS = 10 V, CGATE = 80 nF			4	μs
tOFF	Gate Turn OFF Time	Full VGS to VGS < 0.5, CGATE = 80 nF			2.6	μs
VGS_UVLO	Gate Under-Voltage Lockout	VS = 6 V	9			V
		VS ≥ 10 V	9.2			V
tGS_UVLO	Gate Under-Voltage Lockout Blanking Time	Enable at Charge Pump startup if Ext FET turn-on is required, and applied after CP_LOW expiration (falling edge)	-6%	100	6%	μs
	Gate Under-Voltage Lockout Deglitch Time		-15%	8	15%	μs
QG_MAX	Maximum Gate Charge	VGS = 10 V			800	nC

Parameter		Conditions	Min	Typ	Max	Unit
External MOSFET VDS Monitor						
VDS_TH	VDS Monitor Threshold Range	31 steps adjustable through SPI	300		1800	mV
	VDS Monitor Threshold Step			50		mV
VDS_TH_0				300		mV
VDS_TH_15				1050		mV
VDS_TH_30				1800		mV
VDS_ADC_FS	Full Scale Range Resolution of VDS Monitor ADC	VDS_ADC_FS[9:0] = MIN((VSENSE_N - VOUT)/2 * 1024, 957)	0		957	
VDS_ADC_SR	Sample Rate of VDS Monitor ADC			0.9		Msample/s
VDS_TH_ACC	VDS Monitor Threshold Accuracy		-5%		5%	
tDS_DEG	VDS Monitor Shut-Off Deglitch Time		-25%	5	25%	μs
tDS_DLY	VDS Monitor Shut-Off Delay Time				5	μs
tDS_BLK	VDS Monitor Shut-Off Blanking Time	At High Side External FET startup	-10%	960	10%	μs
Current Sense Amplifier with Integrated ADC (ISNS_P and ISNS_N)						
VISNS_CM	Current Sense Common-Mode Input Voltage Range		0		70	V
VISNS_FS	Full Scale Range of Current Sense Differential Input Voltage		0		160	mV
IISNS_P	ISNS_P Pin Input Current			40		μA
IISNS_N	ISNS_N Pin Input Current			270		μA
VISNS_ADC_RES	Full Scale Range Resolution of Current Sense ADC	VISNS_ADC_FS[12:0] = MIN((VSENSE/160×8192), 8191)	0		8191	
VISNS_ADC_SR	Sample Rate of Current Sense ADC			2.4		kSamples/s
VISNS_ACC	Current Sense Accuracy	1.8 mV < ΔVISNS < 6 mV	-17%		17%	
		6 mV < ΔVISNS < 10 mV	-10%		10%	
		ΔVISNS = 10 mV	-5%		5%	
		ΔVISNS > 20 mV	-3%		3%	
Output Short Circuit Protection						
VSC_TH	Output Short Circuit Protection Threshold Range	16 steps adjustable through SPI	20		160	mV

Parameter		Conditions	Min	Typ	Max	Unit
VSC_TH_0				20		mV
VSC_TH_8				60.6		mV
VSC_TH_16				160		mV
VSC_ADC_FS	Full Scale Range of Short Circuit Protection ADC	VSC_ADC_FS[9:0] = MIN((VSENSE/160*1024), 1023)	0		1023	
VSC_ADC_SR	Sample Rate of Short Circuit Protection ADC			0.9		Msample/s
VSC_ACC	Output Short Circuit Protection Threshold Accuracy		-5%		5%	
tSC_DLY	Output Short Circuit Protection Delay Time				5	μs
Output Over Current Protection						
VOC_TH	Output Over Current Protection Threshold Range	32 steps adjustable through SPI	6		90	mV
VOC_TH_0			-12%	6	12%	mV
VOC_TH_2			-12%	8.7	12%	mV
VOC_TH_3			-7%	10.4	7%	mV
VOC_TH_12			-7%	20.4	7%	mV
VOC_TH_13			-5%	21.8	5%	mV
VOC_TH_31			-5%	89.3	5%	mV
tI-t	I-t tolerance on time step (y axis)		(t - 10%) - 32		(t + 10%) + 32	μs
tSAMPLING	Shunt Current Sampling Time		-10%	61	10%	μs
External MOSFET Thermal Protection via NTC Input (NTC and NTC_M)						
VNTC	NTC Input Voltage Range		VISNS_N-1.2		VISNS_N	V
VNTC_M	NTC_M Output Voltage			VISNS_N-1.2		V

Parameter		Conditions	Min	Typ	Max	Unit
VNTC_ACC	NTC Input Voltage Threshold Accuracy		-3		3	mV
VNTC_TH_0	External FET Thermal Protection NTC Input Voltage Threshold			110.92		mV
VNTC_TH_1				98.76		mV
VNTC_TH_2				88.07		mV
VNTC_TH_3				78.66		mV
VNTC_TH_4				70.38		mV
VNTC_TH_5				63.08		mV
VNTC_TH_6				56.64		mV
VNTC_TH_7				50.95		mV
VNTC_TH_8				45.92		mV
VNTC_TH_9				41.46		mV
VNTC_TH_10				37.5		mV
VNTC_TH_11				37.5		mV
VNTC_TH_12				37.5		mV
VNTC_TH_13					37.5	
VNTC_TH_14				37.5		mV
VNTC_TH_15				37.5		mV
VNTC_ADC_FS	Full Scale Range of External MOSFET Thermal Protection NTC ADC	VNTC_ADC_FS[9:0] = MIN(((VSENSE_N - VNTC)/1.2 * 1024), 1023)	0		1023	
VNTC_ADC_SR	Sample Rate of External MOSFET Thermal Protection NTC ADC			4.9		kSamples/s
VNTC_DEG	External MOSFET Thermal Protection Deglitch Time		10		500	μs

Parameter		Conditions	Min	Typ	Max	Unit
Internal Bypass Switch						
VBP_SAT	Internal Bypass Switch VDS Saturation Protection Threshold		1		2.5	V
IBP_SAT	Internal Bypass Switch Saturation Current	VS - VOUT = VDS_BYPASS_SAT	300			mA
RBP_ON	Internal Bypass Switch Turn-ON Resistance		1	3	5.2	Ω
tBP_ON	Internal Bypass Switch Turn-ON Time				100(VS> 8V) 125(VS= 6V)	μs
tBP_SAT_DEG	Internal Bypass Switch Saturation Diagnostic Deglitch Time		2.9		5.5	μs
VOUT Monitor						
VOUT_ADC_FS	Full-Scale Range of Output Voltage Monitor ADC	VOUT_ADC_FS[9:0] = MIN(VOUT/(51*1.2)*1024, 1023)	0		1023	
VOUT_ADC_SR	VOUT ADC Sample Rate			4.9		kSamples/s
Internal Thermal Protection						
TSD	Internal Thermal Shutdown Threshold		160	175		°C
	Internal Thermal Shutdown Hysteresis			15		°C
TINT_ADC_FS	Full Scale Range of Internal Junction Temperature ADC	TINT_ADC_FS[9:0] = (TJ + 72) * 3	0		1023	
TINT_ADC_SR	Sample Rate of Internal Junction Temperature ADC			10		kSamples/s

(1) Not subject to production test, specified by design.

Typical Performance Characteristics

All test conditions: V_S = 13.5 V, unless otherwise noted.

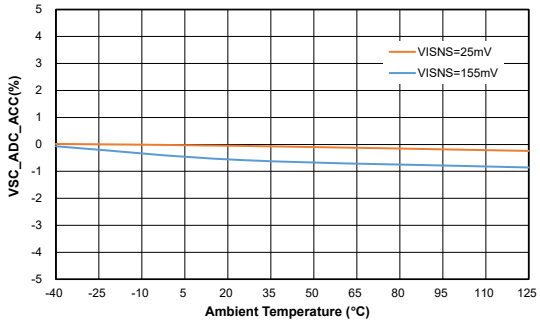


Figure 1. VSC ADC Accuracy vs. Temperature

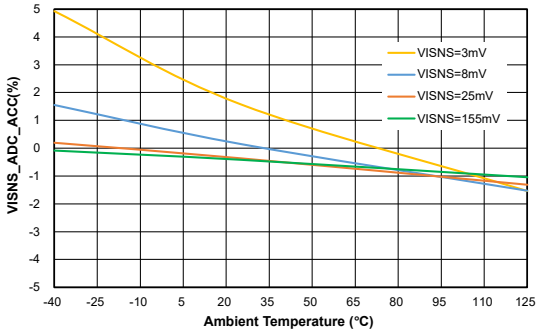


Figure 2. VISNS ADC Accuracy vs. Temperature

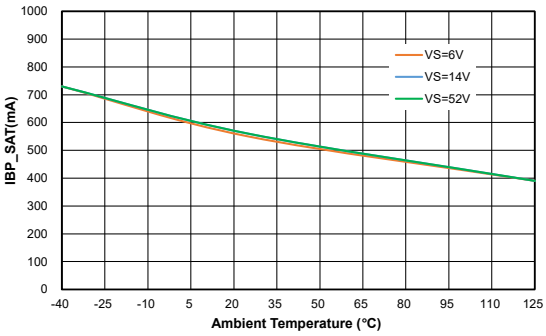


Figure 3. IBP SAT vs. Temperature

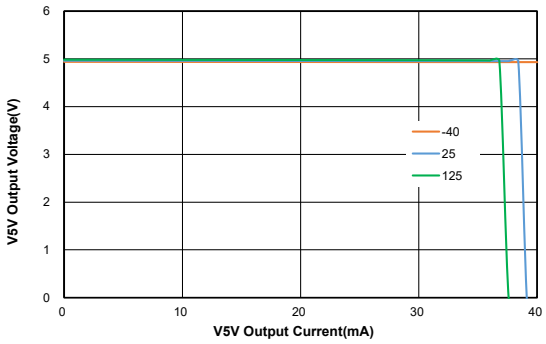


Figure 4. Vout vs. Current

Register Map

Address	Reg Name	Reg Description	Width	Field	Field Name	Access Right	Field Description
01h	CR1	Control Register 1	32	[31:13]	(reserved)	RO	reserved
				[12]	PWM_ON	RW_E	enable PWM for capacitive charge mode, active high
				[11]	GOSTBY	RW_E	GOSTBY can be set to 1 only if UNLOCK = 1; trying to set this bit to 1 when UNLOCK = 0 will have no effects and it will maintain its previous value. GOSTBY can be reset to 0 also when UNLOCK = 0. To send a GOToStandby sequence it is necessary to send two consecutive SPI frames, as follows: 1st SPI write operation to set UNLOCK bit to 1 2nd SPI write operation to set GOSTBY bit to 1 and EN bit to 0. A transition to Standby state causes GOSTBY to be reset to 0.
				[10]	EN	RW_E	EN can be set to 1 only if UNLOCK = 1; trying to set this bit to 1 when UNLOCK = 0 will have no effects and it will maintain its previous value. EN can be reset to 0 also when UNLOCK = 0. To send a GOToUnlocked sequence it is necessary to send two consecutive SPI frames as follows: 1st SPI write operation to set UNLOCK bit to 1 2nd SPI write operation to set GOSTBY bit to 0 and EN bit to 1.

Address	Reg Name	Reg Description	Width	Field	Field Name	Access Right	Field Description
							A transition to Unlocked state causes EN to be set to 1. A transition to Locked state causes EN to be reset to 0.
				[9]	S_T_START	RW_E	When it is set to 1, starts selected self-test. If current state is Unlocked and S_T_CFG is not 000, then setting this bit causes a transition to Self-Test state. This bit is automatically reset.
				[8]	S_T_STOP	RW_E	When it is set to 1, stops execution of selected self-test. This bit is automatically reset.
				[7:5]	S_T_CFG	RW_E	Self Test selection: 000: No selection 001: Current sense 010: VDS detection 100: Power switch stuck-on 011: Current sense + VDS detection 101: Current sense + Power switch stuck-on 110: VDS detection + Power switch stuck-on 111: Current sense + VDS detection + Power switch stuck-on
				[4]	OUTCTL	RW_E	Enables High Side through SPI 1: HS Gate driver commanded on 0: HS Gate driver commanded off
				[3]	BYPASSCTL	RW_E	Enables Low Current Bypass through SPI

Address	Reg Name	Reg Description	Width	Field	Field Name	Access Right	Field Description
							1: LCB commanded on 0: LCB commanded off
				[2]	(reserved)	RO	reserved
				[1]	WD_TRIG	RW_E	Mirror of WD_TRIG bit
				[0]	(reserved)	RO	reserved
02h	CR2	Control Register 2	32	[31:24]	(reserved)	RO	reserved
				[23:16]	T_NOM	RW_E	Configures the value of Nominal Time, required for the fuse emulation: tNOM (s) = b{T_NOM(7:0), 1} T_NOMmin = 00000000 → tNOM (s) = b000000001 = 1s T_NOMmax = 11111111 → tNOM (s) = b111111111 = 511s Nominal Time corresponds to the trip time obtained when current is equal to the Nominal Overcurrent Threshold (OVC_THR).
				[15:11]	OVC_THR	RW_E	Configures the value of Nominal Overcurrent Threshold. The threshold can be set in the range 6 mV to 90 mV See Table 16
				[10:7]	HSHT_THR	RW_E	Configures a threshold for Hard Short Circuit Latch-off. The threshold can be set in the range from 20 mV to 160 mV. See Table 15

Address	Reg Name	Reg Description	Width	Field	Field Name	Access Right	Field Description
				[6:2]	VDS_THR	RW_E	Configures a threshold for External MOSFET desaturation shut-down. The threshold can be set in the range from 0.3 V to 1.80 V in steps of 50 mV (default = 300 mV). Configuration 0x1F is reserved.
				[1]	WD_TRIG	RW_E	Mirror of WD_TRIG bit
				[0]	(reserved)	RO	reserved
03h	CR3	Control Register 3	32	[31:21]	(reserved)	RO	reserved
				[20]	ntc_warning_en	RW_E	0: when ntc > ntc_thr, protection active 1; when ntc > ntc_thr, only warning by DIAG and sr register, not trig protection
				[19]	pwm_auto_stop_en	RW_E	enable pwm auto stop
				[18:13]	pwm_auto_stop_thr	RW_E	when VOUT[9:4]>pwm_auto_stop_thr[5:0], pwm finish, hgate keep on. Threshold: 51*1.2*{pwm_auto_stop_thr[5:0], 4'b0}/1024
				[12:10]	hsht_blk	RW_E	hard short blanking: 0: 0 µs 1: 50 µs 2: 100 µs 3: 200 µs 4: 500 µs 5: 1 ms 6: 1.5 ms

Address	Reg Name	Reg Description	Width	Field	Field Name	Access Right	Field Description
							7: 2 ms
				[9]	UNLOCK	RW_E	0: bits GOSTBY, EN cannot be set to 1 but can be reset; 1: bits GOSTBY, EN can be set to 1, but only with the next valid SPI frame. When UNLOCK = 1, it will be automatically reset with the next valid SPI frame.
				[8:5]	NTC_THR	RW_E	Configures a threshold for External MOSFET over-temperature shutdown via NTC. The threshold can be set in the range 37.50 to 110.92. See Table 17
				[4:3]	WD_TIME	RW_E	Watchdog time selection: 00: tWD = 50ms 01: tWD = 100ms 10: tWD = 150ms 11: tWD = 200ms
				[2]	DIS_OUT_MODE	RW_E	Outputs status in Locked state: 0: leave output and bypass as they are (default) 1: shut off output and bypass
				[1]	WD_TRIG	RW_E	In order to keep device in Unlocked Mode, this bit must be cyclically toggled within a period equal to tWD to refresh the watchdog.
				[0]	(reserved)	RO	reserved
04h	CR4	Control Register 4	32	[31:20]	(reserved)	RO	reserved

Address	Reg Name	Reg Description	Width	Field	Field Name	Access Right	Field Description
				[19:18]	PWM_HSHT_BLK	RW_E	00: vds no pwm blanking 01: vds pwm stage 1 blanking 1x: vds pwm stage 1 and 2 blanking (default)
				[17:10]	PWM_C2_TON	RW_E	PWM charge stage 2 Ton setting: range: 0us~255us, one step 1us 0x0 configuration: high side driver controlled by protection only
				[9:2]	PWM_C1_TON	RW_E	PWM charge stage 1 Ton setting: range: 0 μs~255 μs, one step 1us 0x0 configuration: high side driver controlled by protection only
				[1]	WD_TRIG	RW_E	In order to keep device in Unlocked Mode, this bit must be cyclically toggled within a period equal to tWD to refresh the watchdog.

Detailed Description

Overview

The TPS60C01Q is an eFuse controller with fault detection and protection for the implementation of an intelligent high-side power switch for different automotive applications.

The TPS60C01Q supports operating voltage from 6 V to 52 V. This device provides high-side gate drive to control an external n-channel MOSFET with an integrated 2-stage charge pump. Also, this device can deliver 400-mA bypass current through the internal power path.

The TPS60C01Q integrates four ADCs to monitor the current and voltage, including output current through external MOSFET, output voltage and VDS voltage of the MOSFET, and external NTC resistor voltage of the MOSFET temperature.

The TPS60C01Q implements an external MOSFET protection function. Including MOSFET desaturation shutdown, hard short circuit latch-off, current-vs-time latch-off, and MOSFET over-temperature protection.

The TPS60C01Q uses a 32-bit SPI interface for register read/write operation, which is compatible with 3.3-V and 5-V CMOS levels.

The TPS60C01Q provides a thermal-enhanced QFN5X5-32 package and is guaranteed to operate within the ambient temperature range from – 40°C to +125°C.

Functional Block Diagram

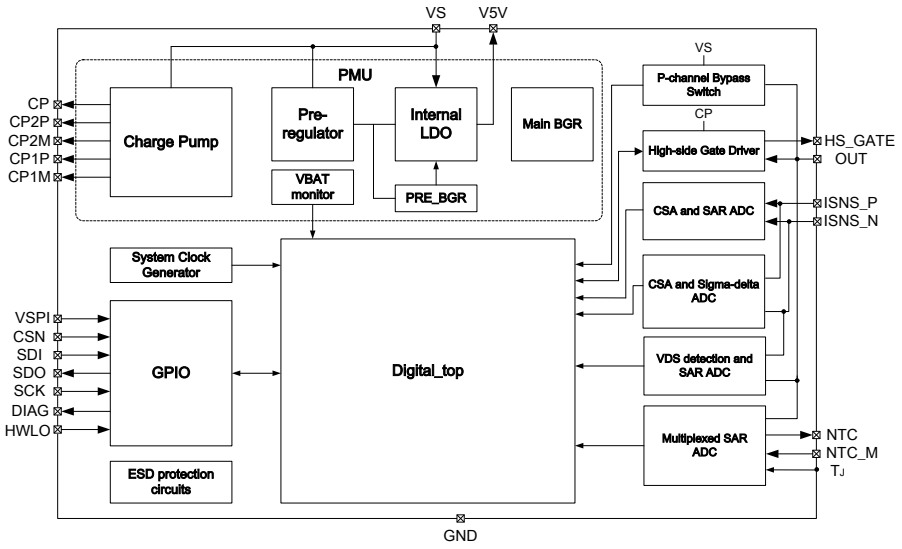


Figure 5. Functional Block Diagram

Feature Description

TPS60C01Q overview

Protection of wire harnesses and PCBs can be achieved by defining an ideal time-to-fuse curve based on the maximum power dissipation over time in the wires or copper PCB traces. This approach ensures that the insulation of wires and PCB substrates remains within a limited temperature and time budget, staying below reliability-specified thresholds. Exceeding these limits may lead to carbonization of organic insulation materials, forming conductive paths that can create local hot spots, sparking, and potentially fire ignition.

The VNF1048F incorporates ST's proprietary eFuse functionality, which provides a robust and flexible overcurrent protection mechanism. This intelligent circuit-breaking feature is designed to protect PCB traces, connectors, and wire harnesses from overheating, without affecting load transients such as inrush currents and capacitor charging.

The eFuse function is configured using two parameters: INOM and tNOM. INOM represents the maximum continuous current allowed, while tNOM determines the current versus time-to-fuse curve when the load current exceeds INOM. The relationship between current and time-to-fuse is approximated by an optimized stepwise function, adjustable within a range bounded by the wire I^2t limit on one end and load transient characteristics on the other. The tNOM value corresponds to the first step-up point of this curve. This current-time curve operates in conjunction with a very fast overcurrent protection mechanism, which triggers immediately when the current reaches a predefined threshold under hard short-circuit conditions.

When the load current is pulse-width modulated (PWM), the eFuse function calculates the root mean square (RMS) value of the current. RMS current measurement also occurs during power switching under normal operation, or after a shutdown due to short-circuit or overload conditions. For example, if the circuit is interrupted due to an overload and subsequently reactivated, the eFuse retains memory of the previous condition and continues to ensure that the maximum IRMS does not exceed INOM.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPS60C01Q is an eFuse controller with fault detection and protection for the implementation of an intelligent high-side power switch for different automotive applications.

Typical Application

Figure 6 shows the typical protection application schematic of the TPS60C01Q.

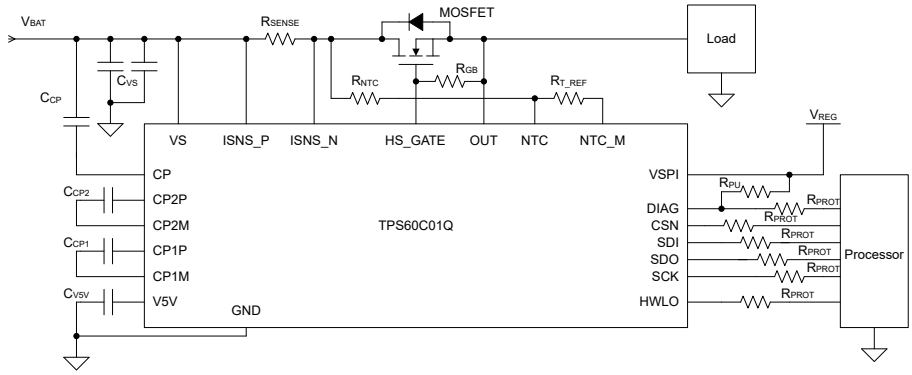


Figure 6. Typical Application Circuit

Layout

Layout Guideline

To get good thermal performance and prevent over-temperature protection, the PCB layout is important. A well-designed PCB layout can effectively optimize heat dissipation, which is crucial for ensuring the long-term reliability of the device.

- It is recommended to maximize the coverage of copper on the PCB to enhance the thermal conductivity of the board. Since the primary heat flow path from the package to the surrounding environment passes through the copper on the PCB, having maximum copper coverage is particularly important when there is no heat sink attached to the opposite side of the board.
- It is recommended to place as many thermal vias as possible underneath the package ground pad to optimize the thermal conductivity of the board.
- It is suggested that all thermal vias be either plated shut or plugged and capped on both sides of the board to prevent solder voids to maintain reliability and performance.
- It is recommended to use wide traces or thick copper weight in the input/output current paths to minimize I×R voltage drop.

Layout Example

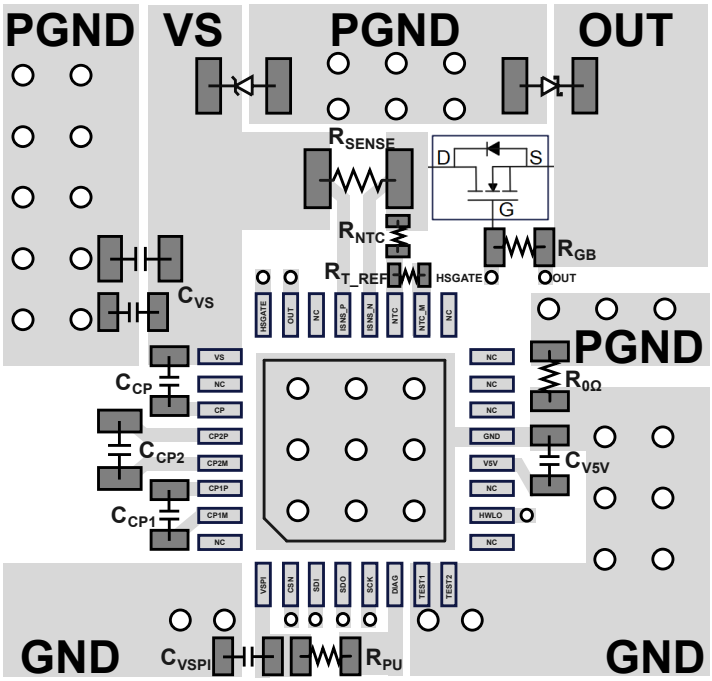
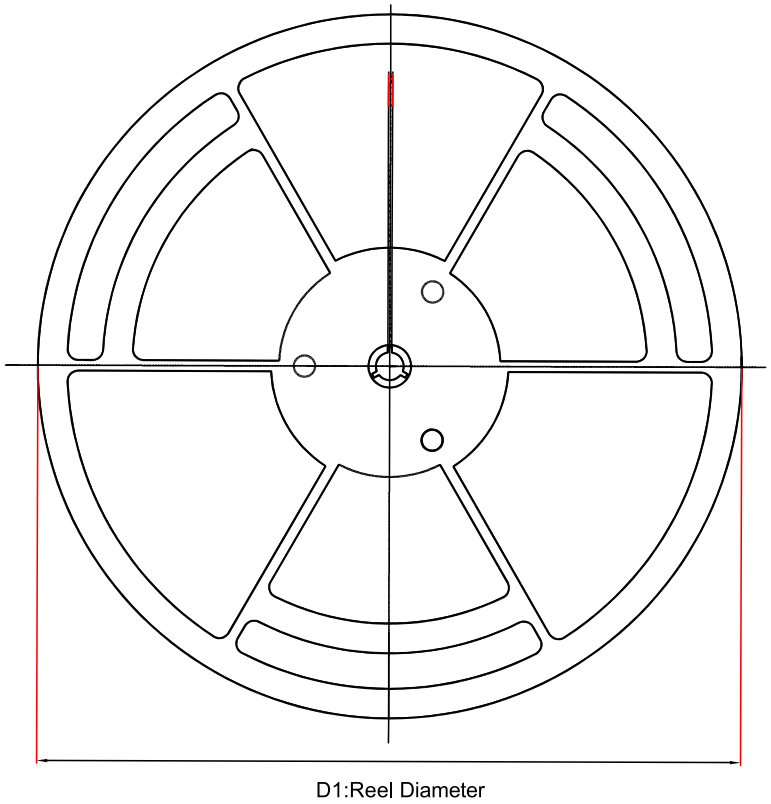
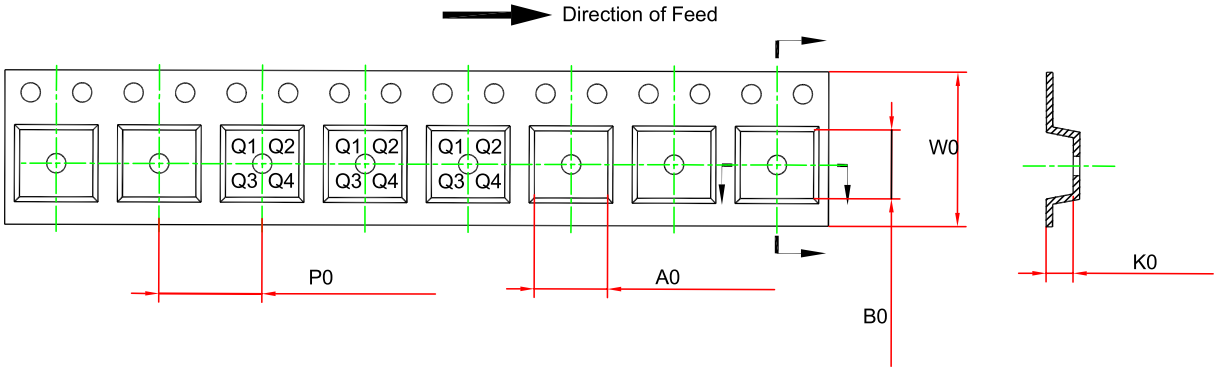


Figure 7. Layout Example

Tape and Reel Information



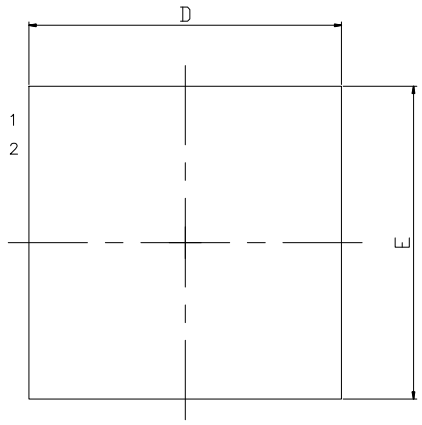


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPS60C01Q-QFZR-S	QFN5X5-32	330	17.6	5.3	5.3	1.1	8	12	Q2

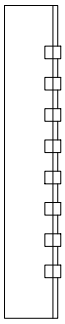
Package Outline Dimensions

QFN5X5-32-WET

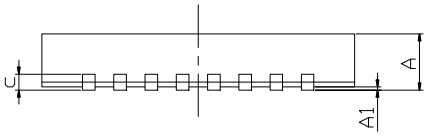
Package Outline Dimensions QFZ(QFN5X5-32-WET-H)



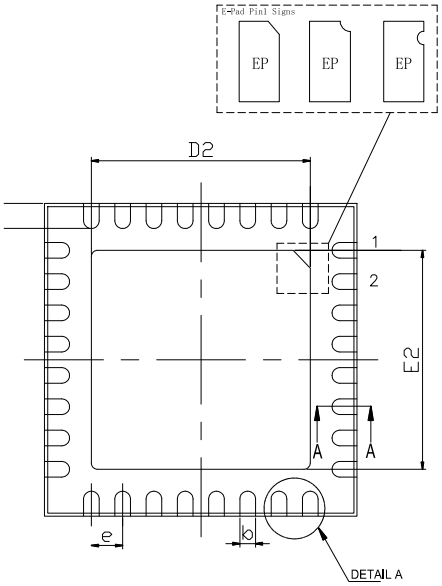
TOP VIEW



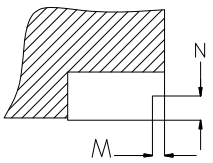
SIDE VIEW



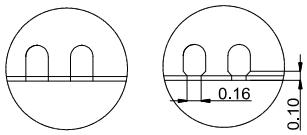
SIDE VIEW



BOTTOM VIEW



Section A-A



引脚根部 Option A 引脚根部 Option B

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
c	0.180	0.250	0.007	0.010
D	4.900	5.100	0.193	0.201
E	4.900	5.100	0.193	0.201
e	0.500 BSC		0.020 BSC	
D2	3.400	3.600	0.134	0.142
E2	3.400	3.600	0.134	0.142
L	0.350	0.450	0.014	0.018
M	0.010	0.090	0.000	0.004
N	0.080	0.180	0.003	0.007

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPS60C01Q-QFZR-S	−40 to 125°C	QFN5X5-32	60C01	MSL3	3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

Disclaimer. 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.

This page intentionally left blank