Automotive 40-V 100-mΩ 1-Channel High-Side Power Switch

Features

- Qualified for Automotive Applications
  - AEC-Q100 Grade 1, T_A: −40°C to +125°C
  - Junction Temperature, T_J: −40°C to +150°C
- Wide Input Voltage Range
  - 4 V to 40 V, with 45 V Maximum Rating
- 100-mΩ Maximum Low Turn-On Resistance at Room Temperature
- 0.5-μA Maximum Low Operating Current in OFF Mode at Room Temperature
- Compatible with 3.3-V and 5-V Logic Control
- Adjustable Current Limit
  - 500 mA to 4 A
  - ±20% Accuracy at 500 mA
- Fault Indication (TPS42S40AQ)
  - Open-Drain Output Status Pin
  - Output Open Load and Short to Battery
  - Output Overload and Short to Ground
  - Over Temperature
- Diagnosis (TPS42S40BQ)
  - Dedicated Current Sense Pin
  - Accurate Current Sense: ±3% at 1 A
- Protection
  - Output Short to Battery Protection
  - Overload and Short to Ground Protection
  - Inductive Load Negative Voltage Protection
  - Loss of Ground, Loss of Supply Protection
  - Over-Temperature Protection
- Package Option
  - ETSSOP14

Applications

- Automotive Off-Board Load Power Supply
- Automotive Body Control, HVAC
- Automotive Infotainment, Navigation, Telematics
- Automotive ADAS, Surround-View Cameras
- Automotive Power Train, Transmission
- Automotive Cluster, Head Unit, HUD
- Industry Control, Factory Automation

Description

The TPS42S40Q is a 100-mΩ single-channel high-side power switch product with AEC-Q100 qualified.

The TPS42S40Q has a wide voltage operating range of 3.5 V to 40 V, with an absolute maximum rating of 45 V. This flexibility makes it suitable for various automotive applications in different conditions.

The TPS42S40Q is equipped with high-precision current sensing capabilities. It offers a current sense accuracy of 3% for loads of 1 A or greater, and 7% for loads of 50 mA or greater. This accurate current sensing enables easy identification of load status and measurement of load current.

The TPS42S40Q integrates full fault detection and device protection to prevent the device damage from open load, overload, over temperature, short-circuit to the battery, short-circuit to ground, reverse battery, loss of ground, loss of power supply and voltage clamp. With all these protection functions, this device is suitable for different resistive, inductive and capacitive loads.

The TPS42S40Q is designed to operate within the ambient temperature range from −40°C to +125°C. Moreover, the TPS42S40Q provides a thermal-enhanced ETSSOP14 package to enable sustained operation despite significant dissipation across the device.

Typical Application Circuit

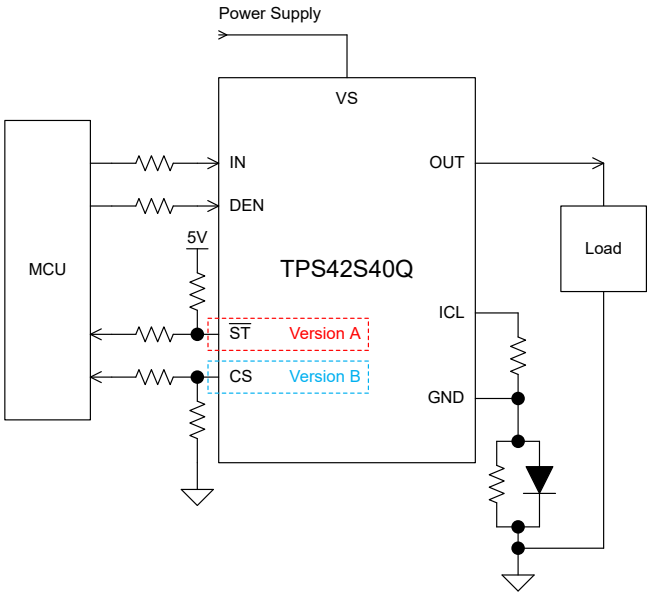


Table of Contents

Product Family Table

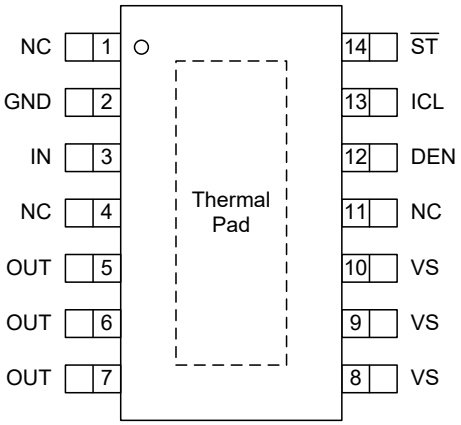
Order Number	Version	Operating Voltage Range (V)	Feature	Package
TPS42S40AQ-TSAR-S	A	4 to 40	Fault Indication	ETSSOP14
TPS42S40BQ-TSAR-S	B	4 to 40	Current Sense	ETSSOP14

Revision History

Date	Revision	Notes
2023-06-25	Rev.Pre.0	Preliminary datasheet.
2024-05-31	Rev.Pre.1	Added detailed description.
2024-08-15	Rev.Pre.2	1. Updated the Electrical Characteristics table. 2. Added the Typical Performance Characteristics.
2024-10-15	Rev.A.0	Initial released.
2024-12-15	Rev.A.1	Corrected the Functional Block Diagram.

Pin Configuration and Functions

TPS42S40AQ
ETSSOP14 Package
Top View



TPS42S40BQ
ETSSOP14 Package
Top View

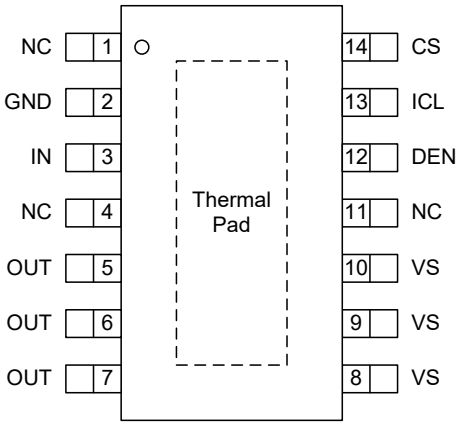


Table 1. Pin Functions: TPS42S40Q

Pin No.	Pin Name		I/O	Description
	TPS42S40AQ	TPS42S40BQ		
14	–	CS	O	Current sense output pin (TPS42S40BQ only). Connect an external resistor to ground to monitor the output current through the internal power MOS. Left this pin open if not used.
12	DEN	DEN	I	Fault-diagnosis function or current-sense function enable pin. Pull this pin HIGH to enable the function or pull this pin LOW to disable the function.
2	GND	GND	–	Ground reference pin.
13	ICL	ICL	O	Current limit adjust pin. Connect an external resistor to ground to set the current limit value. Connect this pin to ground if not used.
3	IN	IN	I	Channel control input pin.
1, 4, 11	NC	NC	–	No internal connection. Suggest connecting to GND to improve the thermal performance.
5, 6, 7	OUT	OUT	O	Channel output pin.
14	$\overline{ST}$	–	O	Status indication pin (TPS42S40AQ only). Open-drain output. Left this pin open if not used.
8, 9, 10	VS	VS	I	Power supply input pin.

(1) Thermal Pad **MUST** be connected to PCB ground plane directly.

Specifications

Absolute Maximum Ratings (1) (2) (3)

Parameter		Min	Max	Unit
Supply Voltage on VS, t < 400 ms (4)			48	V
Reverse Polarity Voltage on VS (5)		−18		V
Continuous Drain Current on OUT		Internal Limited		A
Reverse Current on GND		−50	20	mA
Reverse Current on GND, t < 120 s		−250	20	mA
Voltage on IN and DEN		−0.3	7	V
Current on IN and DEN		−30	2	mA
Voltage on $\overline{ST}$		−0.3	7	V
Current on $\overline{ST}$		−30	10	mA
Input PWM Frequency on IN			2	kHz
Voltage on ICL		−0.3	7	V
Current on ICL		−2	30	mA
Voltage on CS		−2.7	6.5	V
Current on CS		−2	30	mA
T_J	Junction Temperature Range	−40	150	°C
T_A	Ambient Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.
(3) All absolute negative voltage on these terminals is not to go below –0.3 V.
(4) Absolute maximum voltage, withstand 48-V load dump voltage for 400 ms.
(5) Reverse polarity condition: t < 60 s, reverse current < Irev1, GND pin 1-kΩ resistor in parallel with diode.
(6) Not subject to production test, specified by design.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	AEC Q100-002	±4	kV
CDM	Charged Device Model ESD	AEC Q100-011, all pins	±1	kV

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{VS}	Supply Voltage on VS	5	40	V

Parameter		Min	Max	Unit
V_{IN}	Voltage on IN	0	5	V
V_{DEN}	Voltage on DEN	0	5	V
$V_{\overline{ST}}$	Voltage on $\overline{ST}$	0	5	V
I_{OUT}	Nominal DC Load Current	0	4	A
T_A	Ambient Temperature Range	−40	125	°C
T_J	Junction Temperature Range	−40	150	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC,TOP}$	Unit
ETSSOP14	32.95	8.89	31.24	°C/W

Electrical Characteristics

All test conditions: T_A = −40°C to +125°C; typical values at T_A = 25°C, V_{VS} = 5 V to 40 V, over operating free-air temperature range (unless otherwise noted)

Parameter		Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
V_{VS}	Operating Voltage Range		5		40	V
$V_{VS,EXT}$	Extended Operating Voltage Range		3.4		5	V
UVLO	Undervoltage Lockout	VS rising to device turns on	3.4	3.7	4	V
		VS falling to device turns off	3.0	3.2	3.4	V
	Hysteresis			500		mV
I_{VS}	Operating Current	V_{IN} = 5 V, V_{DEN} = 0 V, no load			5	mA
		V_{IN} = 5 V, V_{DEN} = 0 V, 10-Ω load			10	mA
I_{OFF}	Operating Current in OFF Mode	V_{VS} = 13.5 V, V_{IN} = V_{DEN} = V_{CS} = V_{ICL} = V_{OUT} = 0 V, T_A = 25°C			0.5	μA
		V_{VS} = 13.5 V, V_{IN} = V_{DEN} = V_{CS} = V_{ICL} = V_{OUT} = 0 V, T_A = 110°C			5	μA
		V_{VS} = 13.5 V, V_{IN} = V_{DEN} = V_{CS} = V_{ICL} = V_{OUT} = 0 V, T_A = 125°C			12	μA
$I_{OFF,DIAG}$	Operating Current with Diagnostic Enabled in OFF Mode	V_{IN} = 0 V, V_{DEN} = 5 V			2	mA
$t_{OFF,DEG}$ (1)	Off-mode Deglitch Time	IN logic from HIGH to LOW, if waiting time > $t_{OFF,DEG}$, enters standby mode.		2		ms
$I_{OFF,OUT}$	OUT Leakage Current in OFF Mode	V_{VS} = 13.5 V, V_{IN} = V_{OUT} = 0, T_A = 25°C			0.5	μA
		V_{VS} = 13.5 V, V_{IN} = V_{OUT} = 0, T_A = 110°C			5	μA
		V_{VS} = 13.5 V, V_{IN} = V_{OUT} = 0, T_A = 125°C			12	μA
Logic Control (IN and DEN)						
V_{IH}	Logic Input High-level Voltage		2			V
V_{IL}	Logic Input Low-level Voltage				0.8	V
V_{HYS}	Hysteresis Voltage			250		mV
R_{PD}	IN Pulldown Resistor			500		kΩ
	DEN Pulldown Resistor			150		kΩ
Output Power Stage						
R_{ON}	Turn-on Resistance	V_{VS} > 5 V, T_A = 25°C		80	100	mΩ
		V_{VS} > 5 V, T_A = 150°C			166	mΩ

Parameter		Conditions	Min	Typ	Max	Unit
		V_{VS} = 3.5 V, T_A = 25°C			120	mΩ
I_{LIM}	Inherent Current Limit		7		13	A
	Current Limit during Over-Temperature Protection	Inherent current limit under thermal cycling conditions		5		A
		Inherent current limit under thermal cycling conditions. Percentage of current limit set value		50%		
V_{DS}	Drain-to-Source Internally Clamped Voltage		48		70	V
V_F	Drain-to-Source Diode Voltage	V_{IN} = 0, I_{OUT} = −0.2 A		0.7		V
I_{REV} (2)	Reverse Current	Reverse polarity from VS to GND. t < 60 s, V_{VS} = 13.5 V, GND pin 1-kΩ resistor in parallel with diode. T_A = 25°C.		4		A
		Reverse voltage from OUT to VS. t < 60 s, V_{VS} = 13.5 V. T_A = 25°C.		2		A
$t_{D,ON}$ (1)	Turn-On Delay Time	IN rising edge to V_{OUT} = 10%, DEN = HIGH	20		50	µs
$t_{D,OFF}$ (1)	Turn-Off Delay Time	IN falling edge to V_{OUT} = 90%, DEN = HIGH	20		50	µs
dV/dt_{ON} (1)	Turn-On Slew Rate	V_{OUT} = 10% to 90%, DEN = HIGH	0.1		0.5	V/µs
dV/dt_{OFF} (1)	Turn-Off Slew Rate	V_{OUT} = 90% to 10%, DEN = HIGH	0.1		0.5	V/µs
ΔdV/dt (1)	Turn On/Off Slew Rate Matching		−0.15		0.15	V/µs
Fault Detection and Diagnosis						
$I_{LG,OUT}$	OUT Leakage Current of Loss-of-Ground Condition				100	µA
$V_{OL,OFF}$	Open-Load Detection Threshold in OFF Mode	V_{IN} = 0 V, when $V_{VS} - V_{OUT} < V_{OL,OFF}$ and duration longer than $t_{OL,OFF}$, open load fault detected.	1.4	2	2.6	V
$I_{OL,OFF}$	Open-Load Current Sink in OFF Mode	V_{IN} = 0 V, V_{VS} = V_{OUT} = 13.5 V, T_A = 125°C.			-50	µA
$t_{OL,OFF}$	Open-Load Detection Deglitch Time in OFF Mode	V_{IN} = 0 V, When $V_{VS} - V_{OUT} < V_{OL,OFF}$ and duration longer than $t_{OL,OFF}$, open load fault detected.		600		µs
$I_{OL,ON}$	Open-Load Detection Threshold in ON Mode	V_{IN} = 5 V, when $I_{OUT} < I_{OL,ON}$ and duration longer than $t_{OL,ON}$, open load detected. (Version A only)	2	6	10	mA

Parameter		Conditions	Min	Typ	Max	Unit
$t_{OL,ON}$	Open-Load Detection Deglitch Time in ON Mode	V_{IN} = 5 V, when I_{OUT} < $I_{OL,ON}$ and duration longer than $t_{OL,ON}$, open load detected. (Version A only)		700		µs
$V_{\overline{ST}}$	Output Voltage when $\overline{ST}$ = LOW	$I_{\overline{ST}}$ = 2 mA. (Version A only)			0.4	V
T_{SD}	Thermal Shutdown Threshold			175		°C
$T_{SD,RST}$	Thermal Shutdown Status Reset			155		°C
T_{SW}	Thermal Swing Shutdown Threshold			60		°C
T_{HYS}	Hysteresis for Resetting the Thermal Shutdown and Thermal Swing			10		°C
Current Sense						
K_{CS}	Current Sense Ratio			500		
K_{CL}	Current Limit Ratio			2000		
ΔCS	Current Sense Accuracy	I_{OUT} ≥ 5 mA	–80		80	%
		I_{OUT} ≥ 25 mA	–10		10	%
		I_{OUT} ≥ 50 mA	–7		7	%
		I_{OUT} ≥ 0.1 A	–5		5	%
		I_{OUT} ≥ 1 A	–3		3	%
ΔK_{CL} (3) (4)	Current Limit Accuracy	I_{LIMIT} ≥ 0.5 A	–20		20	%
		I_{LIMIT} ≥ 1.6 A	–14		14	%
V_{CS}	Current Sense Voltage Range	V_{VS} ≥ 5 V	0		4	V
$I_{CS,OFF}$	Current Sense Leakage Current in OFF Mode	V_{IN} = 5 V, R_{LOAD} = 10 Ω, V_{DEN} = 0 V, T_A = 125°C			1	µA
		V_{IN} = 0 V, V_{DEN} = 0 V, T_A = 125°C			1	µA
I_{OUT}	Output Current Range	V_{VS} ≥ 5 V, V_{CS} ≤ 4 V	0		4	A
$V_{CS,H}$	Current-Sense Fault High Voltage	V_{VS} ≥ 7 V	4.3	4.75	5	V
		V_{VS} ≥ 5 V	Min (V_{VS} – 0.8, 4.3)		5	V
$I_{CS,H}$	Current-Sense Fault Condition Current	V_{CS} = 4.3 V, V_{VS} > 7 V	9			mA
$V_{CL,TH}$	Current-Limit Internal Threshold Voltage			1.233		V
$t_{CS,OFF}$ (1)	CS Settling Time from DEN Disabled	V_{IN} = 5 V, I_{OUT} ≥ 5 mA. V_{DEN} from 5 to 0 V. CS to 10% of sense value.			10	µs

Parameter		Conditions	Min	Typ	Max	Unit
	CS Settling Time from IN Falling Edge	V_{DEN} = 5 V, I_{OUT} ≥ 5 mA. IN from 5 to 0 V. CS to 10% of sense value.			10	μs
		V_{DEN} = 5 V, I_{OUT} ≥ 5 mA. IN from 5 to 0 V. Current limit triggered.			180	μs
$t_{CS,ON}$ (1)	CS settling time from DEN enabled	V_{IN} = 5 V, I_{OUT} ≥ 5 mA. V_{DEN} from 0 to 5 V. CS to 90% of sense value.			10	μs
	CS settling time from IN rising edge	V_{VS} = 13.5 V, V_{DEN} = 5 V, I_{OUT} ≥ 100 mA. V_{IN} from 0 to 5 V. CS to 90% of sense value.			150	μs

(1) Not subject to production test, specified by design.
(2) Measured on bench with 10 pcs/3 lots samples.
(3) The accuracy of the external current limit is only applicable when the over-current conditions are more than 1.5 times the current-limit setting.
(4) Recommended Minimum current-limit setting value is 500 mA.

Typical Performance Characteristics

All test conditions: V_S = 13.5 V, unless otherwise noted.

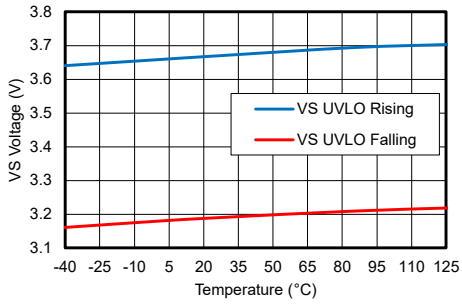


Figure 1. VS Supply Voltage UVLO

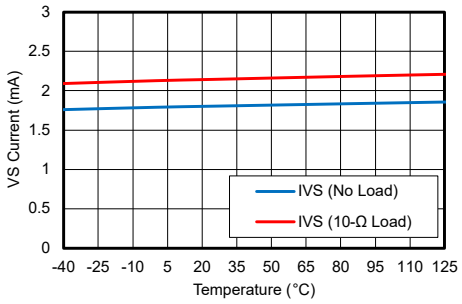


Figure 2. VS Operating Current

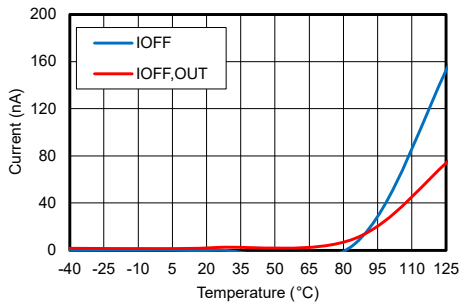


Figure 3. Operating Current and OUT Leakage Current in OFF Mode

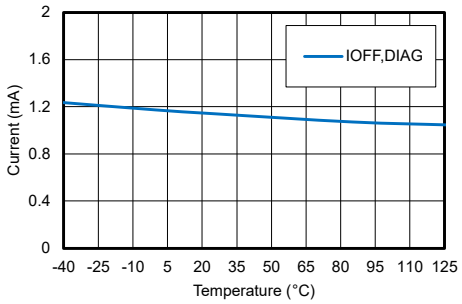


Figure 4. Operating Current with DEN High in OFF Mode

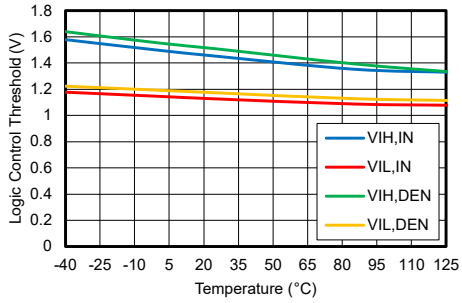


Figure 5. Logic Control Voltage

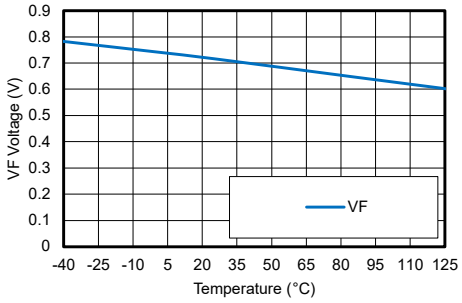


Figure 6. VF Voltage

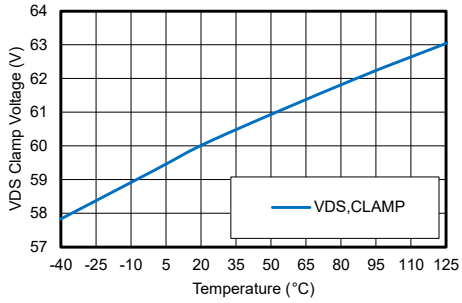


Figure 7. VDS Clamp Voltage

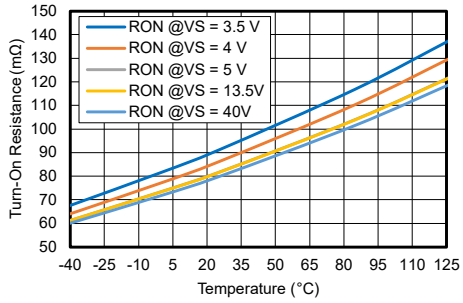


Figure 8. Turn-On Resistance

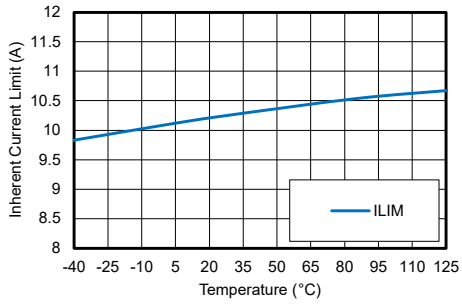


Figure 9. Inherent Current Limit

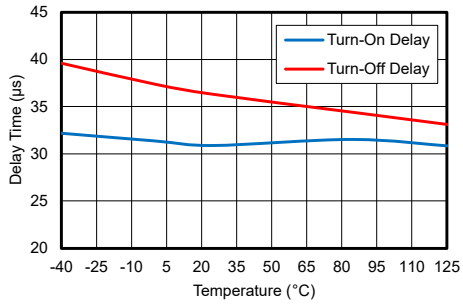


Figure 10. Turn-On and Turn-Off Delay Time

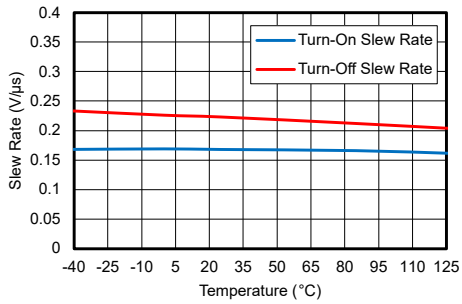


Figure 11. Turn-On and Turn-Off Slew Rate

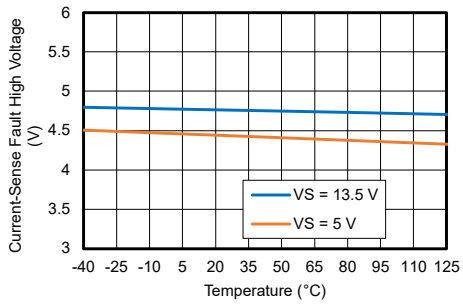


Figure 12. Current Sense Fault High Voltage

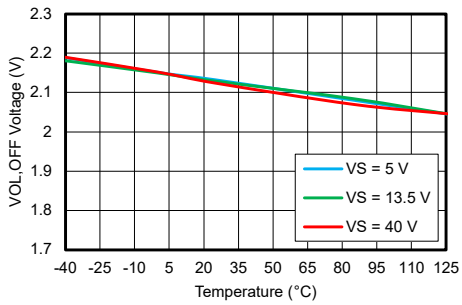


Figure 13. Open-Load Detection Voltage Threshold in OFF Mode

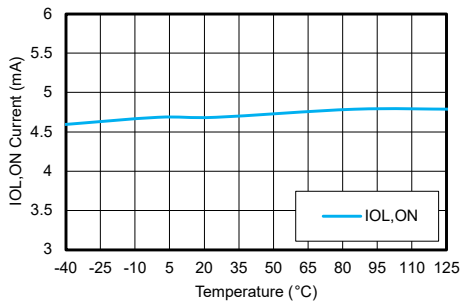
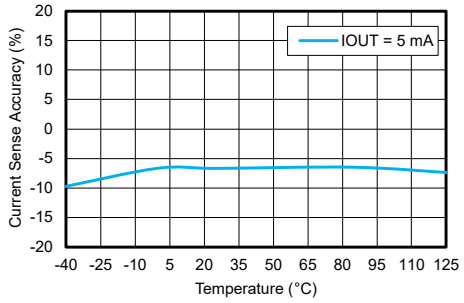
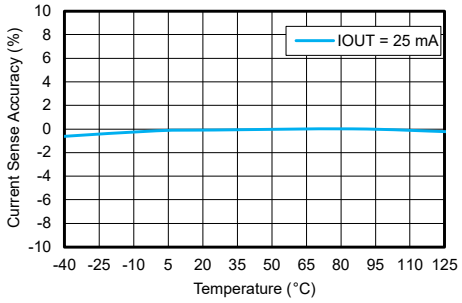


Figure 14. Open-Load Detection Current Threshold in ON Mode



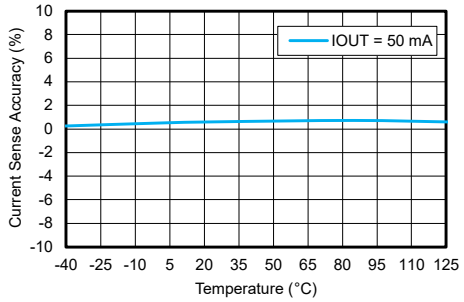
I_{OUT} = 5 mA

Figure 15. Current Sense Accuracy



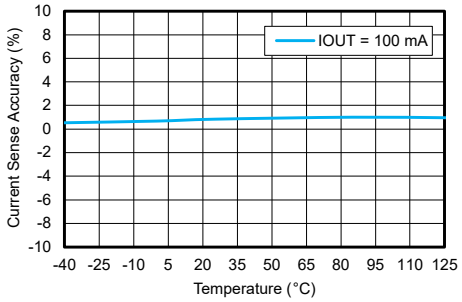
I_{OUT} = 25 mA

Figure 16. Current Sense Accuracy



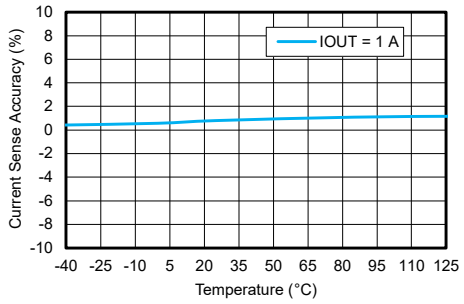
I_{OUT} = 50 mA

Figure 17. Current Sense Accuracy



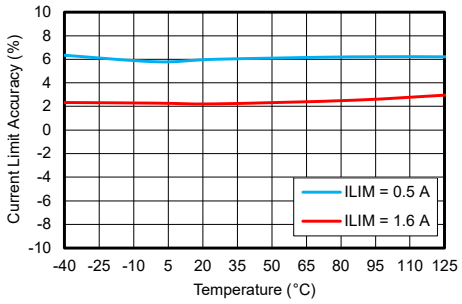
I_{OUT} = 100 mA

Figure 18. Current Sense Accuracy



I_{OUT} = 1 A

Figure 19. Current Sense Accuracy



V_S = 13.5 V

Figure 20. Current Limit Accuracy

Detailed Description

Overview

The TPS42S40Q is a 100-mΩ single-channel high-side power switch product with AEC-Q100 qualified.

The TPS42S40Q has a wide voltage operating range of 3.5 V to 40 V, with an absolute maximum rating of 45 V. This flexibility makes it suitable for various automotive applications in different conditions.

The TPS42S40Q is equipped with high-precision current sensing capabilities. It offers a current sense accuracy of 3% for loads of 1 A or greater, and 7% for loads of 50 mA or greater. This accurate current sensing enables easy identification of load status and measurement of load current.

The TPS42S40Q integrates full fault detection and device protection to prevent the device damage from open load, overload, over temperature, short-circuit to battery, short-circuit to the ground, reverse battery, loss of ground, loss of power supply and voltage clamp. With all these protection functions, this device is suitable for different resistive, inductive and capacitive loads.

Functional Block Diagram

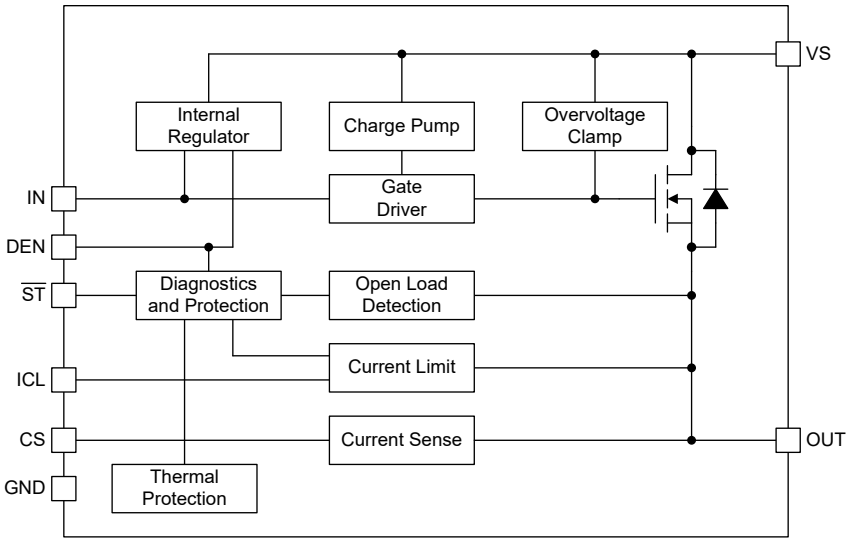


Figure 21. Functional Block Diagram

Feature Description

Under-Voltage Lockout (UVLO)

The TPS42S40Q uses the VS UVLO control to keep the output off until the internal circuitry operates properly. When the VS voltage is lower than the UVLO falling threshold, the TPS42S40Q stays in the shutdown mode. When the VS voltage is greater than the UVLO rising threshold, the device enters operation mode.

Channel Control (IN)

The TPS42S40Q integrates an IN pin for the channel control. The IN pin is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to turn on and off the internal power MOSFET.

Status Indication ($\overline{ST}$)

For the TPS42S40AQ, an $\overline{ST}$ pin is integrated to indicate the device output status.$\overline{ST}$ is an open-drain output pin and an external pull-up resistor is required.

When the fault diagnostic control pin is low (DEN = L), the $\overline{ST}$ pin is internally high impedance, and it is pulled up high. When DEN = H, the $_{ST}$ pin voltage changes according to the output status.

Current Sense (CS)

For the TPS42S40BQ, a CS pin is integrated to sense the output current and diagnostic fault conditions.

When the fault diagnostic control pin is low (DEN = L), the CS pin is internally high impedance. When DEN = H, a current mirror is internally implemented to source a current of I_{OUT}/K_{CS}, which is directed outward to the external resistor connected between the CS pin and the ground, and a voltage is formed on the CS pin. It is suggested to keep the CS voltage in the range of 0 to 4 V during normal operation. Use Equation 1 to calculate the external current sense resistor, R_{CS}.

$$R_{CS} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{CS}}{I_{OUT}} \quad (1)$$

where, K_{CS} is the ratio of the output current to the sensed current. It is a constant value regardless of temperature and supply voltage variations.

When fault conditions occur, the CS pin works as a fault indication pin. In the on state, the V_{CS} voltage is almost 0 while operating in the condition of an open-load or short-t-battery fault. In the OFF state, the V_{CS} voltage is internally pulled-up to $V_{CS,H}$ while operating in the condition of a current-limit, thermal-shutdown, thermal-swing, open-load, or short-to-battery fault. Refer to Diagnostics and Fault Protections for more details.

Adjustable Current Limit (ICL)

The TPS42S40Q integrates an accurate current limit function, and it is adjustable with the external resistor R_{ICL}. When the overload or short-to-ground condition occurs, the current limit function will limit the maximum current through the power FET at the set value and pull up the CS pin voltage to V_{CS} internally.

There are two current-limit thresholds: the internal current limit and the external adjustable current limit.

While the ICL pin is connected to ground directly, the internal current limitation is used. The internal current limit is set to a fixed value of 10 A typically.

While an external resistor is connected at the ICL pin, it transforms a proportional load current into a voltage signal, which is compared with the internal reference voltage, $V_{CL,TH}$. When V_{ICL} exceeds $V_{CL,TH}$, a closed feedback loop is immediately activated, and the current is clamped at the set value. When a ground network is used, the R_{ICL} must be connected to the device GND directly. Use Equation 3 to calculate the R_{ICL}.

$$I_{LIM} = \frac{V_{CL,TH}}{R_{ICL}} = \frac{I_{OUT}}{K_{CL}} \quad (2)$$

$$R_{ICL} = \frac{V_{CL,TH} \times K_{CL}}{I_{OUT}} \quad (3)$$

After the VS is powered up and IN is high, both the internal current limit and the external current limit are active, and the lower one is utilized as the effective current limit.

To provide enhanced protection against a hard short-to-ground condition, an open-loop fast-response mechanism is set to turn off the channel before the current-limit closed loop is established. The open-loop response time is approximately 1 µs.

Inductive Load Switching-Off Clamp

When an inductive load of the TPS42S40Q is turned off, the output voltage is drawn down to a negative level due to the inductance characteristics. The internal power MOSFET could be damaged if the drain-to-source voltage (V_{DS}) is not clamped during the current decay period. In this condition, the $V_{DS,CLAMP}$ voltage is necessary to limit the voltage across

the drain and source, and thus prevent the device from damage. During the current-decay period, the TPS42S40Q turns on the internal power MOSFET to release the energy stored in the inductance. Both the energy from the power supply and the energy from the inductive load are dissipated by the high-side power switch. If there is any resistance in series with the inductance, part of the energy will be also dissipated through this resistance. For PWM-controlled inductive loads, it is recommended to add an external freewheeling diode to protect the device from repetitive power stress.

Diagnosis Enable Function (DEN)

The TPS42S40Q uses the DEN pin to control whether the device diagnostic function is active or not. When multiple TPS42S40Q chips share the same ADC or I/O channel, the multiplexing function can be achieved by the DEN control. Additionally, pulling down the DEN pin can significantly reduce the TPS42S40Q's total power consumption to below 500nA.

Table 2. DEN Logic Table

DEN	IN Pin	Protections and Diagnostics
H	H	See Table 3.
	L	See Table 3.
L	H	Diagnostics is disabled, and protection is normal. CS or $\overline{ST}$ is high impedance.
	L	Diagnostics is disabled, and no protections. CS or $\overline{ST}$ is high impedance

Diagnostics and Fault Protections

When DEN is high, status indication ($\overline{ST}$) or current sense (CS) is enabled. When DEN is low, status indication ($\overline{ST}$) or current sense (CS) is disabled, and the output of $\overline{ST}$ or CS is in high-impedance mode.

Table 3. Fault Table

Condition	IN	OUT	Criterion	$\overline{ST}$ (Version A)	CS (Version B)	Diagnostics Recovery
Normal	L	L		H	0	
	H	H		H	Linear	
Short to Ground	H	L	Current limit.	L	$V_{CS,H}$	Auto
Open Load (1) Short to Battery Reverse Polarity	H	H	A: Output current < $I_{OL,ON}$. B: Judged by users.	L (deglitch)	Almost 0	Auto
	L	H	$V_{VS} - V_{OUT} < V_{OL,OFF}$.	L (deglitch)	$V_{CS,H}$ (deglitch)	Auto
Over Temperature	H		Thermal shutdown.	L	$V_{CS,H}$	
	H		Thermal swing.	L	$V_{CS,H}$	Auto

(1) Need external pullup resistor during off-state

Overload and Short to Ground Fault

When IN is high and the output channel is switched on, the over-load or short-to-ground condition will trigger the device current limitation. In this condition, the output current is limited to the set value, and the $\overline{ST}$ is pulled low or CS is pulled to $V_{CS,H}$. The current limit and the $\overline{ST}$ or CS will be recovered automatically when the fault is removed. The long-time current limit will cause the thermal shutdown to prevent the device from damage.

Open Load Fault

When IN is high and the output channel is switched on, there will be an output current supplied to the load.

- The TPS42S40AQ will report an open-load fault by pulling the $\overline{ST}$ pin low (when the output current is less than $I_{OL,ON}$).
- The TPS42S40BQ will diagnose the fault by reading the V_{CS} voltage. With the accurate current sense, the TPS42S40BQ can support a very low open-load detection threshold. It is recommended to set 10 mA as the upper limit for the open-load detection threshold and 25 mA as the lower limit for the normal operation current.

When IN is low and the output channel is switched off, the output voltage will be pulled down to 0 V with a connected load and will remain close to the supply voltage with an open load ($V_{VS} – V_{OUT} < V_{OL,OFF}$).

- The TPS42S40AQ will report an open-load fault by pulling the $\overline{ST}$ pin low.
- The TPS42S40BQ will pull the CS pin voltage up to $V_{CS,H}$. It is recommended to use an external pull-up resistor at the OUT pin to eliminate the influence of the leakage current, $I_{OL,OFF}$. The pull-up current should not be greater than the load current to prevent false triggering during normal operation. It is recommended to use a switch in series with the pull-up resistor to reduce the standby current and use the pull-up resistor R_{PU} less than 15 kΩ.

Short-to-Battery Fault

The TPS42S40Q integrates the short-to-battery fault detection, which has the same operating mechanism and behavior as the open-load detection.

In the ON state with IN high, the reverse current, caused by the short-to-battery fault, flows the internal MOSFET and leads to small power dissipation on the device.

In the OFF state with IN low, the short-to-battery fault is reported when V_{OUT} is greater than V_{VS}, but the reverse current is determined by the voltage difference between V_{OUT} and V_{VS}. When $V_{OUT} − V_{VS} < V_F$, there is no reverse current. When $V_{OUT} − V_{VS} > V_F$, reverse current occurs. Please note, that the reverse current should be less than I_{REV2} to prevent the device from damage.

Reverse-Polarity Fault

The TPS42S40Q integrates the reverse-polarity fault detection, which has the same operating mechanism and behavior as the open-load detection.

In the ON state with IN high, the reverse current, caused by the reverse polarity, flows the internal MOSFET and leads to small power dissipation on the device.

In the OFF state with IN low, the reverse polarity is reported and the reverse current flows through the body diode will cause high power dissipation. Please note, that the reverse current should be less than I_{REV1} to prevent the device from damage.

Reverse-Current Protection

Either the short-to-battery fault or the reverse-polarity fault will cause the reverse current to flow through the device. Usually, there are two methods to block the reverse current.

1. Add a block diode between the power supply and the VS pin. With this method, both the device and load are protected from the reverse current fault.
2. Add a ground network between the GND pin and the system ground. It is recommended to use an I_F > 100mA diode and a 1-kΩ resistor in parallel in the ground network. With this method, only the TPS42S40Q device is protected from the reverse current fault, and the load is protected by itself.

Please note, that when the ground network is used, the R_{ICL} must be connected to the device GND pin directly.

Loss-of-Ground Protection

The TPS42S40Q turns off the output when the loss-of-ground fault occurs, no matter whether the IN-pin signal is high or low.

Loss-of-Power Supply Protection

The TPS42S40Q turns off the output when the loss-of-power fault occurs, no matter whether the IN-pin signal is high or low. When a loss-of-power fault occurs, the inductive load will still sink current from all pins connected. It is recommended to use the ground network or a freewheeling diode to prevent damage from negative voltage.

Over-Temperature Fault and Protection

The TPS42S40Q integrates two mechanisms for over-temperature diagnosis and protection: thermal shutdown and thermal swing.

When the junction temperature T_J rises above the thermal shutdown threshold T_{SD}, thermal shutdown works and turns off the output immediately. When the device cools down and the junction temperature falls below $T_{SD} - T_{HYS}$, the output turns on again. In the thermal shutdown condition, the $\overline{ST}$ pin of TPS42S40AQ is pulled down and the CS pin of TPS42S40BQ is pulled up to $V_{CS,H}$, and the current limit is reduced to $I_{LIM,STD}$ or half of the set value to prevent the device repeating thermal shutdown. The thermal shutdown fault signal and the reduced current limit will not be reset until the junction temperature decreases below $T_{SD,RST}$.

When the MOSFET junction temperature T_{MOS} rises much more quickly than the logic control module junction temperature T_{LOGIC} and the temperature difference $\Delta T = T_{MOS} – T_{LOGIC} > T_{SW}$, the thermal swing works and turns off the output immediately. When the MOSFET cools down and the temperature difference $\Delta T = T_{MOS} – T_{LOGIC} < T_{SW}T_{HYS}$, the output turns on again. In the thermal swing condition, the $\overline{ST}$ pin of TPS42S40AQ is pulled down and the CS pin of TPS42S40BQ is pulled up to $V_{CS,H}$. The thermal swing fault signal automatically reset after the device recovered from the thermal swing condition.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPS42S40Q is a 100-mΩ single-channel high-side power switch product with AEC-Q100 qualified. The following application schematic shows a typical usage of the TPS42S40Q series.

Typical Application

Figure 22 shows the typical protection application schematic of the TPS42S40Q.

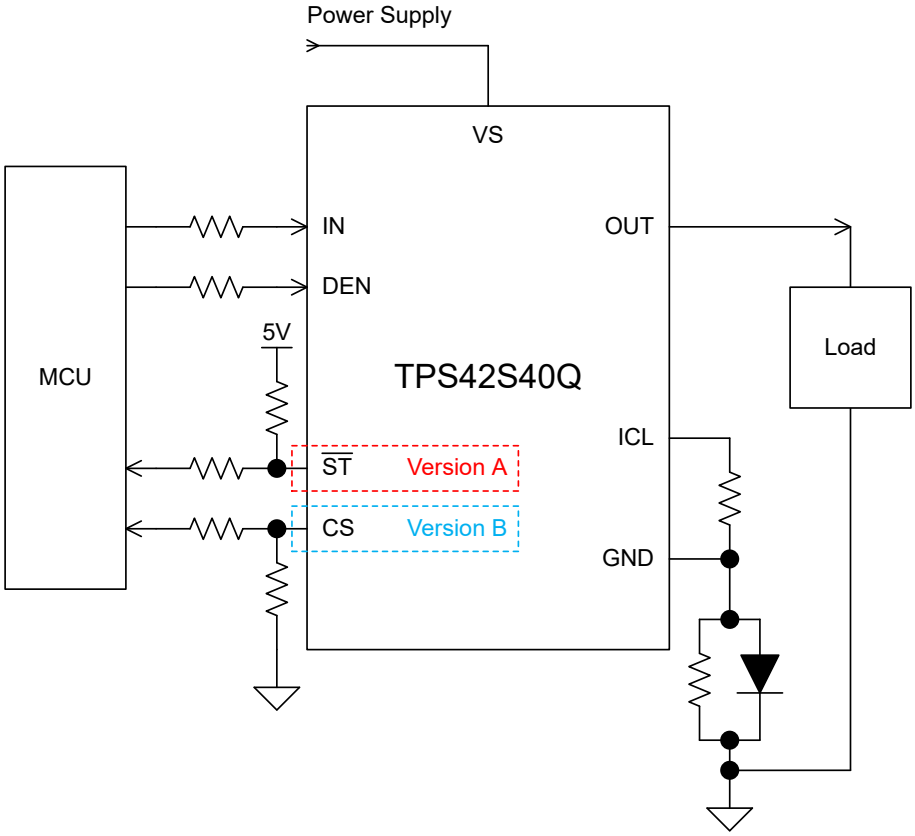


Figure 22. Typical Application Circuit

Power Dissipation

During normal operation, the junction temperature should meet the requirement in the Recommended Operating Conditions table. Use Equation 4 and Equation 5 to calculate the power dissipation and estimate the junction temperature.

The power dissipation (P_D) can be calculated using Equation 4.

$$P_D = I_{OUT}^2 \times R_{ON} + V_S \times I_Q \quad (4)$$

Where,

- I_{OUT} is the output current,
- R_{ON} is the turn-on resistance,
- V_S is the VS pin power supply voltage,
- I_Q is the quiescent current.

The junction temperature (T_J) can be estimated using Equation 5.

$$T_J = T_A + P_D \times \theta_{JA} \quad (5)$$

Where,

- T_A is the ambient temperature,
- P_D is the power dissipation,
- θ_{JA} is the junction-to-ambient thermal resistance.

Layout

Layout Guideline

To get good thermal performance and prevent over-temperature protection, the PCB layout is important. A well-designed PCB layout can effectively optimize heat dissipation, which is crucial for ensuring the long-term reliability of the device.

- It is recommended to maximize the coverage of copper on the PCB to enhance the thermal conductivity of the board. Since the primary heat flow path from the package to the surrounding environment passes through the copper on the PCB, having maximum copper coverage is particularly important when there is no heat sink attached to the opposite side of the board.
- It is recommended to place as many thermal vias as possible underneath the package ground pad to optimize the thermal conductivity of the board.
- It is suggested that all thermal vias be either plated shut or plugged and capped on both sides of the board to prevent solder voids to maintain reliability and performance.
- It is recommended to use wide traces or thick copper weight in the input/output current paths to minimize I×R voltage drop.

Layout Example

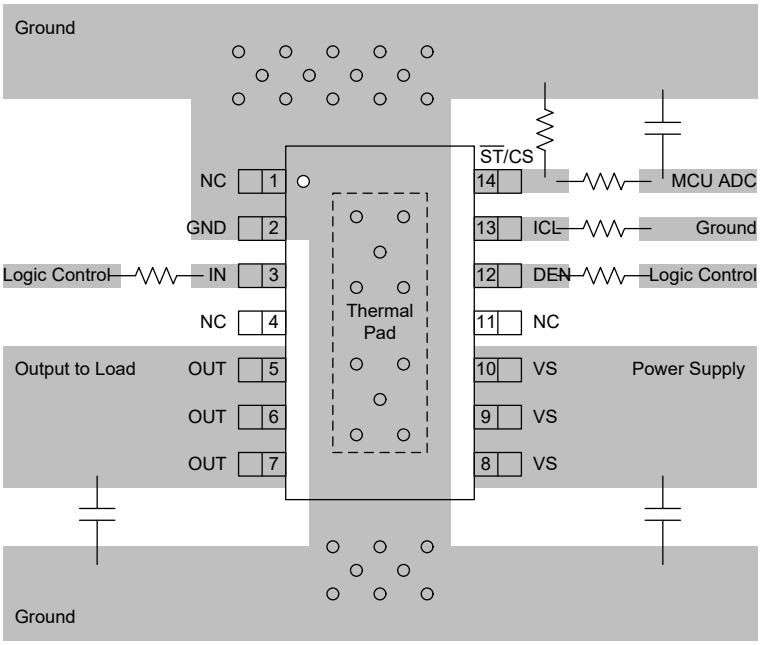


Figure 23. Layout Example

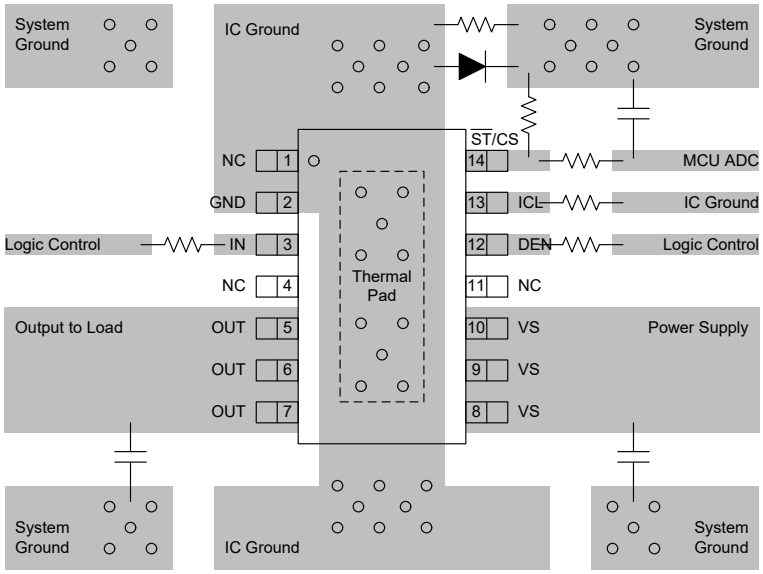
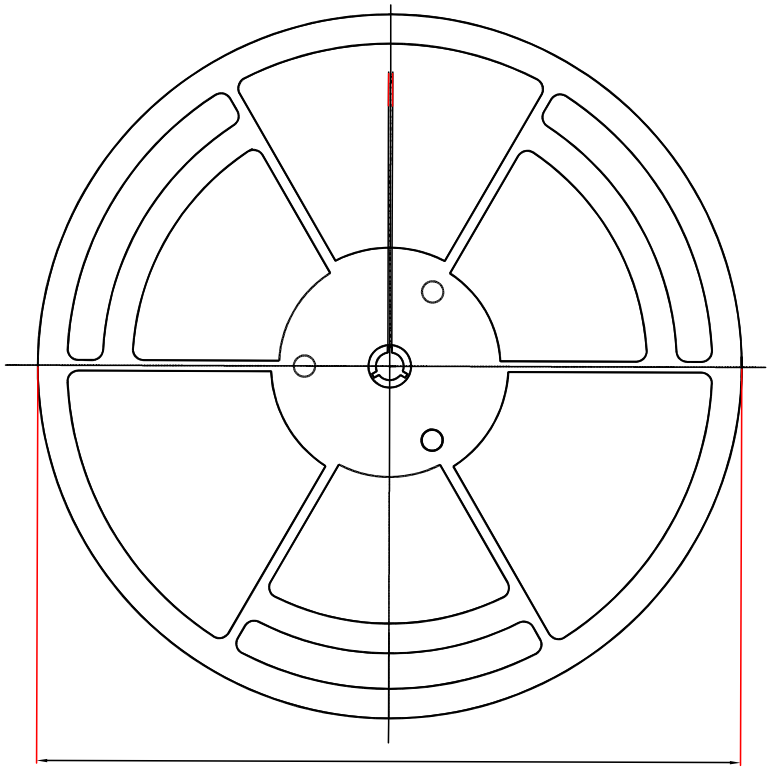
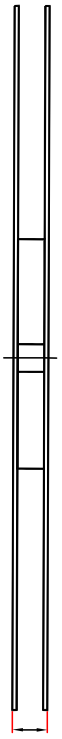
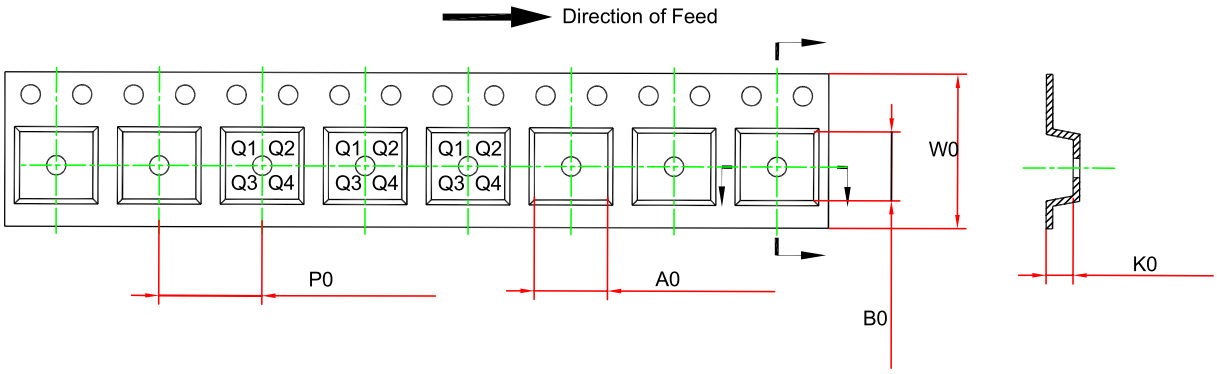


Figure 24. Layout Example with a Ground Network

Tape and Reel Information





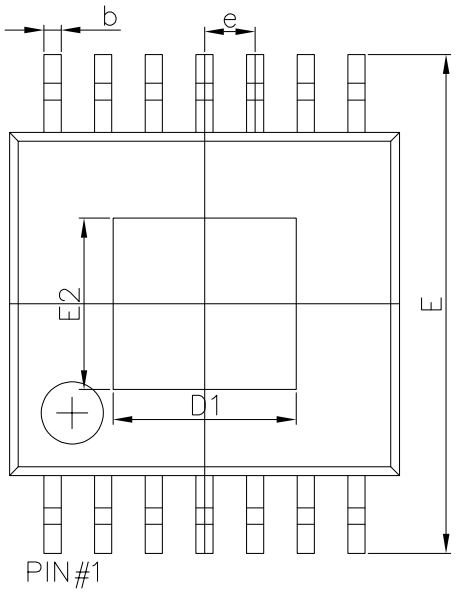


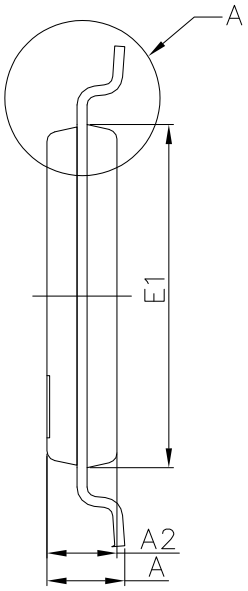
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPS42S40AQ-TSAR-S	ETSSOP-14	330	17.6	6.8	5.4	1.3	8	12	Q1
TPS42S40BQ-TSAR-S	ETSSOP-14	330	17.6	6.8	5.4	1.5	8	12	Q1

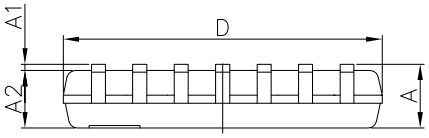
Package Outline Dimensions

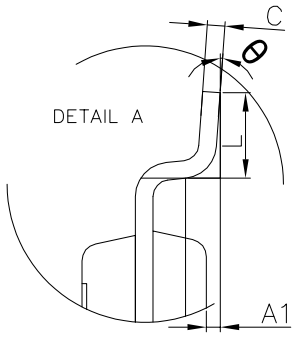
ETSSOP14

Package Outline Dimensions TSA(ETSSOP-14-A)









NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	---	1.200	---	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
D1	2.250	2.450	0.089	0.096
E	6.250	6.550	0.246	0.258
E1	4.300	4.500	0.169	0.177
E2	2.100	2.300	0.083	0.091
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPS42S40AQ-TSAR-S	−40 to 150°C	ETSSOP14	SS40A	MSL3	3,000	Green
TPS42S40BQ-TSAR-S	−40 to 150°C	ETSSOP14	SS40B	MSL3	3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

Trademarks. Any of the 思瑞浦 or 3PEAK trade names, trademarks, graphic marks, and domain names contained in this document /material are the property of 3PEAK. You may NOT reproduce, modify, publish, transmit or distribute any Trademark without the prior written consent of 3PEAK.

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

Disclaimer. 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.