

### **Features**

- Qualified for Automotive Applications
  - AEC-Q100 Grade 1, T<sub>A</sub>: -40°C to +125°C
- Wide Input Voltage Range
  - 4 V to 40 V, with 45 V Maximum Rating
- 160-mΩ Maximum Low Turn-On Resistance at Room Temperature
- · 4 Independent Input and Output Channels
- 0.5-µA Maximum Low Operating Current in OFF Mode at Room Temperature
- Compatible with 3.3-V and 5-V Logic Control
- · Adjustable Current Limit
  - 500 mA to 2.5 A for Each Channel
  - ±20% Accuracy at 500 mA
- Fault Indication (TPS42Q20AQ)
  - Open-Drain Output Status Pin
  - Output Open Load and Short to Battery
  - Output Overload and Short to Ground
  - Over Temperature
- Diagnosis (TPS42Q20BQ)
  - Dedicated Current Sense Pin
  - Accurate Current Sense: ±3% at 500 mA
- Protection
  - Output Short to Battery Protection
  - Overload and Short to Ground Protection
  - Inductive Load Negative Voltage Protection
  - Loss of Ground, Loss of Supply Protection
  - Over-Temperature Protection
- Package Option
  - ETSSOP28

### **Applications**

- Automotive Off-Board Load Power Supply
- Automotive Body Control, HVAC
- · Automotive Infotainment, Navigation, Telematics
- · Automotive ADAS, Surround-View Cameras
- Automotive Power Train, Transmission
- · Automotive LED Lighting
- Automotive Cluster, Head Unit, HUD
- Industry Control, Factory Automation

### **Description**

The TPS42Q20Q is a 160-m $\Omega$  4-channel high-side power switch product with AEC-Q100 qualified.

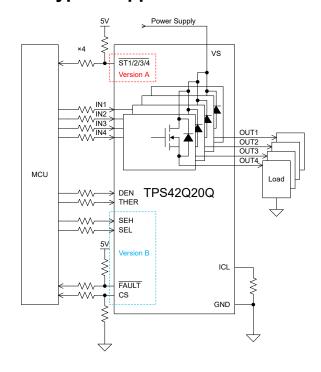
The TPS42Q20Q has a wide voltage operating range of 3.5 V to 40 V, with an absolute maximum rating of 45 V. This flexibility makes it suitable for various automotive applications in different conditions.

The TPS42Q20Q is equipped with high-precision current sensing capabilities. It offers a current sense accuracy of 3% for the loads of 500 mA or greater, and 8% for the loads of 50 mA or greater. This accurate current sensing enables easy identification of load status and measurement of load current.

The TPS42Q20Q integrates full fault detection and device protection to prevent the device damage from open load, overload, over temperature, short-circuit to the battery, short-circuit to ground, reverse battery, loss of ground, loss of power supply and voltage clamp. With all these protection functions, this device is suitable for different resistive, inductive and capacitive loads.

The TPS42Q20Q is designed to operate within the ambient temperature range from -40°C to +125°C. Moreover, the TPS42Q20Q provides a thermal-enhanced ETSSOP28 package to enable sustained operation despite significant dissipation across the device.

## **Typical Application Circuit**





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## **Product Family Table**

Order Number Operating Voltage Range (V)		Feature	Package
TPS42Q20AQ-TSCR-S	4 to 40	Fault Indication	ETSSOP28
TPS42Q20BQ-TSCR-S	4 to 40	Current Sense	ETSSOP28

## **Revision History**

Date	Revision	Notes
2024-02-25	Rev.Pre.0	Preliminary datasheet.

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## **Pin Configuration and Functions**

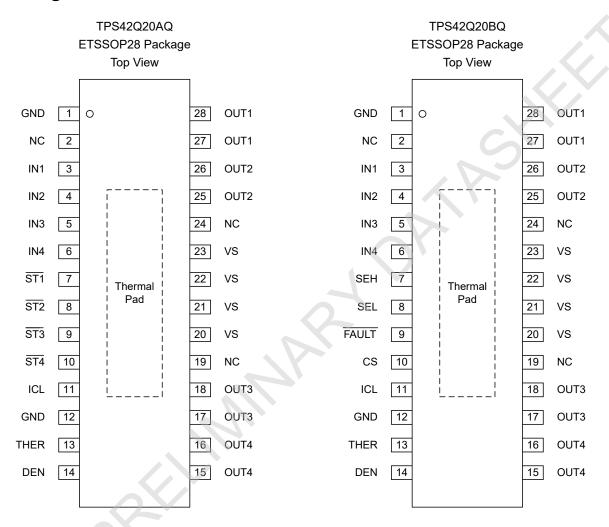


Table 1. Pin Functions: TPS42Q20Q

	Pin N	Name		
Pin No.	TPS42Q20 AQ	TPS42Q20 BQ	I/O	Description
10	-	cs	0	Current sense output pin (TPS42Q20BQ only). Connect an external resistor to ground to monitor the output current through the internal power MOS. Left this pin open if not used.
14	DEN	DEN	I	Fault-diagnosis function or current-sense function enable pin. Pull this pin HIGH to enable the function or pull this pin LOW to disable the function.
9	_	FAULT	0	Device fault indication pin (TPS42Q20BQ only). Open-drain output. Left this pin open if not used.
1, 12	GND	GND	_	Ground reference pin.

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	Pin N	lame		
Pin No.	TPS42Q20 AQ	TPS42Q20 BQ	I/O	Description
11	ICL	ICL	0	Current limit adjust pin. Connect an external resistor to ground to set the current limit value. Connect this pin to ground if not used.
3	IN1	IN1	I	Channel 1 control input pin.
4	IN2	IN2	I	Channel 2 control input pin.
5	IN3	IN3	I	Channel 3 control input pin.
6	IN4	IN4	I	Channel 4 control input pin.
2, 19, 24	NC	NC	_	No internal connection. Suggest connecting to GND to improve the thermal performance.
27, 28	OUT1	OUT1	0	Channel 1 output pin.
25, 26	OUT2	OUT2	0	Channel 2 output pin.
17, 18	OUT3	OUT3	0	Channel 3 output pin.
15, 16	OUT4	OUT4	0	Channel 4 output pin.
7	ST1	_	0	Channel 1 statues indication pin (TPS42Q20AQ only). Open-drain output. Left this pin open if not used.
8	ST2	_	0	Channel 2 statues indication pin (TPS42Q20AQ only). Open-drain output. Left this pin open if not used.
9	ST3	_	0	Channel 3 statues indication pin (TPS42Q20AQ only). Open-drain output. Left this pin open if not used.
10	ST4	-	0	Channel 4 statues indication pin (TPS42Q20AQ only). Open-drain output. Left this pin open if not used.
7	_	SEH	1	Current sense channel selection high bit (TPS42Q20BQ only) .
8	_	SEL	I	Current sense channel selection low bit (TPS42Q20BQ only) .
13	THER	THER	I	Thermal shutdown behavior control pin. Pull this pin low for auto retry or pull this pin high for latch off when thermal shutdown protection is triggered.
20, 21, 22,	VS	VS	I	Power supply input pin.

<sup>(1)</sup> Thermal Pad  ${f MUST}$  be connected to device GND directly.

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### **Specifications**

### Absolute Maximum Ratings (1) (2) (3)

Parameter	Min	Max	Unit
Supply Voltage on VS pin, t < 400 ms <sup>(4)</sup>		48	V
Reverse Polarity Voltage on VS pin <sup>(5)</sup>	-36		V
Continuous Drain Current on OUT pin	Internal	Limited	Α
Reverse Current on GND pin	-50	20	mA
Reverse Current on GND pins, t < 120 s	-100	250	mA
Voltage on INx, DEN, SEL, SEH and THER pins	-0.3	7	V
Current on INx, DEN, SEL, SEH and THER pins	-10		mA
Voltage on STx or FAULT pin	-2.7	7	V
Current on STx or FAULT pin	-30	10	mA
Input PWM Frequency on INx pin		2	kHz
Voltage on ICL pin	-0.3	7	V
Current on ICL pin	-2	30	mA
Voltage on CS pin	-2.7	7	V
Current on CS pin	-2	30	mA
T <sub>J</sub> Junction Temperature Range	-40	150	°C
T <sub>A</sub> Ambient Temperature Range	-40	125	°C
T <sub>STG</sub> Storage Temperature Range	-65	150	°C
T <sub>L</sub> Lead Temperature (Soldering 10 sec)		260	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

#### **ESD, Electrostatic Discharge Protection**

Parameter		Condition	Minimum Level	Unit
НВМ	Human Body Model ESD	AEC Q100-002	±4	kV
CDM	Charged Device Model ESD	AEC Q100-011, all pins	±1	kV

#### **Recommended Operating Conditions**

	Parameter	Min	Max	Unit
V <sub>VS</sub>	Supply Voltage on VS pin	4	40	V

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<sup>(2)</sup> All voltage values are with respect to GND.

<sup>(3)</sup> All absolute negative voltage on these terminals is not to go below -0.3 V.

<sup>(4)</sup> Absolute maximum voltage, withstand 48-V load dump voltage for 400 ms.

<sup>(5)</sup> Reverse polarity condition: t < 60 s, reverse current < Irev1, GND pin 1-k $\Omega$  resistor in parallel with diode.

<sup>(6)</sup> Not subject to production test, specified by design.



	Parameter			Unit
	Voltage on INx, DEN, SEL, SEH, and THER pins	0	5	V
	Voltage on STx and FAULT pins	0	5	V
Іоит	Nominal DC Load Current	0	2.5	Α
T <sub>A</sub>	Ambient Temperature Range	-40	125	°C
TJ	Junction Temperature Range	-40	150	°C

#### **Thermal Information**

Package Type	θ <sub>JA</sub>	а Өјв Өјс,воттом		Unit
ETSSOP14	35	15	3	°C/W

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#### **Electrical Characteristics**

All test conditions:  $T_A = -40^{\circ}\text{C}$  to +125°C; typical values at  $T_A = 25^{\circ}\text{C}$ ,  $V_{VS} = 5 \text{ V}$  to 40 V, over operating free-air temperature range (unless otherwise noted)

	Parameter	Conditions	Min	Тур	Max	Unit
Supply Vo	Itage and Current					
Vvs	Operating Voltage Range		4		40	V
V <sub>VS,EXT</sub>	Extended Operating Voltage Range		3.5	S	4	V
	Lindam saltaga Lagisaut	VS rising to device turns on	3.4	3.7	4	V
UVLO	Undervoltage Lockout	VS falling to device turns off		3.2	3.4	V
	Hysteresis			500		mV
I <sub>VS</sub>	Operating Current	$V_{VS}$ = 13.5V, $V_{INx}$ = 5 V, $V_{DEN}$ = 0 V, $I_{OUTx}$ = 0.5 A, current limit is set to 2 A, all channels on	) \		5	mA
		V <sub>VS</sub> = 13.5 V, V <sub>INX</sub> = V <sub>DEN</sub> = V <sub>CS</sub> = V <sub>ICL</sub> = V <sub>OUTX</sub> = V <sub>THER</sub> = 0 V, T <sub>A</sub> = 25°C			0.5	μA
loff	Operating Current in OFF Mode	$V_{VS} = 13.5 \text{ V}, V_{INx} = V_{DEN} = V_{CS}$ = $V_{ICL} = V_{OUTx} = V_{THER} = 0 \text{ V}, T_A$ = $105^{\circ}\text{C}$			5	μА
		$V_{VS} = 13.5 \text{ V}, V_{INx} = V_{DEN} = V_{CS}$ = $V_{ICL} = V_{OUTx} = V_{THER} = 0 \text{ V}, T_A$ = $125^{\circ}\text{C}$			12	μA
I <sub>OFF,DIAG</sub>	Operating Current with Diagnostic Enabled in OFF Mode	$V_{VS}$ = 13.5 V, $V_{INx}$ = 0 V, $V_{DEN}$ = 5 V, $V_{VS}$ – $V_{OUTx}$ > $V_{OL,OFF}$ , not in open-load mode			5	mA
t <sub>OFF,DEG</sub> (1)	Off-mode Deglitch Time	IN logic from HIGH to LOW, if waiting time > t <sub>OFF,DEG</sub> , enters standby mode.		12.5		ms
		V <sub>VS</sub> = 13.5 V, V <sub>INx</sub> = V <sub>DEN</sub> = V <sub>OUTx</sub> = 0, T <sub>A</sub> = 25°C			0.5	μА
loff,out	OUT Leakage Current in OFF Mode	V <sub>VS</sub> = 13.5 V, V <sub>INx</sub> = V <sub>DEN</sub> = V <sub>OUTx</sub> = 0, T <sub>A</sub> = 105°C			5	μА
		V <sub>VS</sub> = 13.5 V, V <sub>INx</sub> = V <sub>DEN</sub> = V <sub>OUTx</sub> = 0, T <sub>A</sub> = 125°C			12	μA
Logic Con	trol (INx, DEN, SEL, SEH, and THI	ER)				
V <sub>IH,LOGIC</sub>	Logic Input High-level Voltage		2			V
V <sub>IL,LOGIC</sub>	Logic Input Low-level Voltage				8.0	V
V <sub>HYS,LOGIC</sub>	Hysteresis Voltage			300		mV
R <sub>PD</sub>	Pulldown Resistor	V <sub>INx</sub> = V <sub>SEL</sub> = V <sub>SEH</sub> = V <sub>THER</sub> = 5 V		175		kΩ

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	Parameter	Conditions	Min	Тур	Max	Unit
		V <sub>VS</sub> = V <sub>DEN</sub> = 5 V		275		kΩ
Output Po	wer Stage					
		V <sub>VS</sub> > 5 V, T <sub>A</sub> = 25°C		160		mΩ
Ron	Turn-on Resistance	V <sub>VS</sub> > 5 V, T <sub>A</sub> = 150°C		260		mΩ
		V <sub>VS</sub> = 3.5 V, T <sub>A</sub> = 25°C		160		mΩ
	Inherent Current Limit		5.5		8.5	Α
		Inherent current limit under thermal cycling condition	,	3.5		Α
I <sub>LIM</sub>	Current Limit during Over- Temperature Protection	Inherent current limit under thermal cycling condition. Percentage of current limit set value		50%		
V <sub>DS</sub>	Drain-to-Source Internally Clamped Voltage		49		70	V
V <sub>F</sub>	Drain-to-Source Diode Voltage	$V_{INx} = 0$ , $I_{OUTx} = -0.2$ A		0.7		V
		OUT short-to-battery condition. t < 60 s, V <sub>INx</sub> = 0 V. T <sub>A</sub> = 25°C. Single channel is reversed.		2.5		Α
I <sub>REV</sub> (1) Continuous Reverse Source to Drain	Continuous Reverse Current from Source to Drain	Reverse-polarity condition. $t < 60 \text{ s}$ , $V_{\text{INx}} = 0 \text{ V}$ , GND pin $1\text{-k}\Omega$ resistor in parallel with diode. $T_{\text{A}} = 25^{\circ}\text{C}$ . All channels are reversed.		2		Α
t <sub>D,ON</sub> <sup>(1)</sup>	Turn-On Delay Time	$V_{VS}$ = 13.5 V, $V_{DEN}$ = 5 V, $I_{OUTx}$ = 0.5 A, IN rising edge to $V_{OUTx}$ = 10%	20		90	μs
t <sub>D,OFF</sub> (1)	Turn-Off Delay Time	$V_{VS}$ = 13.5 V, $V_{DEN}$ = 5 V, $I_{OUTx}$ = 0.5 A, IN falling edge to $V_{OUTx}$ = 90%	20		90	μs
dV/dt <sub>ON</sub> (1)	Turn-On Slew Rate	V <sub>VS</sub> = 13.5 V, V <sub>DEN</sub> = 5 V, I <sub>OUTx</sub> = 0.5 A, V <sub>OUTx</sub> = 10% to 90%	0.1		0.55	V/µs
dV/dt <sub>OFF</sub>	Turn-Off Slew Rate	V <sub>VS</sub> = 13.5 V, V <sub>DEN</sub> = 5 V, I <sub>OUTx</sub> = 0.5 A, V <sub>OUTx</sub> = 90% to 10%	0.1		0.55	V/µs
ΔdV/dt <sup>(1)</sup>	Turn On and Off Delay Time Difference, $t_{d,rise}$ — $t_{d,fall}$	$\begin{split} &V_{\text{VS}} = 13.5 \text{ V},  V_{\text{DEN}} = 5 \text{ V},  I_{\text{OUTx}} \\ &= 0.5 \text{ A. } t_{\text{d,rise}} \text{ is the V}_{\text{INx}}  \text{rising} \\ &= \text{edge to V}_{\text{OUTx}} = 90\%.  t_{\text{d,fall}}  \text{is the} \\ &V_{\text{INx}}  \text{falling edge to V}_{\text{OUTx}} = 10\% \end{split}$	-50		50	μs
Fault Dete	ction and Diagnosis					
I <sub>LG,OUT</sub>	OUT Leakage Current with Loss-of-Ground Condition				100	μA

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	Parameter	Conditions	Min	Тур	Max	Unit
$V_{OL,OFF}$	Open-Load Detection Threshold in OFF Mode	$V_{\text{INx}}$ = 0 V, when $V_{\text{VS}}$ – $V_{\text{OUT}}$ < $V_{\text{OL,OFF}}$ and duration longer than $t_{\text{OL,OFF}}$ , open load fault detected.	1.4	2	2.6	V
$t_{\text{d,OL,OFF}}$	Open-Load Detection Threshold Deglitch	$V_{\text{INx}}$ = 0 V, when $V_{\text{VS}}$ – $V_{\text{OUT}}$ < $V_{\text{OL,OFF}}$ and duration longer than $t_{\text{OL,OFF}}$ , open load fault detected.	300	600	800	μs
I <sub>OL,OFF</sub>	Open-Load Current Sink in OFF Mode	V <sub>INX</sub> = 0 V, V <sub>DEN</sub> = 5 V, V <sub>VS</sub> = V <sub>OUT</sub> = 13.5 V, T <sub>A</sub> = 125°C.	<b>-</b> 75	6		μΑ
$t_{\text{OL},\text{OFF}}$	Open-Load Detection Deglitch Time in OFF Mode	$V_{\text{INx}}$ = 0 V, When $V_{\text{VS}}$ – $V_{\text{OUT}}$ < $V_{\text{OL,OFF}}$ and duration longer than $t_{\text{OL,OFF}}$ , open load fault detected.		600		μs
V <sub>STx</sub>	Status Output Low Voltage	$I_{\overline{STx}} = 2 \text{ mA. (TPS42Q20AQ)}$			0.4	V
VFAULT	Fault Output Low Voltage	I <sub>FAULT</sub> = 2 mA. (TPS42Q20BQ)			0.4	V
t <sub>CL</sub>	Deglitch Time when Current Limit Occurs	$V_{\overline{INx}} = V_{DEN} = 5 \text{ V}$ , the deglitch time from current limit toggling to $\overline{FAULT}$ , $\overline{STx}$ , CS report.	80		180	μs
$T_{SD}$	Thermal Shutdown Threshold			175		°C
$T_{\text{SD},\text{RST}}$	Thermal Shutdown Status Reset			155		°C
T <sub>SW</sub>	Thermal Swing Shutdown Threshold			60		°C
T <sub>HYS</sub>	Hysteresis for Resetting the Thermal Shutdown and Thermal Swing			10		°C
Current S	Sense					
Kcs	Current Sense Ratio			300		
K <sub>CL</sub>	Current Limit Ratio			2500		
		V <sub>VS</sub> = 13.5 V, I <sub>OUTx</sub> ≥ 5 mA	-65%		65%	
		V <sub>VS</sub> = 13.5 V, I <sub>OUTx</sub> ≥ 25 mA	-15%		15%	
ΔCS	Current Sense Accuracy,	V <sub>VS</sub> = 13.5 V, I <sub>OUTx</sub> ≥ 50 mA	-8%		8%	
		V <sub>VS</sub> = 13.5 V, I <sub>OUTx</sub> ≥ 100 mA	-4%		4%	
		V <sub>VS</sub> = 13.5 V, I <sub>OUTx</sub> ≥ 500 mA	-3%		3%	
(2)		I <sub>LIMIT</sub> ≥ 0.25 A	-20		20	%
ΔK <sub>CL</sub> (3)	Current Limit Accuracy	I <sub>LIMIT</sub> ≥ 0.5 A	-15		15	%
).	0	V <sub>VS</sub> ≥ 6.5 V	0		4	V
Vcs	Current Sense Voltage Range	5 V ≤ V <sub>VS</sub> < 6.5 V	0		V <sub>VS</sub> -2.5	V
	Current Sense Leakage Current	$V_{INX} = 5 \text{ V}, R_{LOAD} = 10 \Omega, V_{DEN} = 0 \text{ V}, T_A = 125^{\circ}\text{C}$			1	μA
Ics,off	in OFF Mode	V <sub>INX</sub> = 0 V, V <sub>DEN</sub> = 0 V, T <sub>A</sub> = 125°C			0.5	μΑ
Іоит	Output Current Range	V <sub>VS</sub> ≥ 6.5 V, V <sub>CS</sub> ≤ 4 V	0		2.5	Α

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	Parameter	Conditions	Min	Тур	Max	Unit
		5 V ≤ V <sub>VS</sub> < 6.5 V, V <sub>CS</sub> ≤ V <sub>VS</sub> − 2.5 V	0		2.5	A
		V <sub>VS</sub> ≥ 7 V	4.5	4.75	5	V
V <sub>cs,н</sub>	Current-Sense Fault High Voltage	5 V ≤ V <sub>VS</sub> < 7 V	Min (V <sub>V</sub> s - 0.8, 4.5)		4.9	V
I <sub>CS,H</sub>	Current-Sense Fault Condition Current	V <sub>CS</sub> = 4.5 V, V <sub>VS</sub> = 13.5 V	15	S		mA
V <sub>CL,TH</sub>	Current-Limit Internal Threshold Voltage			0.8		V
(1)	CS Settling Time from DEN Disabled	$V_{VS}$ = 13.5 V, $V_{INx}$ = 5 V, $I_{OUT}$ $\geq$ 0.5 A. $V_{DEN}$ from 5 to 0 V. CS to 10% of sense value.			20	μs
t <sub>CS,OFF</sub> (1)	CS Settling Time from IN Falling Edge	$V_{VS}$ = 13.5 V, $V_{DEN}$ = 5 V, $I_{OUT} \ge$ 0.5 A. INx from 5 to 0 V. CS to 10% of sense value.			100	μs
(1)	CS settling time from DEN enabled	$V_{VS}$ = 13.5 V, $V_{INx}$ = 5 V, $I_{OUT}$ $\geq$ 0.5 A. $V_{DEN}$ from 0 to 5 V. CS to 90% of sense value.			20	μs
t <sub>CS,ON</sub> (1)	CS settling time from IN rising edge	$V_{VS}$ = 13.5 V, $V_{DEN}$ = 5 V, $I_{OUT} \ge$ 0.5 A. $V_{IN}$ from 0 to 5 V. CS to 90% of sense value.			150	μs
t <sub>SEx</sub>	Multi-Channel Current Sense Transition Delay Time	V <sub>VS</sub> = 13.5 V, V <sub>D_EN</sub> = 5 V, current sense output delay when multi-sense pins SEL and SEH transition from channel to channel			50	μs

<sup>(1)</sup> Not subject to production test, specified by design.

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<sup>(2)</sup> Measured on bench with 10 pcs/3 lots samples.

<sup>(3)</sup> The accuracy of the external current limit is only applicable when the over-current conditions are more than 1.5 times the current-limit setting.



### **Typical Performance Characteristics**

All test conditions:  $V_S$  = 13.5 V, unless otherwise noted.

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### **Detailed Description**

#### Overview

The TPS42Q20Q is a  $160\text{-m}\Omega$  4-channel high-side power switch product with AEC-Q100 qualified.

The TPS42Q20Q has a wide voltage operating range of 3.5 V to 40 V, with an absolute maximum rating of 45 V. This flexibility makes it suitable for various automotive applications in different conditions.

The TPS42Q20Q is equipped with high-precision current sensing capabilities. It offers a current sense accuracy of 3% for the loads of 500 mA or greater, and 8% for the loads of 50 mA or greater. This accurate current sensing enables easy identification of load status and measurement of load current.

The TPS42Q20Q integrates full fault detection and device protection to prevent the device damage from open load, overload, over temperature, short-circuit to the battery, short-circuit to ground, reverse battery, loss of ground, loss of power supply and voltage clamp. With all these protection functions, this device is suitable for different resistive, inductive and capacitive loads.

The TPS42Q20Q is designed to operate within the ambient temperature range from −40°C to +125°C. Moreover, the TPS42Q20Q provides a thermal-enhanced ETSSOP28 package to enable sustained operation despite significant dissipation across the device.

#### **Functional Block Diagram**

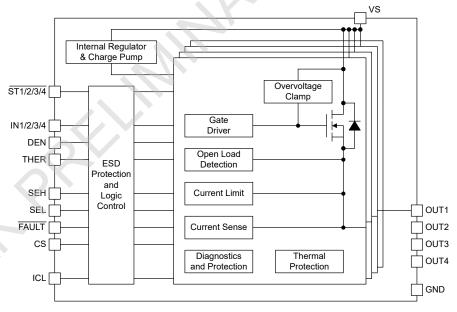


Figure 1. Functional Block Diagram

### **Feature Description**

#### **Under-Voltage Lockout (UVLO)**

The TPS42Q20Q uses the VS UVLO control to keep the output off until the internal circuitry operates properly. When the VS voltage is lower than the UVLO falling threshold, the TPS42Q20Q stays in the shutdown mode. When the VS voltage is greater than the UVLO rising threshold, the device enters operation mode.

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#### Channel Control (IN1, IN2, IN3, and IN4)

The TPS42Q20Q integrates the IN1, IN2, IN3 and IN4 pins to control each channel. The INx (x = 1, 2, 3, and 4) pins are active high. Connect these pins to the GPIO ports of an external processor or digital logic control circuit to turn on and off the internal power MOSFET of each channel.

### Status Indication (ST1, ST2, ST3, and ST4)

For the TPS42Q20AQ, the STx (x = 1, 2, 3, and 4) pins are integrated to indicate the device output status of each channel. STx are open-drain output pins and external pull-up resistors are required.

When the fault diagnostic control pin is low (DEN = L), the STx pins are internally high impedance, and they are pulled up high. When DEN = H, the voltage of the STx pins changes according to the output status.

#### **Current Sense (CS)**

For the TPS42Q20BQ, a CS pin is integrated to sense the output current and diagnostic fault conditions.

When the fault diagnostic control pin is low (DEN = L), the CS pin is internally high impedance. When DEN = H, a current mirror is internally implemented to source a current of IOUTx/KCS, which is directed outward to the external resistor connected between the CS pin and the ground, and a voltage is formed on the CS pin. It is suggested to keep the CS voltage in the range of 0 to 4 V during normal operation. Use Equation 1 to calculate the external current sense resistor, Rcs.

$$R_{CS} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{CS}}{I_{OUT}}$$
 (1)

where, K<sub>CS</sub> is the ratio of the output current to the sensed current. It is a constant value regardless of temperature and supply voltage variations.

When fault conditions occur, the CS pin works as a fault indication pin. In the on state, the Vcs voltage is almost 0 while operating in the condition of an open-load or short-t-battery fault. In the OFF state, the Vcs voltage is internally pulled-up to V<sub>CS,H</sub> while operating in the condition of a current-limit, thermal-shutdown, thermal-swing, open-load, or short-to-battery fault. Refer to Diagnostics and Fault Protections for more details.

#### Multiplexing of Current Sense (SEH, SEL)

For the TPS42Q20BQ, SEH and SEL pins are used to select the output channel that needs current detection.

#### Adjustable Current Limit (ICL)

The TPS42Q20Q integrates an accurate current limit function, and it is adjustable with the external resistor R<sub>ICL</sub>. When the overload or short-to-ground condition occurs, the current limit function will limit the maximum current through the power FET at the set value and pull up the CS pin voltage to Vcs internally.

There are two current-limit thresholds: the internal current limit and the external adjustable current limit.

While the ICL pin is connected to ground directly, the internal current limitation is used. The internal current limit is set to a fixed value of 3.5 A typically.

While an external resistor is connected at the ICL pin, it transforms a proportional load current into a voltage signal, which is compared with the internal reference voltage, V<sub>CL,TH</sub>. When V<sub>ICL</sub> exceeds V<sub>CL,TH</sub>, a closed feedback loop is immediately activated, and the current is clamped at the set value. When a ground network is used, the R<sub>ICL</sub> must be connected to the device GND directly. Use Equation 3 to calculate the R<sub>ICL</sub>.

$$I_{LIM} = \frac{V_{CL, TH}}{R_{ICL}} = \frac{I_{OUT}}{K_{CL}}$$

$$R_{ICL} = \frac{V_{CL, TH} \times K_{CL}}{I_{OUT}}$$
(2)

$$R_{ICL} = \frac{V_{CL, TH} \times K_{CL}}{I_{OUT}}$$
 (3)

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After the VS is powered up and IN is high, both the internal current limit and the external current limit are active, and the lower one is utilized as the effective current limit.

To provide enhanced protection against a hard short-to-ground condition, an open-loop fast-response mechanism is set to turn off the channel before the current-limit closed loop is established. The open-loop response time is approximately 1 µs.

#### **Inductive Load Switching-Off Clamp**

When an inductive load of the TPS42Q20Q is turned off, the output voltage is drawn down to a negative level due to the inductance characteristics. The internal power MOSFET could be damaged if the drain-to-source voltage (VDS) is not clamped during the current decay period. In this condition, the V<sub>DS,CLAMP</sub> voltage is necessary to limit the voltage across the drain and source, and thus prevent the device from damage. During the current-decay period, the TPS42Q20Q turns on the internal power MOSFET to release the energy stored in the inductance. Both the energy from the power supply and the energy from the inductive load are dissipated by the high-side power switch. If there is any resistance in series with the inductance, part of the energy will be also dissipated through this resistance. For PWM-controlled inductive loads, it is recommended to add an external freewheeling diode to protect the device from repetitive power stress.

#### **Diagnosis Enable Function (DEN)**

The TPS42Q20Q uses the DEN pin to control whether the device diagnostic function is active or not. When multiple TPS42Q20Q chips share the same ADC or I/O channel, the multiplexing function can be achieved by the DEN control. Additionally, pulling down the DEN pin can significantly reduce the TPS42Q20Q's total power consumption to below 500 nA.

DEN	INx Pin	SEH	SEL	CS Channel	CS, FAULT, STx	Protections and Diagnostics
	-	0	0	Channel 1	See Table 3.	See Table 3.
	_	0	1	Channel 2	See Table 3.	See Table 3.
Н	_	1	0	Channel 3	See Table 3.	See Table 3.
	_	1	1	Channel 4	See Table 3.	See Table 3.
L	Н	-	-/	-	High Impedance	Diagnostics are disabled, and protections are normal.
_	L	-	7-	_	High Impedance	Diagnostics are disabled, and no protection.

**Table 2. DEN Logic Table** 

#### **Diagnostics and Fault Protections**

When DEN is high, status indication  $(\overline{STx})$  or current sense (CS) is enabled. When DEN is low, status indication  $(\overline{STx})$  or current sense (CS) is disabled, and the output of STx or CS is in high-impedance mode. **Table 3. Fault Table** 

Condition	INx	OUTx	THER	Criterion	STx (TPS42Q20 AQ)	CS (TPS42Q20 BQ)	FAULT (TPS42Q20 BQ)	Fault Recovery
Name	L	L	_	_	Н	0	Н	-
Normal	Н	Н	_	_	Н	Linear	Н	-
Overload, Short to Ground	Н	L	-	Current limit.	L	V <sub>CS,H</sub>	L	Auto
Open Load <sup>(1)</sup> , Short to Battery, Reverse Polarity	L	Н	-	V <sub>VS</sub> - V <sub>OUTx</sub> < V <sub>OL,OFF</sub> .	L	V <sub>CS,H</sub>	L	Auto

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Condition	INx	OUTx	THER	Criterion	STx (TPS42Q20 AQ)	CS (TPS42Q20 BQ)	FAULT (TPS42Q20 BQ)	Fault Recovery
	Н	_	L	Thermal shutdown.	L	V <sub>CS,H</sub>	L	Auto
Over Temperature	Н	_	Н	Thermal shutdown.	L	V <sub>CS,H</sub>	L	Latch
	Н	_	_	Thermal swing.	L	Vcs,н	L	Auto

<sup>(1)</sup> Need external pullup resistor during off-state

#### Overload and Short to Ground Fault

When the INx pins are high and the output channels are switched on, the over-load or short-to-ground condition will trigger the device current limitation. In this condition, the output current of the fault channel is limited to the set value, and the corresponding  $\overline{STx}$  pin is pulled low or the CS pin is pulled to  $V_{CS,H}$ . The current limit and the  $\overline{STx}$  or the CS pin will be recovered automatically when the fault is removed. The long-time current limit will cause the thermal shutdown to prevent the device from damage.

#### **Open Load Fault**

When the INx pins are high and the output channels are switched on, there will be an output current supplied to the load.

- The TPS42Q20AQ will report an open-load fault by pulling the corresponding \$\overline{STx}\$ pin low (when the output current is less than Iol.on).
- The TPS42Q20BQ will diagnose the fault by reading the V<sub>CS</sub> voltage. With the accurate current sense, the TPS42Q20BQ can support a very low open-load detection threshold. It is recommended to set 10 mA as the upper limit for the open-load detection threshold and 25 mA as the lower limit for the normal operation current.

When the INx pins are low and the output channel is switched off, the output voltage will be pulled down to 0 V with a connected load and will remain close to the supply voltage with an open load ( $V_{VS} - V_{OUTX} < V_{OL,OFF}$ ).

- The TPS42Q20AQ will report an open-load fault by pulling the corresponding STx pin low.
- The TPS42Q20BQ will pull the CS pin voltage up to V<sub>CS,H</sub>. It is recommended to use an external pull-up resistor at the OUTx pin to eliminate the influence of the leakage current, I<sub>OL,OFF</sub>. The pull-up current should not be greater than the load current to prevent false triggering during normal operation. It is recommended to use a switch in series with the pull-up resistor to reduce the standby current and use the pull-up resistor R<sub>PU</sub> less than 15 kΩ.

#### **Short-to-Battery Fault**

The TPS42Q20Q integrates the short-to-battery fault detection, which has the same operating mechanism and behavior as the open-load detection.

In the ON state with the INx high, the reverse current, caused by the short-to-battery fault, flows the internal MOSFET and lead to small power dissipation on the device.

In the OFF state with the INx low, the short-to-battery fault is reported when  $V_{OUTx}$  is greater than  $V_{VS}$ , but the reverse current is determined by the voltage difference between  $V_{OUTx}$  and  $V_{VS}$ . When  $V_{OUTx} - V_{VS} < V_F$ , there is no reverse current. When  $V_{OUTx} - V_{VS} > V_F$ , reverse current occurs. Please note, that the reverse current should be less than  $I_{REV}$  to prevent the device from damage.

#### **Reverse-Polarity Fault**

The TPS42Q20Q integrates the reverse-polarity fault detection, which has same operating mechanism and behavior as the open-load detection.

In the ON state with the INx high, the reverse current, caused by the reverse polarity, flows the internal MOSFET and leads to small power dissipation on the device.

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In the OFF state with the INx low, reverse-polarity is reported and the reverse current flows through the body diode will cause high power dissipation. Please note, that the reverse current should be less than I<sub>REV</sub> to prevent the device from damage.

#### **Reverse-Current Protection**

Either of the short-to-battery fault or the reverse-polarity fault will cause the reverse current flowing through the device. Usually, there are two methods to block the reverse current.

- 1. Add a block diode between the power supply and the VS pin. With this method, both the device and load are protected from the reverse current fault.
- 2. Add a ground network between the GND pin and the system ground. It is recommended to use an  $I_F > 100$ mA diode and a 1-k $\Omega$  resistor in parallel in the ground network. With this method, only the TPS42Q20Q device is protected from the reverse current fault, and the load is protected by itself.

Please note, when the ground network is used, the R<sub>ICL</sub> must be connected to the device GND pin directly.

#### **Loss-of-Ground Protection**

The TPS42Q20Q turns off the output when the loss-of-ground fault occurs, no matter whether the IN-pin signal is high or low.

#### **Loss-of-Power Supply Protection**

The TPS42Q20Q turns off the output when the loss-of-power fault occurs, no matter whether the IN-pin signal is high or low. When a loss-of-power fault occurs, the inductive load will still sink current from all pins connected. It is recommended to use the ground network or a freewheeling diode to prevent damage from negative voltage.

#### **Over-Temperature Fault and Protection**

The TPS42Q20Q integrates two mechanisms for over-temperature diagnosis and protection: thermal shutdown and thermal swing.

When the junction temperature  $T_J$  rises above the thermal shutdown threshold  $T_{SD}$ , thermal shutdown works and turns off the output immediately. When the device cools down and the junction temperature falls below  $T_{SD}$  –  $T_{HYS}$ , the output turns on again. In the thermal shutdown condition, the  $\overline{STx}$  pin of TPS42Q20AQ is pulled down and the CS pin of TPS42Q20BQ is pulled up to  $V_{CS,H}$ , and the current limit is reduced to  $I_{LIM,STD}$  or half of the set value to prevent the device repeating thermal shutdown. The thermal shutdown fault signal and the reduced current limit will not be reset until the junction temperature decreases below  $T_{SD,RST}$ .

When the MOSFET junction temperature  $T_{MOS}$  rises much more quickly than the logic control module junction temperature  $T_{LOGIC}$  and the temperature difference  $\Delta T = T_{MOS} - T_{LOGIC} > T_{SW}$ , the thermal swing works and turns off the output immediately. When the MOSFET cools down and the temperature difference  $\Delta T = T_{MOS} - T_{LOGIC} < T_{SW}T_{HYS}$ , the output turns on again. In the thermal swing condition, the  $\overline{STx}$  pin of TPS42Q20AQ is pulled down and the CS pin of TPS42Q20BQ is pulled up to  $V_{CS,H}$ . The thermal swing fault signal automatically reset after the device recovered from the thermal swing condition.

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### **Application and Implementation**

#### Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### **Application Information**

The TPS42Q20Q is a 160-m $\Omega$  4-channel high-side power switch product with AEC-Q100 qualified. The following application schematic shows a typical usage of the TPS42Q20Q series.

### **Typical Application**

Figure 2 shows the typical protection application schematic of the TPS42Q20Q.

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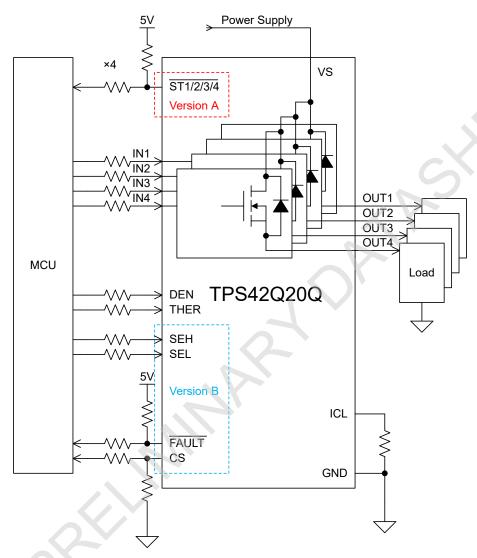


Figure 2. Typical Application Circuit

#### **Power Dissipation**

During normal operation, the junction temperature should meet the requirement in the Recommended Operating Conditions table. Use Equation 4 and Equation 5 to calculate the power dissipation and estimate the junction temperature.

The power dissipation (PD) can be calculated using Equation 4.

$$P_{D} = (I_{OUT1}^{2} + I_{OUT2}^{2} + I_{OUT3}^{2} + I_{OUT4}^{2}) \times R_{ON} + V_{S} \times I_{Q}$$
(4)

Where,

- I<sub>OUTx</sub> is the output current of each channel,
- R<sub>ON</sub> is the turn-on resistance,
- Vs is the VS pin power supply voltage,
- IQ is the quiescent current.

The junction temperature (T<sub>J</sub>) can be estimated using Equation 5.

$$T_{J} = T_{A} + P_{D} \times \theta_{JA} \tag{5}$$

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#### Where,

- T<sub>A</sub> is the ambient temperature,
- P<sub>D</sub> is the power dissipation,
- $\theta_{JA}$  is the junction-to-ambient thermal resistance.

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### Layout

#### **Layout Guideline**

To get good thermal performance and prevent over-temperature protection, the PCB layout is important. A well-designed PCB layout can effectively optimize heat dissipation, which is crucial for ensuring the long-term reliability of the device.

- It is recommended to maximize the coverage of copper on the PCB to enhance the thermal conductivity of the board.
   Since the primary heat flow path from the package to the surrounding environment passes through the copper on the PCB, having maximum copper coverage is particularly important when there is no heat sink attached to the opposite side of the board.
- It is recommended to place as many thermal vias as possible underneath the package ground pad to optimize the thermal conductivity of the board.
- It is suggested that all thermal vias be either plated shut or plugged and capped on both sides of the board to prevent solder voids to maintain reliability and performance.
- It is recommended to use wide traces or thick copper weight in the input/output current paths to minimize I×R voltage drop.

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### **Layout Example**

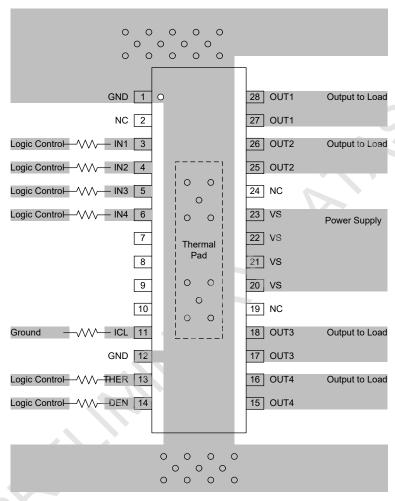


Figure 3. Layout Example

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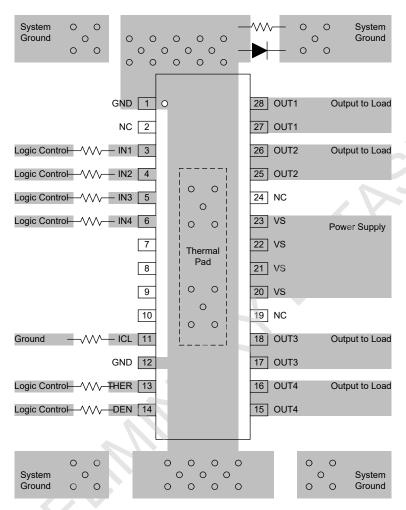
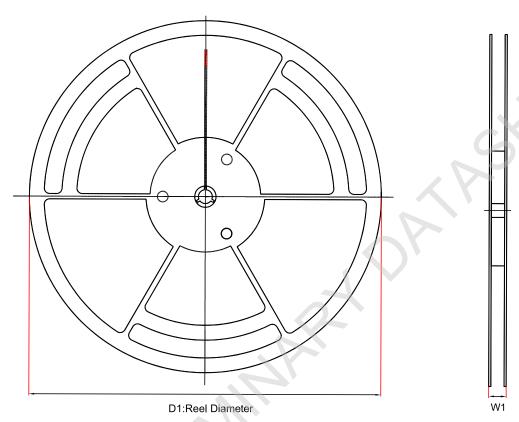


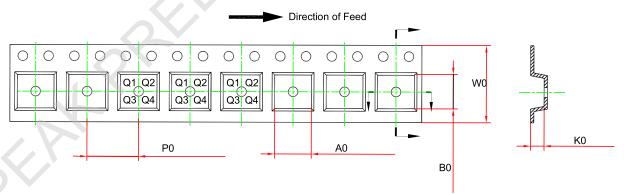
Figure 4. Layout Example with a Ground Network

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## **Tape and Reel Information**





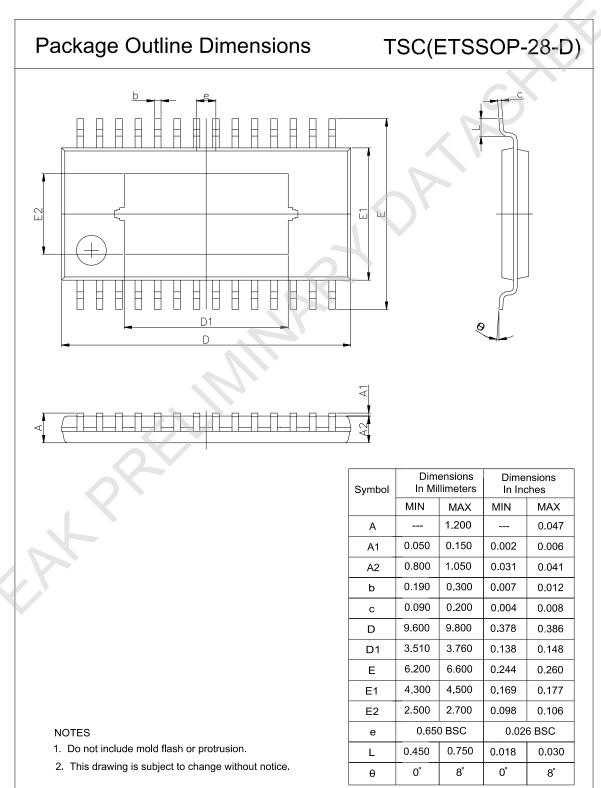
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPS42Q20AQ- TSCR-S	ETSSOP28	330	21.6	6.9	10.2	1.5	12	16	Q1
TPS42Q20BQ- TSCR-S	ETSSOP28	330	21.6	6.9	10.2	1.5	12	16	Q1

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## **Package Outline Dimensions**

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### **Order Information**

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPS42Q20AQ-TSCR-S	−40 to 125°C	ETSSOP28	SQ20A	MSL3	2,500	Green
TPS42Q20BQ-TSCR-S	−40 to 125°C	ETSSOP28	SQ20B	MSL3	2,500	Green

**Green**: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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