40-V 160-mΩ 4-Channel High-Side Power Switch

Features

- Junction Temperature Range: –40°C to +125°C
- Wide Input Voltage Range
  - 3.5 V to 40 V, with 48 V Maximum Rating
- 160-mΩ Maximum Low Turn-On Resistance at Room Temperature
- 4 Independent Input and Output Channels
- 0.3-μA Maximum Low Operating Current in OFF Mode at Room Temperature
- Compatible with 3.3-V and 5-V Logic Control
- Adjustable Current Limit
  - 500 mA to 2.5 A for Each Channel
  - ±15% Accuracy at 500 mA
- Fault Indication (TPS42Q20A)
  - Open-Drain Output Status Pin
  - Output Open Load and Short to Battery
  - Output Overload and Short to Ground
  - Over Temperature
- Diagnosis (TPS42Q20B)
  - Dedicated Current Sense Pin
  - Accurate Current Sense: ±3% at 500 mA
- Protection
  - Output Short to Battery Protection
  - Overload and Short to Ground Protection
  - Inductive Load Negative Voltage Protection
  - Loss of Ground, Loss of Supply Protection
  - Over-Temperature Protection
- Package Option
  - ETSSOP28

Applications

- Off-Board Load Power Supply
- HVAC
- Navigation, Telematics
- Transmission
- LED Lighting
- Industry Control, Factory Automation

Description

The TPS42Q20 is a 160-mΩ 4-channel high-side power switch product.

The TPS42Q20 has a wide voltage operating range of 3.5 V to 40 V, with an absolute maximum rating of 48 V. This flexibility makes it suitable for different conditions.

The TPS42Q20 is equipped with high-precision current sensing capabilities. It offers a current sense accuracy of 3% for the loads of 500 mA or greater, and 8% for the loads of 50 mA or greater. This accurate current sensing enables easy identification of load status and measurement of load current.

The TPS42Q20 integrates full fault detection and device protection to prevent the device damage from open load, overload, over temperature, short-circuit to the battery, short-circuit to ground, reverse battery, loss of ground, loss of power supply, and voltage clamp. With all these protection functions, this device is suitable for different resistive, inductive, and capacitive loads.

The TPS42Q20 is designed to operate within the junction temperature range from −40°C to +125°C. Moreover, the TPS42Q20 provides a thermal-enhanced ETSSOP28 package to enable sustained operation despite significant dissipation across the device.

Typical Application Circuit

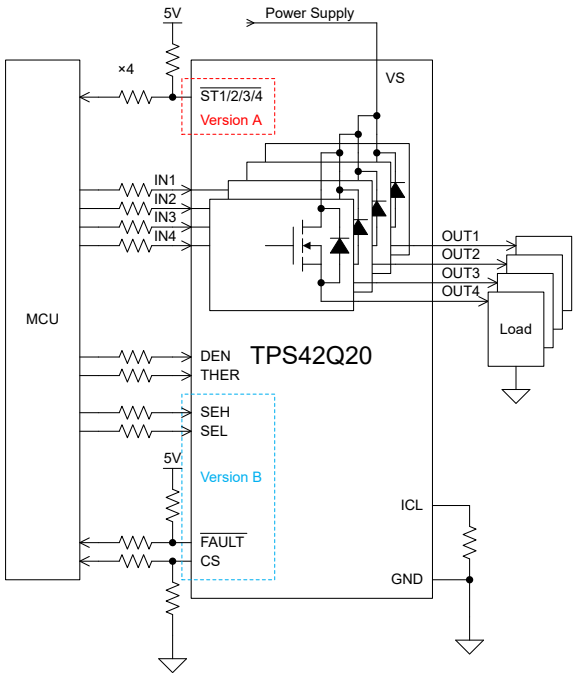


Table of Contents

Product Family Table

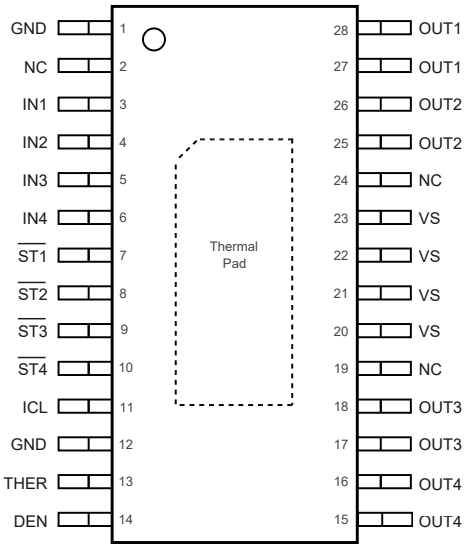
Order Number	Operating Voltage Range (V)	Feature	Package
TPS42Q20A-TSCR-S	4 to 40	Fault Indication	ETSSOP28
TPS42Q20B-TSCR-S	4 to 40	Current Sense	ETSSOP28

Revision History

Date	Revision	Notes
2026-01-18	Rev.A.0	Initial release.

Pin Configuration and Functions

TPS42Q20A
ETSSOP28 Package
Top View



TPS42Q20B
ETSSOP28 Package
Top View

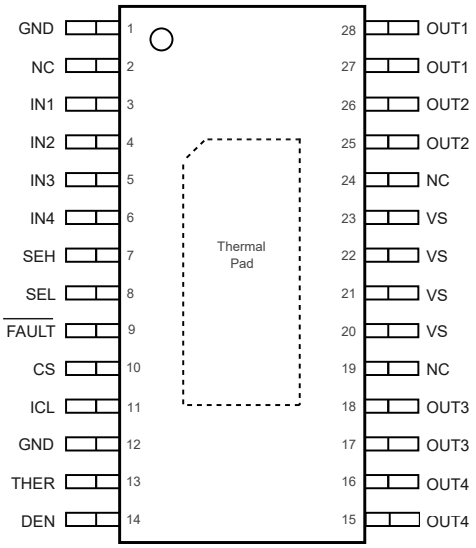


Table 1. Pin Functions: TPS42Q20

Pin No.	Pin Name		I/O	Description
	TPS42Q20A	TPS42Q20B		
10	–	CS	O	Current sense output pin (TPS42Q20B only). Connect an external resistor to ground to monitor the output current through the internal power MOS. Left this pin open if not used.
14	DEN	DEN	I	Fault-diagnosis function or current-sense function enable pin. Pull this pin HIGH to enable the function or pull this pin LOW to disable the function.
9	–	$\overline{\text{FAULT}}$	O	Device fault indication pin (TPS42Q20B only). Open-drain output. Left this pin open if not used.
1, 12	GND	GND	–	Ground reference pin.
11	ICL	ICL	O	Current limit adjust pin. Connect an external resistor to ground to set the current limit value. Connect this pin to ground if not used.
3	IN1	IN1	I	Channel 1 control input pin.
4	IN2	IN2	I	Channel 2 control input pin.
5	IN3	IN3	I	Channel 3 control input pin.
6	IN4	IN4	I	Channel 4 control input pin.
2, 19, 24	NC	NC	–	No internal connection. Suggest connecting to GND to improve the thermal performance.

Pin No.	Pin Name		I/O	Description
	TPS42Q20A	TPS42Q20B		
27, 28	OUT1	OUT1	O	Channel 1 output pin.
25, 26	OUT2	OUT2	O	Channel 2 output pin.
17, 18	OUT3	OUT3	O	Channel 3 output pin.
15, 16	OUT4	OUT4	O	Channel 4 output pin.
7	$\overline{ST1}$	–	O	Channel 1 statues indication pin (TPS42Q20A only). Open-drain output. Left this pin open if not used.
8	$\overline{ST2}$	–	O	Channel 2 statues indication pin (TPS42Q20A only). Open-drain output. Left this pin open if not used.
9	$\overline{ST3}$	–	O	Channel 3 statues indication pin (TPS42Q20A only). Open-drain output. Left this pin open if not used.
10	$\overline{ST4}$	–	O	Channel 4 statues indication pin (TPS42Q20A only). Open-drain output. Left this pin open if not used.
7	–	SEH	I	Current sense channel selection high bit (TPS42Q20B only) .
8	–	SEL	I	Current sense channel selection low bit (TPS42Q20B only) .
13	THER	THER	I	Thermal shutdown behavior control pin. Pull this pin low for auto retry or pull this pin high for latch off when thermal shutdown protection is triggered.
20, 21, 22, 23	VS	VS	I	Power supply input pin.

(1) Thermal Pad **MUST** be connected to device GND directly.

Specifications

Absolute Maximum Ratings (1) (2) (3)

Parameter		Min	Max	Unit
Supply Voltage on VS Pin, t < 400 ms (4)			48	V
Reverse Polarity Voltage on VS Pin (5)		−36		V
Continuous Drain Current on OUT Pin		Internal Limited		A
Reverse Current on GND Pin		−50	20	mA
Reverse Current on GND Pins, t < 120 s		−100	250	mA
Voltage on INx, DEN, SEL, SEH and THER Pins		−0.3	7	V
Current on INx, DEN, SEL, SEH and THER Pins		−10		mA
Voltage on $\overline{STx}$ or $\overline{FAULT}$ Pin		−2.7	7	V
Current on $\overline{STx}$ or $\overline{FAULT}$ Pin		−30	10	mA
Input PWM Frequency on INx Pin			2	kHz
Voltage on ICL Pin		−0.3	7	V
Current on ICL Pin		−2	30	mA
Voltage on CS Pin		−2.7	7	V
Current on CS Pin		−2	30	mA
T_J	Junction Temperature Range	−40	150	°C
T_A	Ambient Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.
(3) All absolute negative voltages on these terminals are not to go below −0.3 V.
(4) Absolute maximum voltage, withstand 48-V load dump voltage for 400 ms.
(5) Reverse polarity condition: t < 60 s, reverse current < Irev1, GND pin 1-kΩ resistor in parallel with diode.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{VS}	Supply Voltage Range for Normal Operation	4	40	V
$V_{VS,EXT}$	Extended Operating Voltage Range (1)	3.5	4	V
	Voltage on INx, DEN, SEL, SEH, and THER pins	0	5	V
	Voltage on $\overline{STx}$ and $\overline{FAULT}$ pins	0	5	V
I_{OUT}	Nominal DC Load Current	0	2.5	A
T_J	Junction Temperature Range	−40	125	°C

(1) The device can function properly in the extended operating range, whereas the validity of specific parametric values is not ensured.

Thermal Information

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC,TOP}$	Unit
ETSSOP28	27.7	7.5	18	°C/W

Electrical Characteristics

All test conditions: T_J = −40°C to +125°C; typical values at T_J = 25°C, V_{VS} = 5 V to 40 V, over operating free-air temperature range (unless otherwise noted)

Parameter		Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
UVLO	Undervoltage Lockout	VS rising to device turns on	3.4	3.7	4	V
		VS falling to device turns off		3.2	3.4	V
	Hysteresis			500		mV
I_{VS}	Operating Current	V_{VS} = 13.5V, V_{INx} = 5 V, V_{DEN} = 0 V, I_{OUTx} = 0.5 A, current limit is set to 2 A, all channels on			8	mA
I_{OFF}	Operating Current in OFF Mode	V_{VS} = 13.5 V, V_{INx} = V_{DEN} = V_{CS} = V_{ICL} = V_{OUTx} = V_{THER} = 0 V, T_A = 25°C			0.3	μA
		V_{VS} = 13.5 V, V_{INx} = V_{DEN} = V_{CS} = V_{ICL} = V_{OUTx} = V_{THER} = 0 V, T_A = 125°C			2	μA
$I_{OFF,DIAG}$	Operating Current with Diagnostic Enabled in OFF Mode	V_{VS} = 13.5 V, V_{INx} = 0 V, V_{DEN} = 5 V, V_{VS} – V_{OUTx} > $V_{OL,OFF}$, not in open-load mode			5	mA
$t_{OFF,DEG}$ (1)	Off-mode Deglitch Time	IN logic from HIGH to LOW, if waiting time > $t_{OFF,DEG}$, enters standby mode.		12.5		ms
$I_{OFF,OUT}$	OUT Leakage Current in OFF Mode	V_{VS} = 13.5 V, V_{INx} = V_{DEN} = V_{OUTx} = 0, T_A = 25°C			0.3	μA
		V_{VS} = 13.5 V, V_{INx} = V_{DEN} = V_{OUTx} = 0, T_A = 125°C			0.6	μA
Logic Control (INx, DEN, SEL, SEH, and THER)						
$V_{IH,LOGIC}$	Logic Input High-level Voltage		2			V
$V_{IL,LOGIC}$	Logic Input Low-level Voltage				0.8	V
$V_{HYS,LOGIC}$	Hysteresis Voltage			300		mV
R_{PD}	Pulldown Resistor	V_{INx} = V_{SEL} = V_{SEH} = V_{THER} = 5 V		175		kΩ
		V_{VS} = V_{DEN} = 5 V		275		kΩ
Output Power Stage						
R_{ON}	Turn-on Resistance	V_{VS} > 5 V, T_A = 25°C		160		mΩ
		V_{VS} > 5 V, T_A = 150°C		260		mΩ
		V_{VS} = 3.5 V, T_A = 25°C		160		mΩ
I_{LIM}	Inherent Current Limit		5		8	A
	Current Limit during Over-Temperature Protection	Inherent current limit under thermal cycling condition		3.5		A

Parameter		Conditions	Min	Typ	Max	Unit
		Inherent current limit under thermal cycling condition. Percentage of current limit set value		50%		
V_{DS}	Drain-to-Source Internally Clamped Voltage		49		70	V
V_F	Drain-to-Source Diode Voltage	V_{INx} = 0, I_{OUTx} = −0.2 A		0.7		V
I_{REV} (1)	Continuous Reverse Current from Source to Drain	OUT short-to-battery condition. t < 60 s, V_{INx} = 0 V. T_A = 25°C. Single channel is reversed.		2.5		A
		Reverse-polarity condition. t < 60 s, V_{INx} = 0 V, GND pin 1-kΩ resistor in parallel with diode. T_A = 25°C. All channels are reversed.		2		A
$t_{D,ON}$ (1)	Turn-On Delay Time	V_{VS} = 13.5 V, V_{DEN} = 5 V, I_{OUTx} = 0.5 A, IN rising edge to V_{OUTx} = 10%	20		90	µs
$t_{D,OFF}$ (1)	Turn-Off Delay Time	V_{VS} = 13.5 V, V_{DEN} = 5 V, I_{OUTx} = 0.5 A, IN falling edge to V_{OUTx} = 90%	20		90	µs
dV/dt_{ON} (1)	Turn-On Slew Rate	V_{VS} = 13.5 V, V_{DEN} = 5 V, I_{OUTx} = 0.5 A, V_{OUTx} = 10% to 90%	0.1		0.55	V/µs
dV/dt_{OFF} (1)	Turn-Off Slew Rate	V_{VS} = 13.5 V, V_{DEN} = 5 V, I_{OUTx} = 0.5 A, V_{OUTx} = 90% to 10%	0.1		0.55	V/µs
$\Delta dV/dt$ (1)	Turn On and Off Delay Time Difference, $t_{d,rise}$– $t_{d,fall}$	V_{VS} = 13.5 V, V_{DEN} = 5 V, I_{OUTx} = 0.5 A. $t_{d,rise}$ is the V_{INx} rising edge to V_{OUTx} = 90%. $t_{d,fall}$ is the V_{INx} falling edge to V_{OUTx} = 10%	−50		50	µs
Fault Detection and Diagnosis						
$I_{LG,OUT}$	OUT Leakage Current with Loss-of-Ground Condition				12	µA
$V_{OL,OFF}$	Open-Load Detection Threshold in OFF Mode	V_{INx} = 0 V, when V_{VS} – V_{OUT} < $V_{OL,OFF}$ and duration longer than $t_{OL,OFF}$, open load fault detected.	1.4	2	2.6	V
$t_{d,OL,OFF}$	Open-Load Detection Threshold Deglitch	V_{INx} = 0 V, when V_{VS} – V_{OUT} < $V_{OL,OFF}$ and duration longer than $t_{OL,OFF}$, open load fault detected.	300	600	800	µs
$I_{OL,OFF}$	Open-Load Current Sink in OFF Mode	V_{INx} = 0 V, V_{DEN} = 5 V, V_{VS} = V_{OUT} = 13.5 V, T_A = 125°C.	−75			µA

Parameter		Conditions	Min	Typ	Max	Unit
$t_{OL,OFF}$	Open-Load Detection Deglitch Time in OFF Mode	V_{INx} = 0 V, When $V_{VS} - V_{OUT} < V_{OL,OFF}$ and duration longer than $t_{OL,OFF}$, open load fault detected.		600		μs
$V_{\overline{STx}}$	Status Output Low Voltage	$I_{\overline{STx}}$ = 2 mA. (TPS42Q20A)			0.4	V
$V_{\overline{FAULT}}$	Fault Output Low Voltage	I_{FAULT} = 2 mA. (TPS42Q20B)			0.4	V
t_{CL}	Deglitch Time when Current Limit Occurs	$V_{\overline{INx}} = V_{DEN}$ = 5 V, the deglitch time from current limit toggling to $\overline{FAULT}$, $\overline{STx}$, CS report.	80		180	μs
T_{SD}	Thermal Shutdown Threshold			175		°C
$T_{SD,RST}$	Thermal Shutdown Status Reset			155		°C
T_{SW}	Thermal Swing Shutdown Threshold			60		°C
T_{HYS}	Hysteresis for Resetting the Thermal Shutdown and Thermal Swing			10		°C
Current Sense						
K_{CS}	Current Sense Ratio			300		
K_{CL}	Current Limit Ratio			2500		
ΔCS	Current Sense Accuracy,	V_{VS} = 13.5 V, I_{OUTx} ≥ 5 mA	−65%		65%	
		V_{VS} = 13.5 V, I_{OUTx} ≥ 25 mA	−15%		15%	
		V_{VS} = 13.5 V, I_{OUTx} ≥ 50 mA	−8%		8%	
		V_{VS} = 13.5 V, I_{OUTx} ≥ 100 mA	−4%		4%	
		V_{VS} = 13.5 V, I_{OUTx} ≥ 500 mA	−3%		3%	
ΔK_{CL} (3)	Current Limit Accuracy	I_{LIMIT} ≥ 0.25 A	–20		20	%
		I_{LIMIT} ≥ 0.5 A	–15		15	%
V_{CS}	Current Sense Voltage Range	V_{VS} ≥ 6.5 V	0		4	V
		5 V ≤ V_{VS} < 6.5 V	0		V_{VS}-2.5	V
$I_{CS,OFF}$	Current Sense Leakage Current in OFF Mode	V_{INx} = 5 V, R_{LOAD} = 10 Ω, V_{DEN} = 0 V, T_A = 125°C			1	μA
		V_{INx} = 0 V, V_{DEN} = 0 V, T_A = 125°C			0.5	μA
I_{OUT}	Output Current Range	V_{VS} ≥ 6.5 V, V_{CS} ≤ 4 V	0		2.5	A
		5 V ≤ V_{VS} < 6.5 V, V_{CS} ≤ V_{VS} − 2.5 V	0		2.5	A
$V_{CS,H}$	Current-Sense Fault High Voltage	V_{VS} ≥ 7 V	4.3	4.75	5	V
		5 V ≤ V_{VS} < 7 V	Min (V_{VS} – 0.8, 4.5)		5	V
$I_{CS,H}$	Current-Sense Fault Condition Current	V_{CS} = 4.5 V, V_{VS} = 13.5 V	15			mA

Parameter		Conditions	Min	Typ	Max	Unit
$V_{CL,TH}$	Current-Limit Internal Threshold Voltage			0.8		V
$t_{CS,OFF}$ (1)	CS Settling Time from DEN Disabled	V_{VS} = 13.5 V, V_{INx} = 5 V, I_{OUT} ≥ 0.5 A. V_{DEN} from 5 to 0 V. CS to 10% of sense value.			20	μs
	CS Settling Time from IN Falling Edge	V_{VS} = 13.5 V, V_{DEN} = 5 V, I_{OUT} ≥ 0.5 A. INx from 5 to 0 V. CS to 10% of sense value.			100	μs
$t_{CS,ON}$ (1)	CS Settling Time from DEN Enabled	V_{VS} = 13.5 V, V_{INx} = 5 V, I_{OUT} ≥ 0.5 A. V_{DEN} from 0 to 5 V. CS to 90% of sense value.			20	μs
	CS Settling Time from IN Rising Edge	V_{VS} = 13.5 V, V_{DEN} = 5 V, I_{OUT} ≥ 0.5 A. V_{IN} from 0 to 5 V. CS to 90% of sense value.			150	μs
t_{SEx}	Multi-Channel Current Sense Transition Delay Time	V_{VS} = 13.5 V, V_{D_EN} = 5 V, current sense output delay when multi-sense pins SEL and SEH transition from channel to channel			50	μs

(1) Not subject to production test, specified by design.

Typical Performance Characteristics

All test conditions: V_S = 13.5 V, unless otherwise noted.

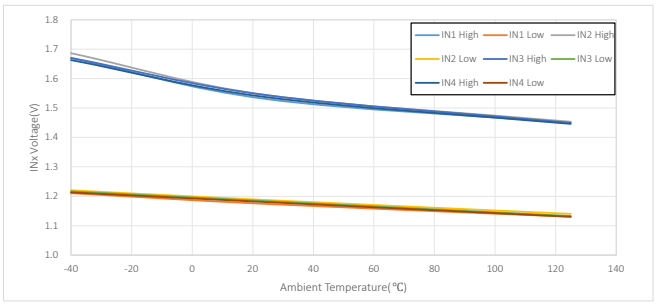


Figure 1. IN_X Voltage

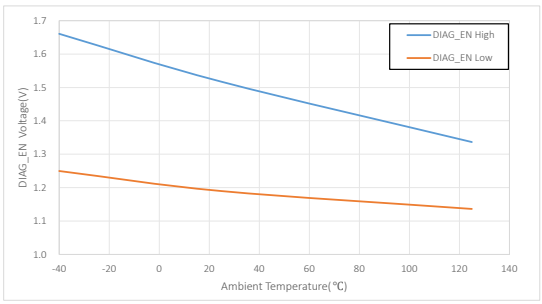


Figure 2. DIAG_EN Voltage

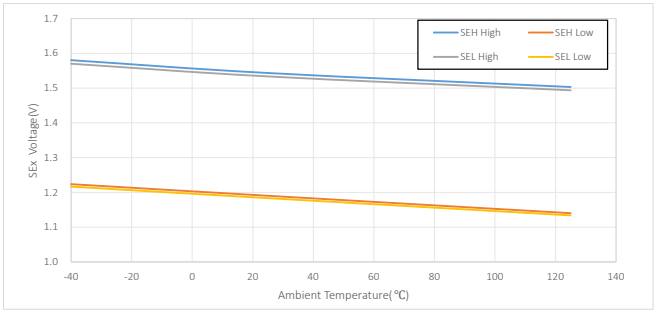


Figure 3. SE_X Voltage

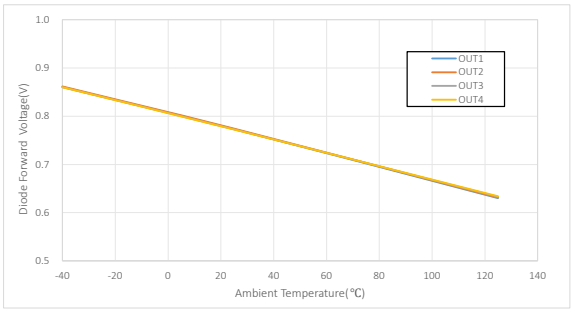


Figure 4. Diode Forward Voltage

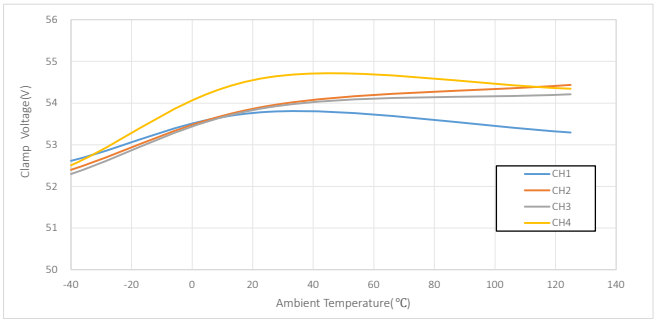


Figure 5. Clamp Voltage

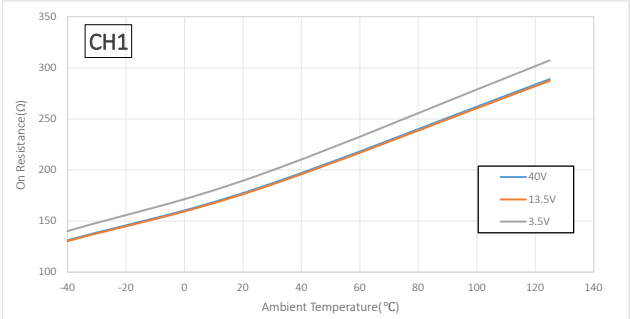


Figure 6. CH1 R_{ON}

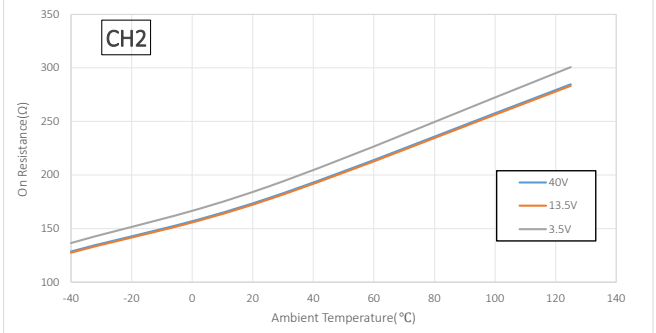


Figure 7. CH2 R_{ON}

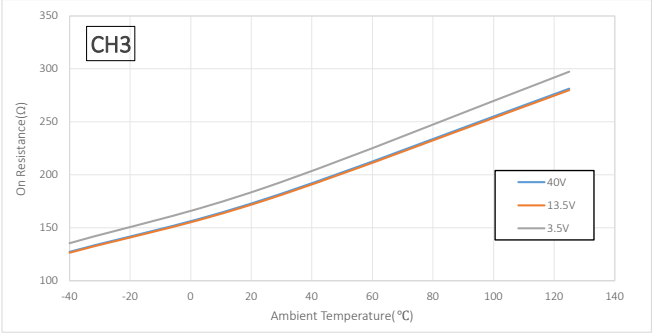


Figure 8. CH3 R_{ON}

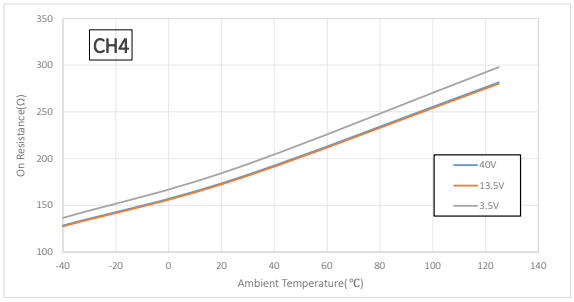


Figure 9. CH4 R_{ON}

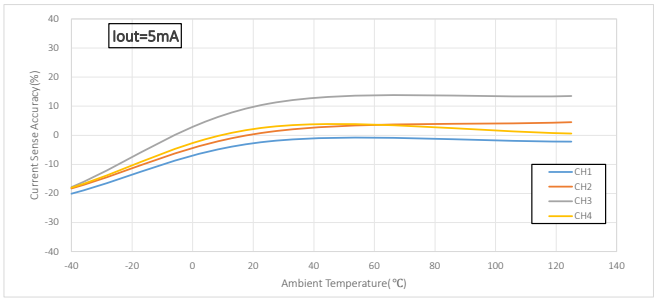


Figure 10. Current Sense Accuracy, 5 mA

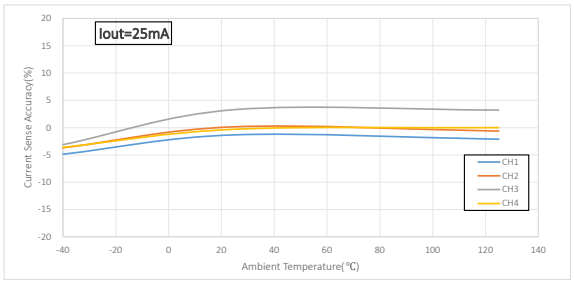


Figure 11. Current Sense Accuracy, 25 mA

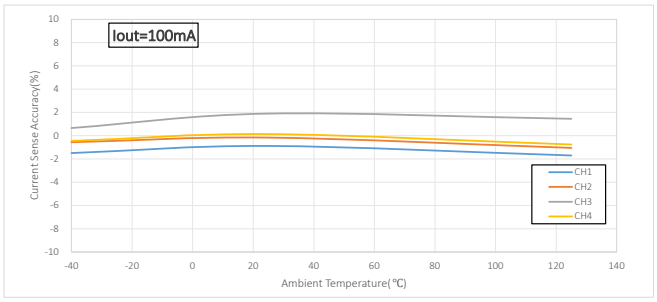


Figure 12. Current Sense Accuracy, 100 mA

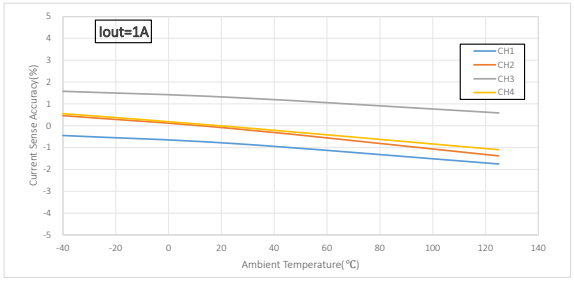


Figure 13. Current Sense Accuracy, 1 A

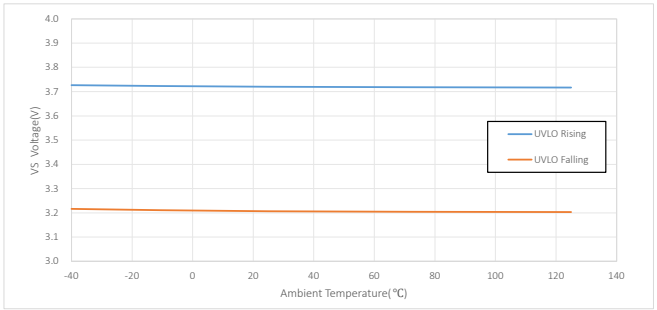


Figure 14. UVLO

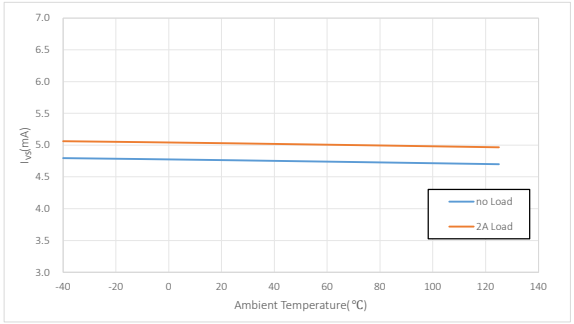


Figure 15. I_{VS}

Detailed Description

Overview

The TPS42Q20 is a 160-mΩ 4-channel high-side power switch product.

The TPS42Q20 has a wide voltage operating range of 3.5 V to 40 V, with an absolute maximum rating of 48 V. This flexibility makes it suitable for different conditions.

The TPS42Q20 is equipped with high-precision current sensing capabilities. It offers a current sense accuracy of 3% for the loads of 500 mA or greater, and 8% for the loads of 50 mA or greater. This accurate current sensing enables easy identification of load status and measurement of load current.

The TPS42Q20 integrates full fault detection and device protection to prevent the device damage from open load, overload, over temperature, short-circuit to the battery, short-circuit to ground, reverse battery, loss of ground, loss of power supply, and voltage clamp. With all these protection functions, this device is suitable for different resistive, inductive and capacitive loads.

The TPS42Q20 is designed to operate within the junction temperature range from −40°C to +125°C. Moreover, the TPS42Q20 provides a thermal-enhanced ETSSOP28 package to enable sustained operation despite significant dissipation across the device.

Functional Block Diagram

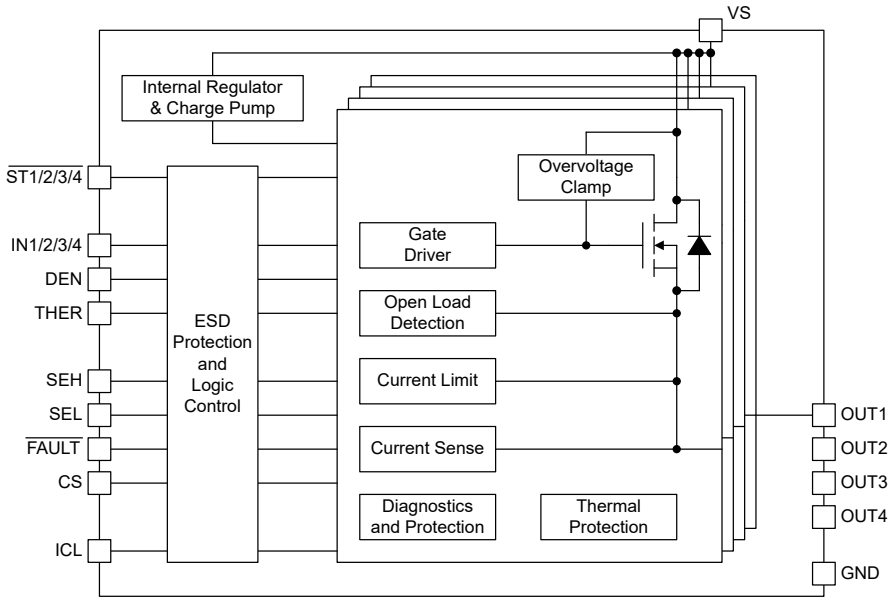


Figure 16. Functional Block Diagram

Feature Description

Under-Voltage Lockout (UVLO)

The TPS42Q20 uses the VS UVLO control to keep the output off until the internal circuitry operates properly. When the VS voltage is lower than the UVLO falling threshold, the TPS42Q20 stays in the shutdown mode. When the VS voltage is greater than the UVLO rising threshold, the device enters operation mode.

Channel Control (IN1, IN2, IN3, and IN4)

The TPS42Q20 integrates the IN1, IN2, IN3, and IN4 pins to control each channel. The INx (x = 1, 2, 3, and 4) pins are active high. Connect these pins to the GPIO ports of an external processor or digital logic control circuit to turn on and off the internal power MOSFET of each channel.

Status Indication ($\overline{ST1}$, $\overline{ST2}$, $\overline{ST3}$, and $\overline{ST4}$)

For the TPS42Q20A, the $\overline{STx}$ (x = 1, 2, 3, and 4) pins are integrated to indicate the device output status of each channel. $\overline{STx}$ are open-drain output pins, and external pull-up resistors are required.

When the fault diagnostic control pin is low (DEN = L), the $\overline{STx}$ pins are internally high impedance, and they are pulled up high. When DEN = H, the voltage of the $_{STx}$ pins changes according to the output status.

Current Sense (CS)

For the TPS42Q20B, a CS pin is integrated to sense the output current and diagnostic fault conditions.

When the fault diagnostic control pin is low (DEN = L), the CS pin is internally high impedance. When DEN = H, a current mirror is internally implemented to source a current of I_{OUTx}/K_{CS}, which is directed outward to the external resistor connected between the CS pin and the ground, and a voltage is formed on the CS pin. It is suggested to keep the CS voltage in the range of 0 to 4 V during normal operation. Use Equation 1 to calculate the external current sense resistor, R_{CS}.

$$R_{CS} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{CS}}{I_{OUT}} \quad (1)$$

where, K_{CS} is the ratio of the output current to the sensed current. It is a constant value regardless of temperature and supply voltage variations.

When fault conditions occur, the CS pin works as a fault indication pin. In the on state, the V_{CS} voltage is almost 0 while operating in the condition of an open-load or short-to-battery fault. In the OFF state, the V_{CS} voltage is internally pulled-up to $V_{CS,H}$ while operating in the condition of a current-limit, thermal-shutdown, thermal-swing, open-load, or short-to-battery fault. Refer to Diagnostics and Fault Protections for more details.

Multiplexing of Current Sense (SEH, SEL)

For the TPS42Q20B, SEH and SEL pins are used to select the output channel that needs current detection.

Adjustable Current Limit (ICL)

The TPS42Q20 integrates an accurate current limit function, and it is adjustable with the external resistor R_{ICL}. When the overload or short-to-ground condition occurs, the current limit function will limit the maximum current through the power FET at the set value and pull up the CS pin voltage to V_{CS} internally.

There are two current-limit thresholds: the internal current limit and the external adjustable current limit.

While the ICL pin is connected to ground directly, the internal current limitation is used. The internal current limit is set to a fixed value of 3.5 A typically.

While an external resistor is connected at the ICL pin, it transforms a proportional load current into a voltage signal, which is compared with the internal reference voltage, $V_{CL,TH}$. When V_{ICL} exceeds $V_{CL,TH}$, a closed feedback loop is immediately activated, and the current is clamped at the set value. When a ground network is used, the R_{ICL} must be connected to the device GND directly. Use Equation 3 to calculate the R_{ICL}.

$$\frac{V_{CL,TH}}{R_{ICL}} = \frac{I_{OUT}}{K_{CL}} \quad (2)$$

$$R_{ICL} = \frac{V_{CL,TH} \times K_{CL}}{I_{OUT}} \quad (3)$$

After the VS is powered up and IN is high, both the internal current limit and the external current limit are active, and the lower one is utilized as the effective current limit.

To provide enhanced protection against a hard short-to-ground condition, an open-loop fast-response mechanism is set to turn off the channel before the current-limit closed loop is established. The open-loop response time is approximately 1 µs.

Inductive Load Switching-Off Clamp

When an inductive load of the TPS42Q20 is turned off, the output voltage is drawn down to a negative level due to the inductance characteristics. The internal power MOSFET could be damaged if the drain-to-source voltage (V_{DS}) is not clamped during the current decay period. In this condition, the $V_{DS,CLAMP}$ voltage is necessary to limit the voltage across the drain and source, and thus prevent the device from damage. During the current-decay period, the TPS42Q20 turns on the internal power MOSFET to release the energy stored in the inductance. Both the energy from the power supply and the energy from the inductive load are dissipated by the high-side power switch. If there is any resistance in series with the inductance, part of the energy will also be dissipated through this resistance. For PWM-controlled inductive loads, it is recommended to add an external freewheeling diode to protect the device from repetitive power stress.

Diagnosis Enable Function (DEN)

The TPS42Q20 uses the DEN pin to control whether the device diagnostic function is active or not. When multiple TPS42Q20 chips share the same ADC or I/O channel, the multiplexing function can be achieved by the DEN control. Additionally, pulling down the DEN pin can significantly reduce the TPS42Q20's total power consumption to below 500 nA.

Table 2. DEN Logic Table

DEN	INx Pin	SEH	SEL	CS Channel	CS, $\overline{\text{FAULT}}$, $\overline{\text{STx}}$	Protections and Diagnostics
H	–	0	0	Channel 1	See Table 3.	See Table 3.
	–	0	1	Channel 2	See Table 3.	See Table 3.
	–	1	0	Channel 3	See Table 3.	See Table 3.
	–	1	1	Channel 4	See Table 3.	See Table 3.
L	H	–	–	–	High Impedance	Diagnostics are disabled, and protections are normal.
	L	–	–	–	High Impedance	Diagnostics are disabled, and no protection.

Diagnostics and Fault Protections

When DEN is high, status indication ($\overline{\text{STx}}$) or current sense (CS) is enabled. When DEN is low, status indication ($\overline{\text{STx}}$) or current sense (CS) is disabled, and the output of $\overline{\text{STx}}$ or CS is in high-impedance mode.

Table 3. Fault Table

Condition	INx	OUTx	THER	Criterion	$\overline{\text{STx}}$ (TPS42Q20A)	CS (TPS42Q20B)	$\overline{\text{FAULT}}$ (TPS42Q20B)	Fault Recovery
Normal	L	L	–	–	H	0	H	–
	H	H	–	–	H	Linear	H	–
Overload, Short to Ground	H	L	–	Current limit.	L	$V_{CS,H}$	L	Auto

Condition	INx	OUTx	THER	Criterion	$\overline{STx}$ (TPS42Q20A)	CS (TPS42Q20B)	$\overline{FAULT}$ (TPS42Q20B)	Fault Recovery
Open Load (1), Short to Battery, Reverse Polarity	L	H	–	$V_{VS} – V_{OUTx} < V_{OL,OFF}$.	L	$V_{CS,H}$	L	Auto
Over Temperature	H	–	L	Thermal shutdown.	L	$V_{CS,H}$	L	Auto
	H	–	H	Thermal shutdown.	L	$V_{CS,H}$	L	Latch
	H	–	–	Thermal swing.	L	$V_{CS,H}$	L	Auto

(1) Need an external pull-up resistor during off-state

Overload and Short to Ground Fault

When the INx pins are high and the output channels are switched on, the over-load or short-to-ground condition will trigger the device current limitation. In this condition, the output current of the fault channel is limited to the set value, and the corresponding $\overline{STx}$ pin is pulled low or the CS pin is pulled to $V_{CS,H}$. The current limit and the $\overline{STx}$ or the CS pin will be recovered automatically when the fault is removed. The long-time current limit will cause the thermal shutdown to prevent the device from being damaged.

Open Load Fault

When the INx pins are high and the output channels are switched on, there will be an output current supplied to the load.

- Note that the detection is not reported on the $\overline{STx}$or $\overline{FAULT}$pins.
- The MCU must multiplex the SEL and SEH pins to detect the channel-on open-load fault proactively.

When the INx pins are low and the output channel is switched off, the output voltage will be pulled down to 0 V with a connected load and will remain close to the supply voltage with an open load ($V_{VS} – V_{OUTx} < V_{OL,OFF}$).

- The TPS42Q20A will report an open-load fault by pulling the corresponding $\overline{STx}$ pin low.
- The TPS42Q20B will pull the CS pin voltage up to $V_{CS,H}$. It is recommended to use an external pull-up resistor at the OUTx pin to eliminate the influence of the leakage current, $I_{OL,OFF}$. The pull-up current should not be greater than the load current to prevent false triggering during normal operation. It is recommended to use a switch in series with the pull-up resistor to reduce the standby current and use the pull-up resistor R_{PU} less than 15 kΩ.

Short-to-Battery Fault

The TPS42Q20 integrates the short-to-battery fault detection, which has the same operating mechanism and behavior as the open-load detection.

In the ON state with the INx high, the reverse current, caused by the short-to-battery fault, flows through the internal MOSFET and leads to small power dissipation on the device.

In the OFF state with the INx low, the short-to-battery fault is reported when V_{OUTx} is greater than V_{VS}, but the reverse current is determined by the voltage difference between V_{OUTx} and V_{VS}. When $V_{OUTx} - V_{VS} < V_F$, there is no reverse current. When $V_{OUTx} - V_{VS} > V_F$, reverse current occurs. Please note that the reverse current should be less than I_{REV} to prevent the device from damage.

Reverse-Polarity Fault

The TPS42Q20 integrates the reverse-polarity fault detection, which has the same operating mechanism and behavior as the open-load detection.

In the ON state with the INx high, the reverse current, caused by the reverse polarity, flows through the internal MOSFET and leads to small power dissipation on the device.

In the OFF state with the INx low, reverse-polarity is reported and the reverse current flows through the body diode, which will cause high power dissipation. Please note that the reverse current should be less than I_{REV} to prevent the device from damage.

Reverse-Current Protection

Either the short-to-battery fault or the reverse-polarity fault will cause the reverse current to flow through the device. Usually, there are two methods to block the reverse current.

1. Add a block diode between the power supply and the VS pin. With this method, both the device and load are protected from the reverse current fault.
2. Add a ground network between the GND pin and the system ground. It is recommended to use an I_F > 100mA diode and a 4.7-kΩ resistor in parallel in the ground network. With this method, only the TPS42Q20 device is protected from the reverse current fault, and the load is protected by itself.

Please note, when the ground network is used, the R_{ICL} must be connected to the GND pin directly.

Loss-of-Ground Protection

The TPS42Q20 turns off the output when the loss-of-ground fault occurs, no matter whether the IN-pin signal is high or low.

Loss-of-Power Supply Protection

The TPS42Q20 turns off the output when the loss-of-power fault occurs, no matter whether the IN-pin signal is high or low. When a loss-of-power fault occurs, the inductive load will still sink current from all pins connected. It is recommended to use the ground network or a freewheeling diode to prevent damage from negative voltage.

Over-Temperature Fault and Protection

The TPS42Q20 integrates two mechanisms for over-temperature diagnosis and protection: thermal shutdown and thermal swing.

When the junction temperature T_J rises above the thermal shutdown threshold T_{SD}, thermal shutdown works and turns off the output immediately. When the device cools down and the junction temperature falls below T_{SD} − T_{HYS}, the output turns on again. In the thermal shutdown condition, the $\overline{STx}$ pin of TPS42Q20A is pulled down and the CS pin of TPS42Q20B is pulled up to $V_{CS,H}$, and the current limit is reduced to $I_{LIM,STD}$ or half of the set value to prevent the device from repeating thermal shutdown. The thermal shutdown fault signal and the reduced current limit will not be reset until the junction temperature decreases below $T_{SD,RST}$.

When the MOSFET junction temperature T_{MOS} rises much more quickly than the logic control module junction temperature T_{LOGIC} and the temperature difference $\Delta T = T_{MOS} - T_{LOGIC} > T_{SW}$, the thermal swing works and turns off the output immediately. When the MOSFET cools down and the temperature difference $\Delta T = T_{MOS} - T_{LOGIC} < T_{SW}T_{HYS}$, the output turns on again. In the thermal swing condition, the $\overline{STx}$ pin of TPS42Q20A is pulled down and the CS pin of TPS42Q20B is pulled up to $V_{CS,H}$. The thermal swing fault signal automatically resets after the device recovers from the thermal swing condition.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPS42Q20 is a 160-mΩ 4-channel high-side power switch product. The following application schematic shows a typical usage of the TPS42Q20 series.

Typical Application

Figure 17 shows the typical protection application schematic of the TPS42Q20.

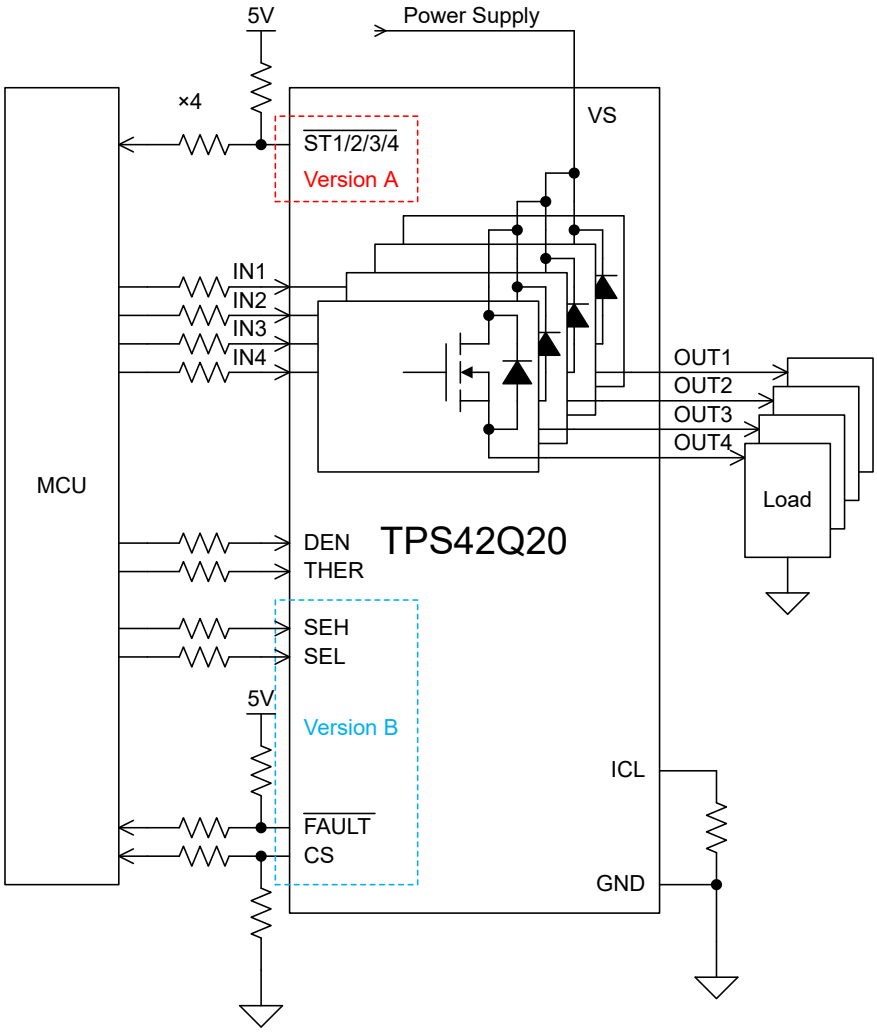


Figure 17. Typical Application Circuit

Power Dissipation

During normal operation, the junction temperature should meet the requirements in the Recommended Operating Conditions table. Use Equation 4 and Equation 5 to calculate the power dissipation and estimate the junction temperature.

The power dissipation (P_D) can be calculated using Equation 4.

$$P_D = \left(I_{OUT1}^2 + I_{OUT2}^2 + I_{OUT3}^2 + I_{OUT4}^2\right) \times R_{ON} + V_S \times I_Q \quad (4)$$

Where,

- I_{OUTx} is the output current of each channel,
- R_{ON} is the turn-on resistance,
- V_S is the VS pin power supply voltage,
- I_Q is the quiescent current.

The junction temperature (T_J) can be estimated using Equation 5.

$$T_J = T_A + P_D \times \theta_{JA} \quad (5)$$

Where,

- T_A is the ambient temperature,
- P_D is the power dissipation,
- θ_{JA} is the junction-to-ambient thermal resistance.

Layout

Layout Guideline

To get good thermal performance and prevent over-temperature protection, the PCB layout is important. A well-designed PCB layout can effectively optimize heat dissipation, which is crucial for ensuring the long-term reliability of the device.

- It is recommended to maximize the coverage of copper on the PCB to enhance the thermal conductivity of the board. Since the primary heat flow path from the package to the surrounding environment passes through the copper on the PCB, having maximum copper coverage is particularly important when there is no heat sink attached to the opposite side of the board.
- It is recommended to place as many thermal vias as possible underneath the package ground pad to optimize the thermal conductivity of the board.
- It is suggested that all thermal vias be either plated shut or plugged and capped on both sides of the board to prevent solder voids to maintain reliability and performance.
- It is recommended to use wide traces or thick copper weight in the input/output current paths to minimize I×R voltage drop.

Layout Example

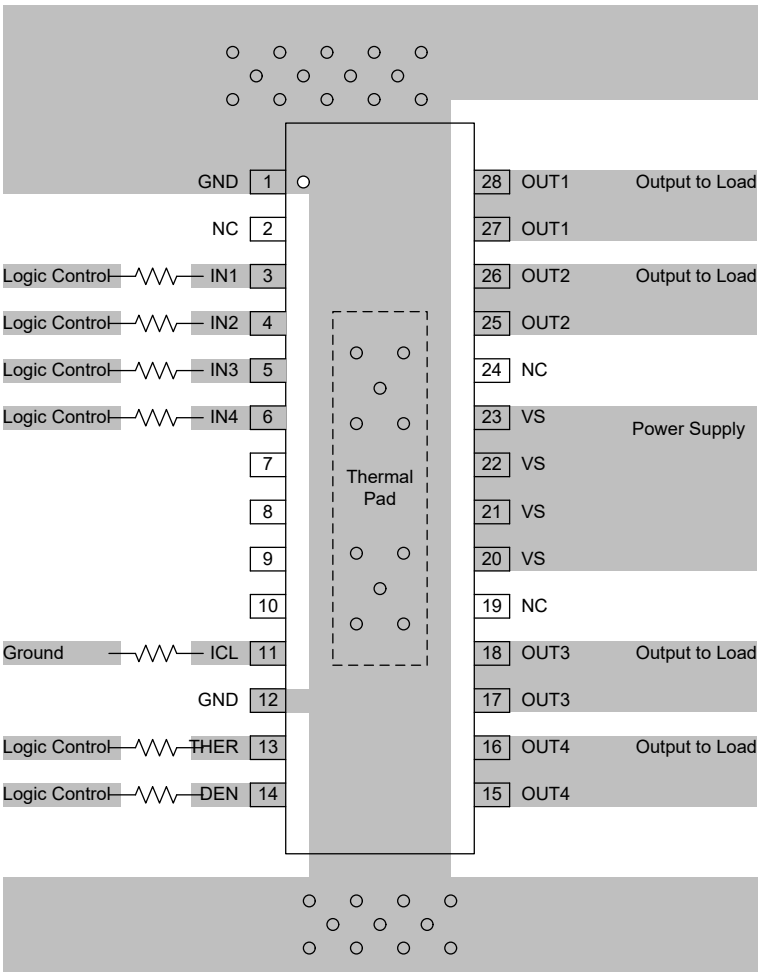


Figure 18. Layout Example

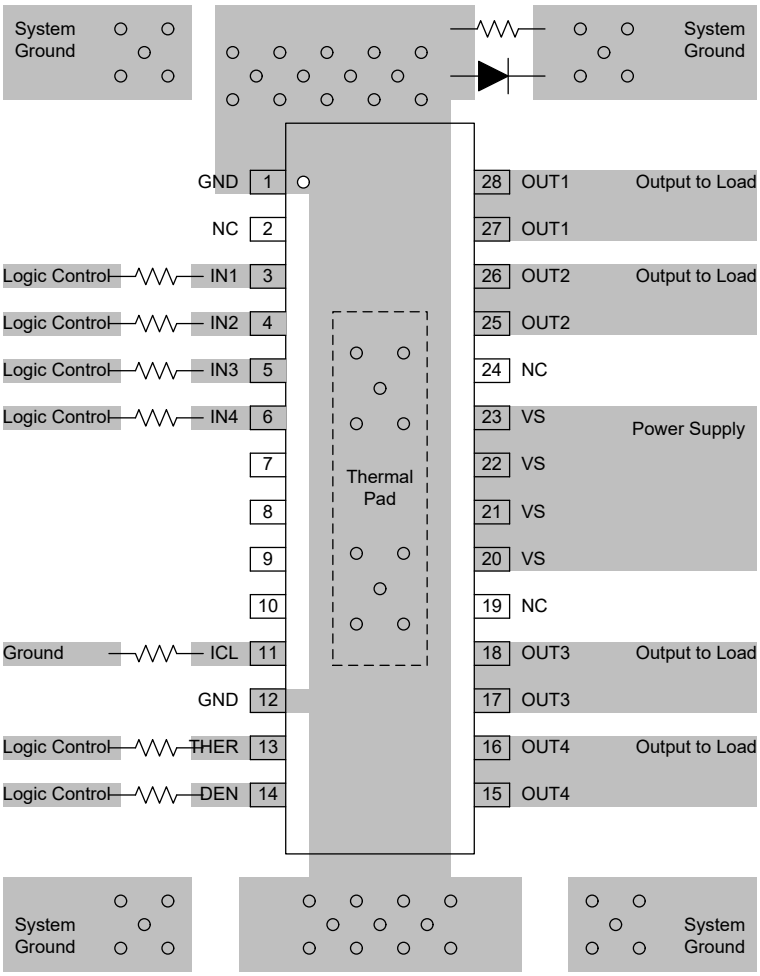
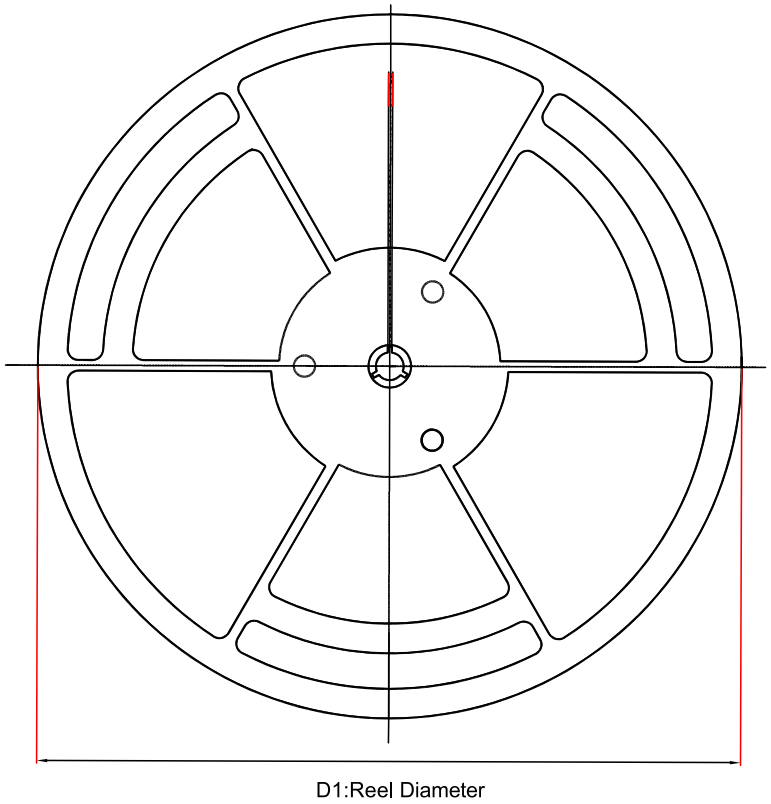
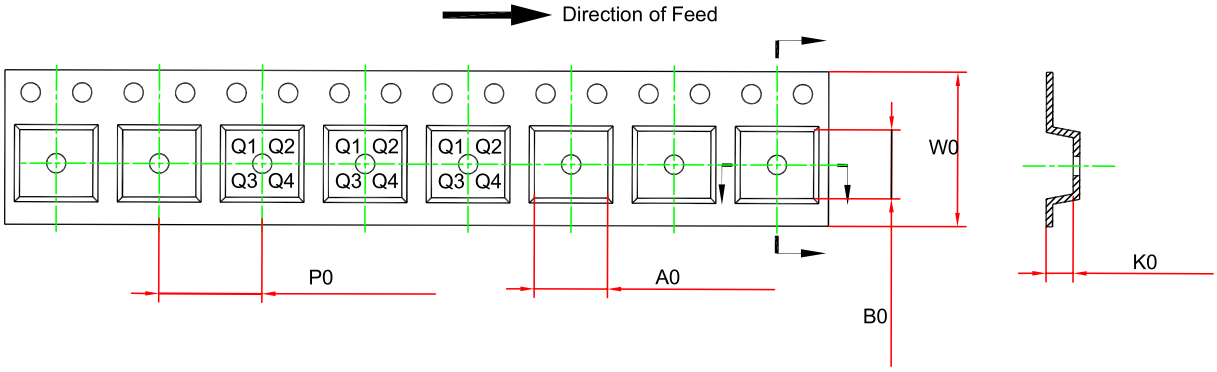


Figure 19. Layout Example with a Ground Network

Tape and Reel Information



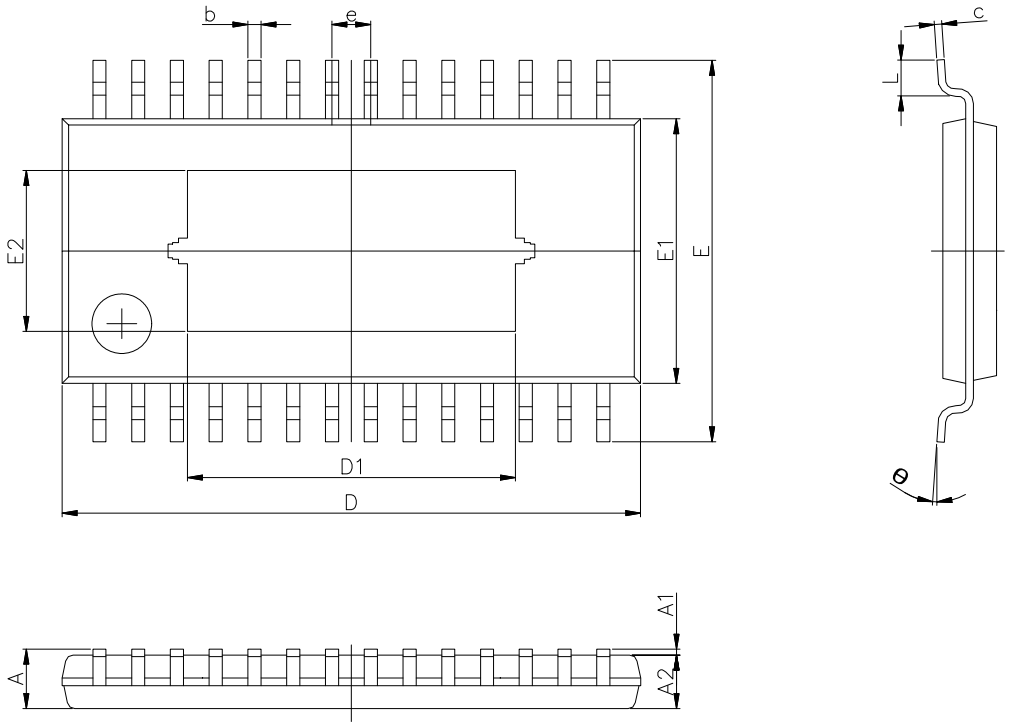


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPS42Q20A-TSCR-S	ETSSOP28	330	21.6	6.9	10.2	1.5	12	16	Q1
TPS42Q20B-TSCR-S	ETSSOP28	330	21.6	6.9	10.2	1.5	12	16	Q1

Package Outline Dimensions

ETSSOP-28

Package Outline Dimensions TSC(ETSSOP-28-D)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	---	1.200	---	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
D1	3.510	3.760	0.138	0.148
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
E2	2.500	2.700	0.098	0.106
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

NOTES
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPS42Q20A-TSCR-S	−40 to 125°C	ETSSOP28	SQ20A	MSL3	2,500	Green
TPS42Q20B-TSCR-S	−40 to 125°C	ETSSOP28	SQ20B	MSL3	2,500	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

Disclaimer. 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.

This page intentionally left blank