5-A E-fuse Protection Switches with Inrush Control

Features

- TPS14P50: 12-V E-fuse
  - 15-V Over-Voltage Clamp
- TPS05P50: 5-V E-fuse
  - 6.1-V Over-Voltage Clamp
- 27-mΩ Low Turn-On Resistance
- 5-A Maximum Continuous Current
  - 2-A to 5-A Adjustable Current Limit
  - ±15% Adjustable Current Limit Accuracy
- Adjustable Output Voltage Slew Rate
- Adjustable Undervoltage Lock Out
- Integrated Inrush Control
- Protection:
  - Over-Current Protection
  - Short-to-Ground Protection
  - Over-Temperature Protection
- Temperature Range: −40°C to 125°C
- Package Options:
  - DFN3X3-10

Applications

- Hotswap Protection
- HDD and SSD Driver Card
- PCIe Cards
- Server Fan Power Supply

Description

The TPS14P50 and TPS05P50 are 5-A e-fuse switches with voltage clamp and current limit protection functions integrated. The TPS14P50 integrates a 15-V over-voltage clamp and the TPS05P50 integrates a 6.1-V over-voltage clamp. The over-voltage clamp function can limit the output voltage during the input voltage surge to protect the load from damage. The TPS14P50 and TPS05P50 integrate an adjustable current limit function. The current limit level can be set from 2 A to 5 A by connecting an external resistor at the ILIM pin and the current limit accuracy is ±15% typically.

To limit the inrush current and meet the output voltage smoothly ramp up requirement, the TPS14P50 and TPS05P50 integrate a soft-start function, which can be adjusted by a capacitor connected at the dVdt pin.

Both of the TPS14P50 and the TPS05P50 products are guaranteed to operate in the ambient temperature range from −40°C to +125°C. Additionally, both products provide the thermal-enhanced DFN3X3-10 package to enable sustained operation despite significant dissipation across the device.

Typical Application Circuit

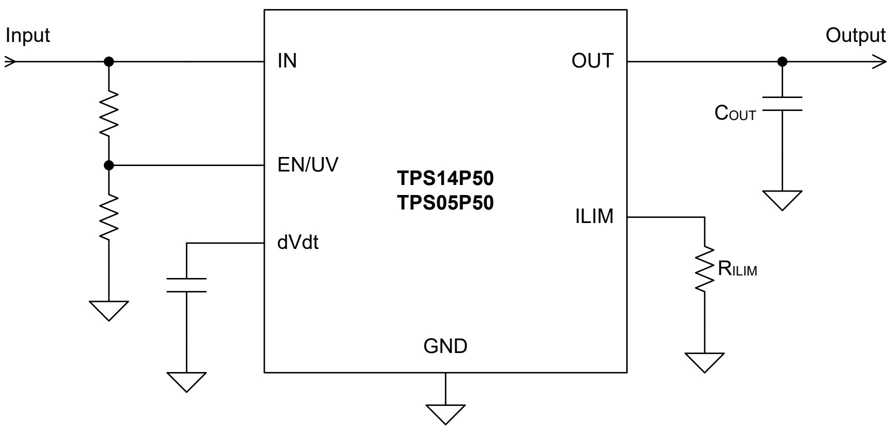


Table of Contents

Features 1
Applications 1
Description 1
Typical Application Circuit 1
Product Family Table 3
Revision History 3
Pin Configuration and Functions 4
Specifications 5
Absolute Maximum Ratings (1) 5
ESD, Electrostatic Discharge Protection 5
Recommended Operating Conditions 5
Thermal Information 6
Electrical Characteristics 7
Typical Performance Characteristics 9
Detailed Description 14
Overview 14
Functional Block Diagram 14
Feature Description 14
Application and Implementation 17
Application Information 17
Typical Application 17
Layout 19
Layout Guideline 19
Layout Example 19
Tape and Reel Information 20
Package Outline Dimensions 22
DFN3X3-10-A 22
Order Information 23
IMPORTANT NOTICE AND DISCLAIMER 24

Product Family Table

Order Number	Over-Voltage Clamp (V)	Fault Response	Package
TPS14P50A-DF8R	15	Auto Retry	DFN3X3-10
TPS14P50B-DF8R	15	Latched	DFN3X3-10
TPS05P50A-DF8R	6.1	Auto Retry	DFN3X3-10
TPS05P50B-DF8R	6.1	Latched	DFN3X3-10

Revision History

Revision	Notes
Rev.Pre.0	Preliminary datasheet.
Rev.Pre.1	Added Typical Performance Characteristics, Functional Block Diagram, and Feature Description.
Rev.A.0	Initial Released.

Pin Configuration and Functions

TPS14P50 and TPS05P50
DFN3X3-10 Package
Top View

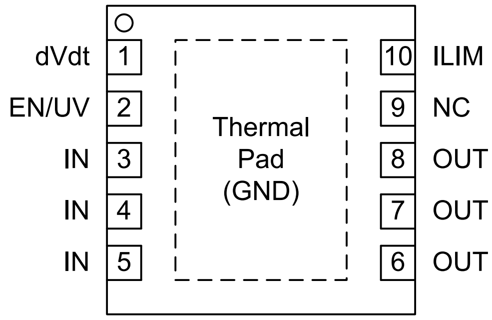


Table 1. Pin Functions: TPS14P50 and TPS05P50

Pin No.	Pin Name	I/O	Description
dVdt	1	O	Output voltage ramp up slew rate control pin. Connect a capacitor from this pin to ground to set the output voltage ramp-up slew rate.
EN/UV	2	I	Device enable and UVLO set pin. Pull this pin to HIGH or Low to enable or disable the device output. Connect a resistor divider to set the UVLO threshold.
GND	Thermal Pad	-	Ground reference pin. MUST connect this pin the to the PCB ground plane directly.
ILIM	5	O	Output current limit adjust pin. Connect a resistor from this pin to the ground to set the current limit threshold.
IN	3, 4, 5	I	Input power supply voltage pin. Suggest connecting a 0.1 μF or greater ceramic capacitor from IN to GND closely by the device.
NC	9	-	No internal connection.
OUT	6, 7, 8	O	Output voltage pin. Output capacitor is not required. 3PEAK suggests adding a 1 μF or greater ceramic capacitor from this pin to ground to improve transient performance.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
IN	Input Supply Voltage	−0.3	20	V
IN	Transient Input Supply Voltage (< 1 ms)	−0.3	22	V
OUT	Output Voltage	−0.3	20	V
OUT	Transient Output Voltage (< 1 µs)	−1.2		V
dVdt		−0.3	7	V
EN/UV		−0.3	7	V
ILIM		−0.3	7	V
T_J	Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.
(3) Not subject to production test, specified by design.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{IN}	TPS14P50	4.5	12	14	V
V_{IN}	TPS05P50	4.5	5	5.5	V
V_{dVdt}		0		6	V
C_{dVdt}	Output Capacitor ESR Requirements		1	1000	nF
$V_{EN/UV}$		0		6	V
V_{ILIM}		0		3	V
R_{ILIM}	Current Limit Resistor	10		162	kΩ
I_{OUT}	Continuous Output Current	1		5	A
C_{OUT}	Output Capacitor Requirements	0.1	1	1000	µF

Parameter		Min	Typ	Max	Unit
T_J	Junction Temperature	−40		125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
DFN3X3-10	46.5	14.4	47.6	°C/W

Electrical Characteristics

All test conditions: V_{IN} = 12 V for TPS14P50, V_{IN} = 5 V for TPS05P50, $V_{EN/UV}$ = 2 V, R_{LIM} = 100 kΩ, C_{dVdT} = OPEN, T_J = −40°C to 125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
UVLO	V_{IN} Under-Voltage Lockout Threshold	V_{IN} rising, $V_{EN/UV}$ = 2 V, I_{OUT} = 10 mA	4.15	4.3	4.49	V
	Hysteresis			350		mV
I_Q	Quiescent Current, TPS14P50	$V_{EN/UV}$ = 2 V, I_{OUT} = 0 mA		0.5	0.8	mA
	Quiescent Current, TPS05P50	$V_{EN/UV}$ = 2 V, I_{OUT} = 0 mA		0.5	0.8	mA
I_{SD}	Shutdown Current	$V_{EN/UV}$ = 0 V		0.1	0.2	mA
V_{OVC}	Over-Voltage Clamp	V_{IN} > 16.5V, I_{OUT} = 10mA, TPS14P50	13.8	15	16.5	V
		V_{IN} > 5.5V, I_{OUT} = 10mA, TPS05P50	5.5	6.1	6.75	V
Enable/UVLO Voltage and Current						
$V_{IH,EN/UV}$	EN/UV Logic Input High (Enable)		1.37	1.4	1.50	V
$V_{IL,EN/UV}$	EN/UV Logic Input Low (Disable)		1.32	1.35	1.40	V
$I_{EN/UV}$	EN/UV Pin Leakage Current	V_{EN} = 0 V to 5 V	−0.1		0.1	μA
dVdt Output Ramp-Up Control						
I_{dVdt}	dVdt Charging Current	Force V_{dVdt} = 0 V		220		nA
R_{dVdt}	dVdt Discharging Resistance	$V_{EN/UV}$ = 0 V, force 10 mA to dVdt	90	130	170	Ω
V_{dVdt}	dVdt Maximum Capacitor Voltage			1.2		V
Output Power MOSFET						
R_{ON}	Turn-On Resistance	T_J = 25°C	24	27	31	mΩ
		T_J = −40 to 125°C	15	27	40	mΩ
$I_{OUT-OFF}$	OUT Bias Current in OFF Status	$V_{EN/UV}$ = 0 V, V_{OUT} = 0 V	−5	0	1.2	μA
		$V_{EN/UV}$ = 0 V, V_{OUT} = 300 mV	100	137	190	μA
Output Current						
I_{ILIM}	ILIM Bias Current			10		μA
I_{OL}	OUT Over-Load Current Limit	R_{ILIM} = 45.3 kΩ, V_{IN-OUT} = 1 V	2.0	2.3	2.6	A
		R_{ILIM} = 100 kΩ, V_{IN-OUT} = 1 V	3.45	3.75	4.05	A
		R_{ILIM} = 150 kΩ, V_{IN-OUT} = 1 V	4.8	5.1	5.4	A
$I_{ILIM,SC}$	ILIM Short Current Limit	R_{ILIM} = 0 Ω		0.9		A
$I_{ILIM,OP}$	ILIM Open Current Limit	R_{ILIM} = open		0.9		A
$V_{ILIM,OP}$	ILIM Open Sense Threshold	R_{ILIM} = open, V_{ILIM} rising		3.1		V

Parameter		Conditions	Min	Typ	Max	Unit
I_{SC}	OUT Short-Circuit Current Limit (1)	R_{ILIM} = 45.3 kΩ, V_{IN-OUT} = 5 V, TPS05P50		2.05		A
		R_{ILIM} = 45.3 kΩ, V_{IN-OUT} = 12 V, TPS14P50		1.98		A
		R_{ILIM} = 100 kΩ, V_{IN-OUT} = 5 V, TPS05P50		3.56		A
		R_{ILIM} = 100 kΩ, V_{IN-OUT} = 12 V, TPS14P50		3.32		A
		R_{ILIM} = 150 kΩ, V_{IN-OUT} = 5 V, TPS05P50		4.95		A
		R_{ILIM} = 150 kΩ, V_{IN-OUT} = 12 V, TPS14P50		4.5		A
Ratio	Ratio of Fast-Trip Current Limit and Over-Load Current Limit	$\frac{I_{FAST\_TRIP}}{I_{IL}}$		1.6		
Temperature Range						
T_{SD}	Thermal shutdown threshold			150		°C
	Thermal shutdown hysteresis			10		°C
Timing						
$t_{ON,DLY}$	Turn-On Delay Time	EN/UV↑ to V_{OUT} = 10% × V_{IN}		220		μs
$t_{OFF,DLY}$	Turn-Off Delay Time	EN/UV↓ to V_{OUT} = 90% × V_{IN}		0.4		μs
t_{dVdt}	Output Ramp-Up Time	C_{dVdt} = 0, V_{IN} = 5 V, EN/UV↑ to V_{OUT} = 90% × V_{IN}, TPS05P50		0.4		ms
		C_{dVdt} = 0, V_{IN} = 12 V, EN/UV↑ to V_{OUT} = 90% × V_{IN}, TPS14P50		0.4		ms
		C_{dVdt} = 1 nF, V_{IN} = 5 V, EN/UV↑ to V_{OUT} = 90% × V_{IN}, TPS05P50		5		ms
		C_{dVdt} = 1 nF, V_{IN} = 12 V, EN/UV↑ to V_{OUT} = 90% × V_{IN}, TPS14P50		5		ms
$t_{FAST,DLY}$	Fast-Trip Off Delay Time	I_{OUT} > $I_{FASTRIP}$ to I_{OUT} = 0		300		ns
$t_{TSD,DLY}$	Thermal Shutdown Recovery Delay Time (auto retry version)	V_{IN} = 5 V, TPS05P50		240		μs
		V_{IN} = 12 V, TPS14P50		240		μs

Typical Performance Characteristics

All test conditions: V_{IN} = 12 V for TPS14P50, V_{IN} = 5 V for TPS05P50, $V_{EN/UV}$ = 2 V, R_{LIM} = 100 kΩ, C_{IN} = 0.1 μF, C_{OUT} = 1 μF, C_{dVdT} = OPEN, T_J = 25°C, unless otherwise noted.

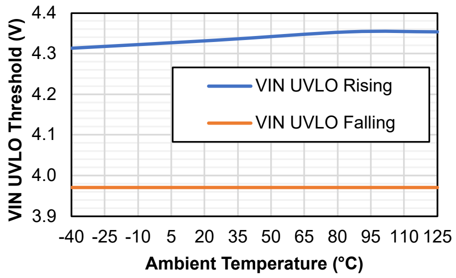


Figure 1. Supply Input UVLO vs Temperature

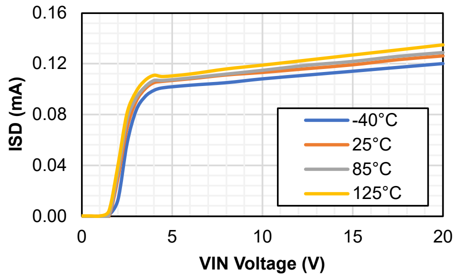
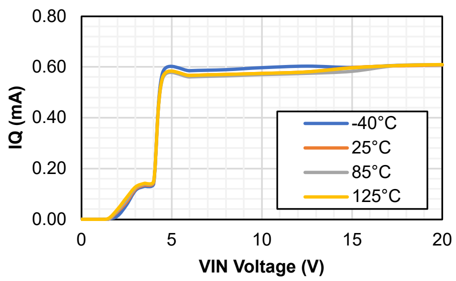
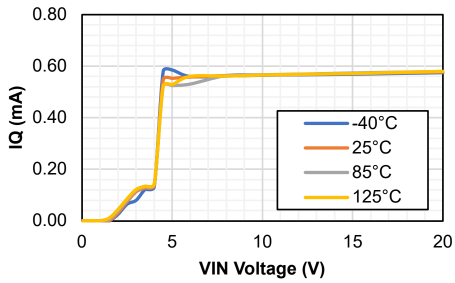


Figure 2. Shutdown Current vs Supply Voltage



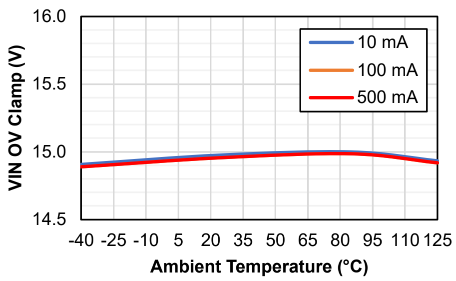
TPS14P50

Figure 3. Quiescent Current vs Supply Voltage



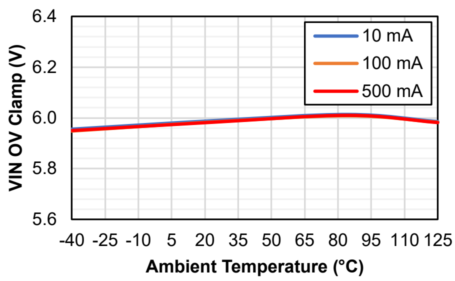
TPS05P50

Figure 4. Quiescent Current vs Supply Voltage



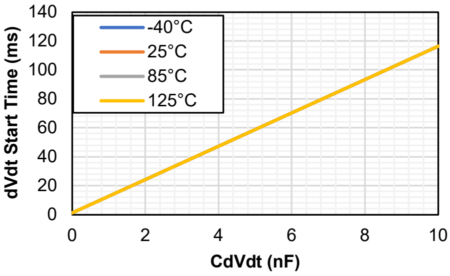
TPS14P50

Figure 5. Output Voltage Clamp vs Supply Voltage



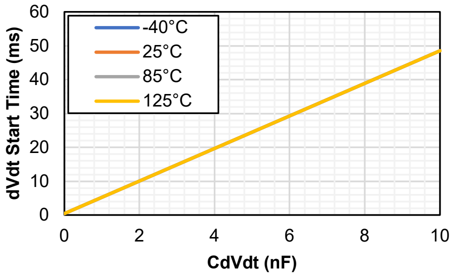
TPS05P50

Figure 6. Output Voltage Clamp vs Supply Voltage



TPS14P50

Figure 7. Soft-Start Time vs Capacitance



TPS05P50

Figure 8. Soft-Start Time vs Capacitance

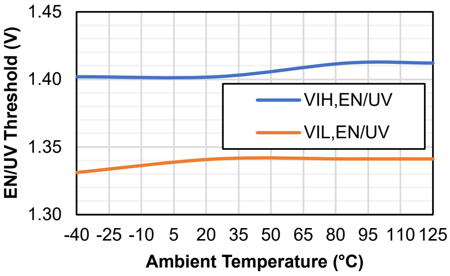


Figure 9. EN/UV Threshold vs Temperature

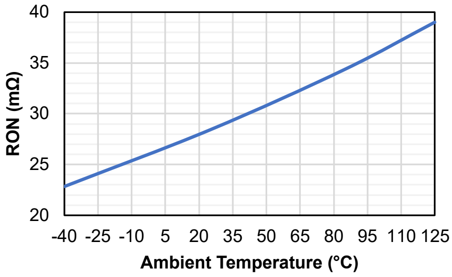
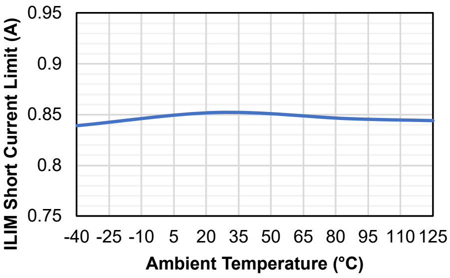
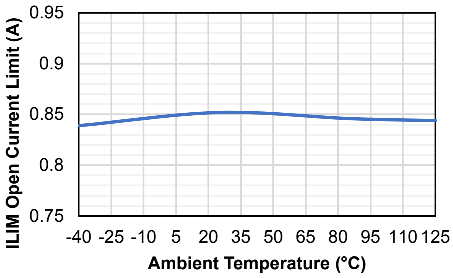


Figure 10. R_{ON} vs Temperature



R_{ILIM} = 0

Figure 11. ILIM Short Current Limit vs Temperature



R_{ILIM} = OPEN

Figure 12. ILIM Open Current Limit vs Temperature

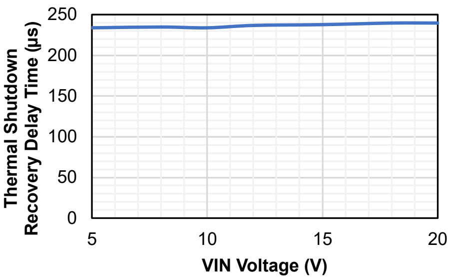
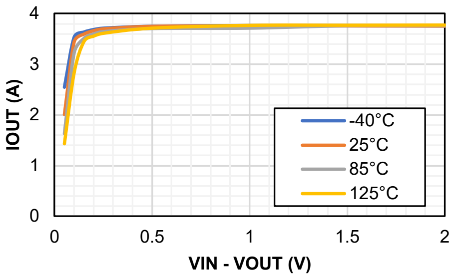
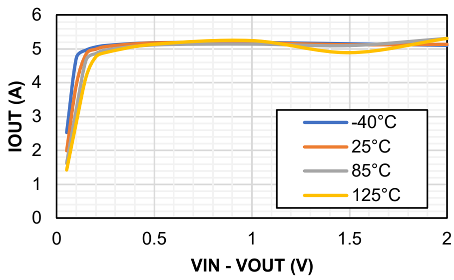


Figure 13. Thermal Shutdown Auto Retry Delay Time vs Supply Voltage



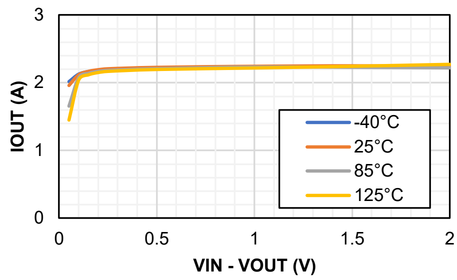
R_{LIM} = 100 kΩ

Figure 14. I_{OUT} vs $V_{IN} - V_{OUT}$



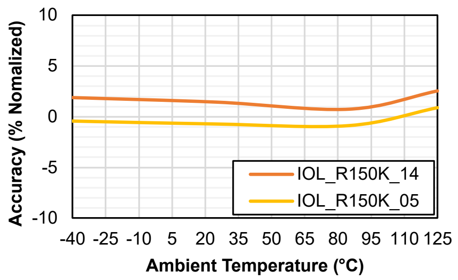
R_{LIM} = 150 kΩ

Figure 15. I_{OUT} vs V_{IN} − V_{OUT}



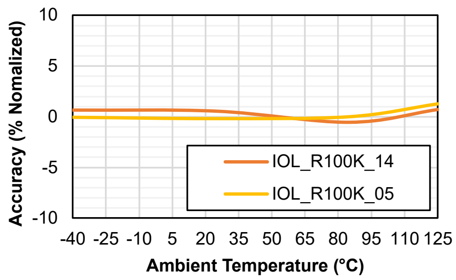
R_{LIM} = 45.3 kΩ

Figure 16. I_{OUT} vs V_{IN} − V_{OUT}



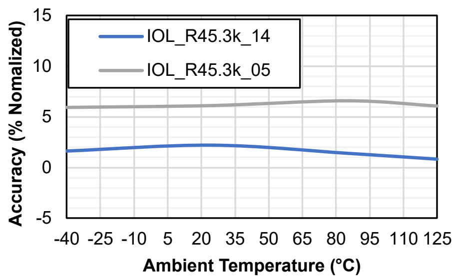
R_{LIM} = 150 kΩ

Figure 17. Over-Load Accuracy vs Temperature



R_{LIM} = 100 kΩ

Figure 18. Over-Load Accuracy vs Temperature



R_{LIM} = 45.3 kΩ

Figure 19. Over-Load Accuracy vs Temperature

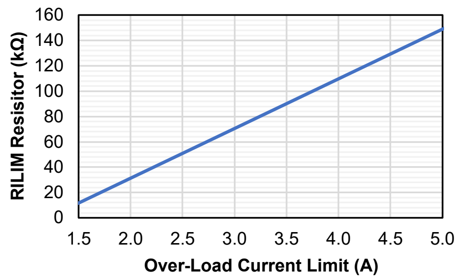
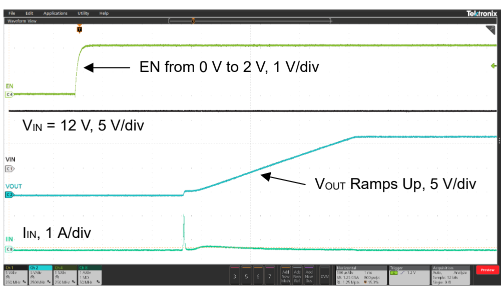
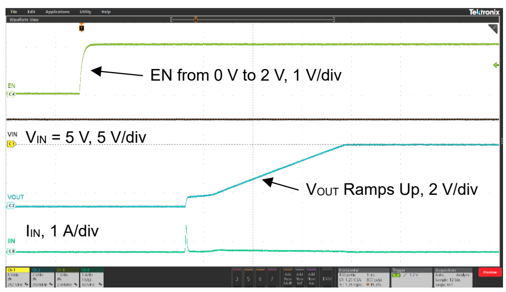


Figure 20. RLIM Resistor vs Over-Load Current Limit



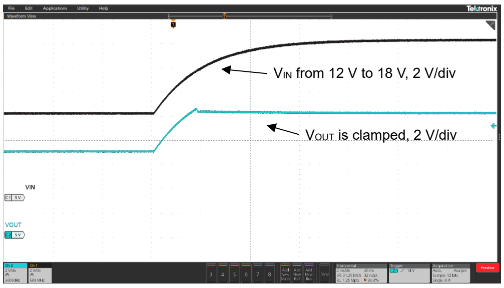
TPS14P50, C_{dVdt} = 4.7 µF, C_{OUT} = 4.7 µF

Figure 21. Startup with EN/UV



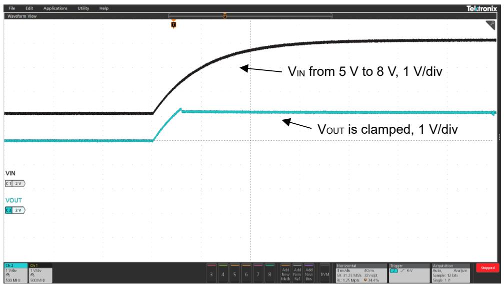
TPS05P50, C_{dVdt} = 4.7 µF, C_{OUT} = 4.7 µF

Figure 22. Startup with EN/UV



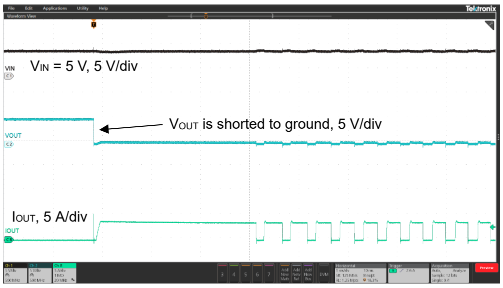
TPS14P50

Figure 23. Over-Voltage Clamp



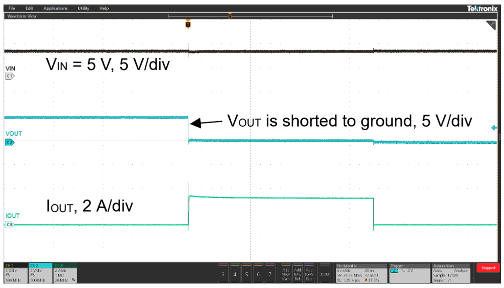
TPS05P50

Figure 24. Over-Voltage Clamp



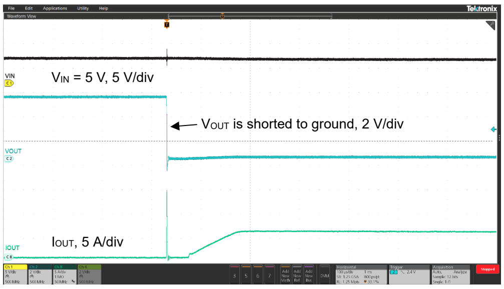
Auto-Retry Version

Figure 25. Thermal Shutdown Auto Retry



Latch Version

Figure 26. Thermal Shutdown Latch



V_{IN} = 5 V, R_{LIM} = 150 kΩ

Figure 27. Output Short to Ground

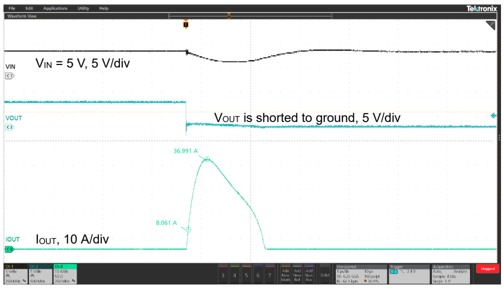


Figure 28. Output Short to Ground

Figure 29. Enabled with Output Short to Ground

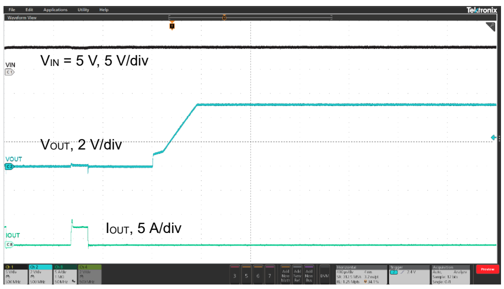
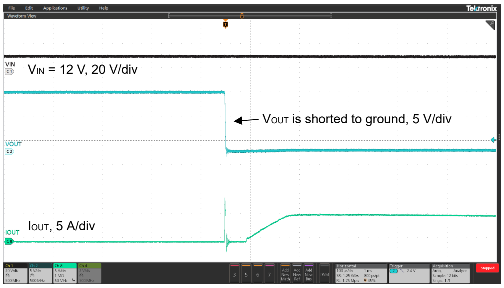


Figure 30. Recovery from Short to Ground



V_{IN} = 12 V, R_{LIM} = 150 kΩ

Figure 31. Output Short to Ground

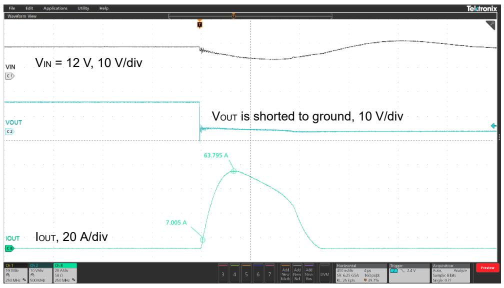


Figure 32. Output Short to Ground

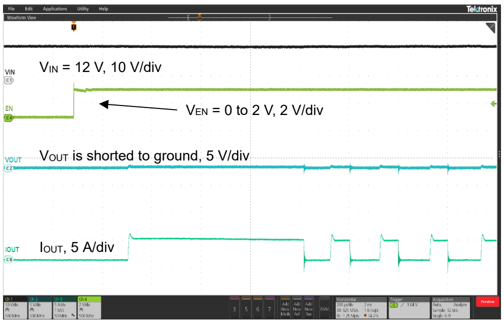


Figure 33. Enabled with Output Short to Ground

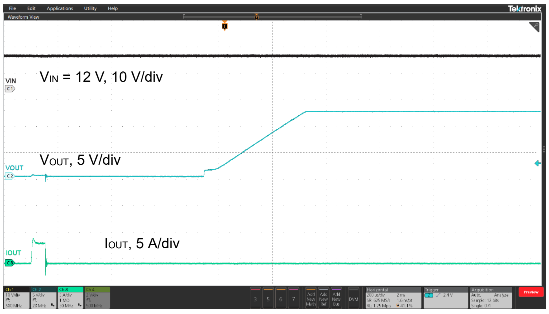


Figure 34. Recovery from Short to Ground

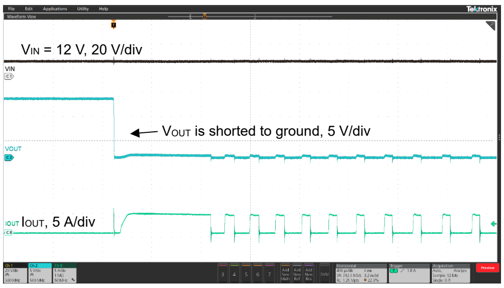
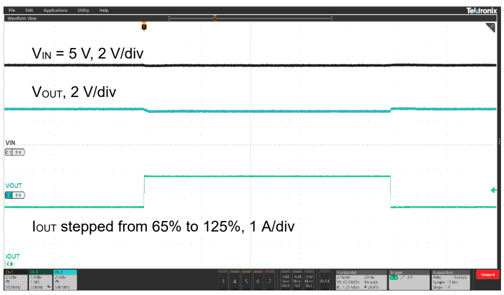


Figure 35. Thermal Shutdown Auto Retry



Load Stepped from 65% to 125%, back to 65%.

Figure 36. Over-Load Current Limit

Detailed Description

Overview

The TPS14P50 and TPS05P50 are 5-A e-fuse switches with voltage clamp and current limit protection functions integrated. The TPS14P50 integrates a 15-V over-voltage clamp and the TPS05P50 integrates a 6.1-V over-voltage clamp. The over-voltage clamp function can limit the output voltage during the input voltage surge to protect the load from damage. The TPS14P50 and TPS05P50 integrate an adjustable current limit function. The current limit level can be set from 2 A to 5 A by connecting an external resistor at the ILIM pin and the current limit accuracy is ±15% typically.

To limit the inrush current and meet the output voltage smoothly ramp-up requirement, the TPS14P50 and TPS05P50 integrate a soft-start function, which can be adjusted by a capacitor connected at the dVdt pin.

Functional Block Diagram

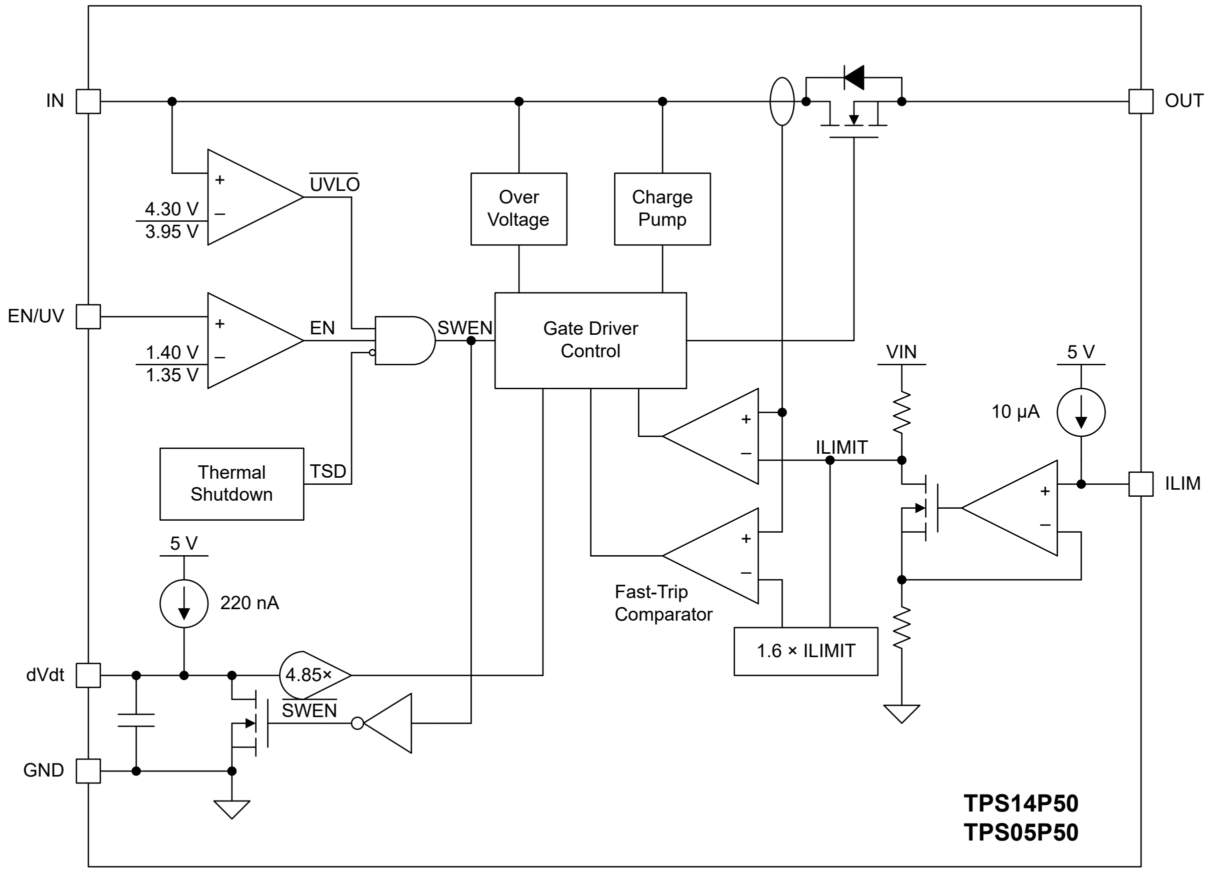


Figure 37. Functional Block Diagram

Feature Description

Under-Voltage Lockout (UVLO)

The TPS14P50 and TPS05P50 have two methods of controlling undervoltage lockout (UVLO): using V_{IN} UVLO threshold or using $V_{EN/UV}$ with external resistor divider.

For the $V_{EN/UV}$ threshold, it is adjustable with external resistor dividers R1 and R2. The value could be calculated with Equation 1 and Equation 2.

$$V_{UV,R} = \frac{R1 + R2}{R1} \times V_{IH,EN/UV} \quad (1)$$

$$V_{UV,F} = \frac{R1 + R2}{R1} \times V_{IL,EN/UV} \quad (2)$$

Where $V_{IH,EN/UV}$ is the rising threshold and $V_{IL,EN/UV}$ is the falling threshold. R1 and R2 are the resistors connected between IN, EN/UV and GND pins of the device.

The current through R1 and R2 could be calculated with Equation 3. The resistor value should be selected according to the leakage current from V_{IN}. It is suggested to set current $I_{R1,R2}$ to be 20 times greater than the EN/UV pin leakage current ($I_{EN/UV}$).

$$I_{R1,R2} = \frac{V_{IN}}{R1 + R2} \quad (3)$$

For the V_{IN} UVLO threshold, refer to the Electrical Characteristics table for UVLO threshold and hysteresis. Please note, the EN/UV pin is rated only to 7 V maximum and it cannot be connected directly to $V_{IN} \geq 7$ V. Suggest connect R1 = 1 MΩ to limit the pull-up current below 20 µA when R2 is open.

Over-Voltage Clamp (OVC)

For both TPS14P50 and TPS05P50, the absolute maximum voltage rating of IN pin is 20 V, and the recommended V_{IN} operating voltage range is 4.5 V to 14 V and 4.5 V to 5.5 V for TPS05P50 respectively. However, when the VIN voltage is greater than the recommended operating voltage range, the device enters the over-voltage clamp (OVC) mode to limit the output voltage at VOVC.

In the OVC mode, the power dissipation could be calculated with Equation 4. Please note, the power dissipation could heat up the device and cause over-temperature protection.

$$P_{D,OVC} = (V_{IN} - V_{OVC}) \times I_{OUT} \quad (4)$$

Output Slew Rate Control (dVdt)

Both TPS14P50 and TPS05P50 support output slew rate control with the capacitor connected at the dVdt pin during device start up. The dVdt pin could be left open to use the inherent slew rate. When the dVdt capacitor is connected, the total output ramp-up time could be calculated with Equation 5.

$$t_{dVdt} = \frac{V_{dVdt} \times V_{IN}}{I_{dVdt} \times GAIN} \times (C_{dVdt} + C_{INT}) + t_{INT} \quad (5)$$

Where:

- V_{dVdt} = 1.2 V, which is the dVdt external capacitor voltage;
- I_{dVdt} = 220 nA, which is the dVdt external capacitor charging current;
- C_{dVdt} is the dVdt external capacitor;
- C_{INT} = 70 pF, which is the dVdt internal capacitor;
- t_{INT} = 220 µs, which is the internal delay time;
- GAIN is 6 V for TPS05P50 and 15 V for TPS14P50.

Output Current Limit (ILIM)

Both TPS14P50 and TPS05P50 use output current limit to protect the device during fault conditions, e.g., output is over loaded. The current limit value is set according to Equation 6.

$$I_{OL} = 0.7 + 3 \times 10^{-5} \times R_{LIM} \quad (6)$$

Both TPS14P50 and TPS05P50 integrate a fast-trip comparator to protect the device. When a transient short circuit event occurs, the current through the power MOSFET will rise quickly. The fast-trip comparator is much more responsive than the current-limit amplifier, and it shuts down the device when $I_{OUT} > I_{FAST\text{-}TRIP}$ and limits the maximum short-circuit current. The fast-trip trigger threshold, $I_{FAST\text{-}TRIP}$, is set to $1.6 \times I_{OL}$. After the fast-trip current limitation, the output current gradually ramps up to the I_{OL} controller by the current-limit amplifier,

When device is operating in current-limit mode, the internal power dissipation (see Power Dissipation) will raise the junction temperature rapidly, and ultimately lead to the over-temperature protection

Over-Temperature Protection

The recommended operating junction temperature range is from −40°C to 125°C. When the junction temperature is between 125°C and the thermal shutdown (TSD) threshold, the regulator can still work well but will reduce the device lifetime for long-term use.

The over-temperature protection works when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. When the device cools down and the junction temperature falls below the value, which equals to thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPS14P50 and TPS05P50 are 5-A e-fuse switches with voltage clamp and current limit protection features integrated. The following application schematic shows a typical usage of the TPS14P50 and TPS05P50.

Typical Application

Figure 38 shows the typical application schematic of the TPS14P50 and TPS05P50.

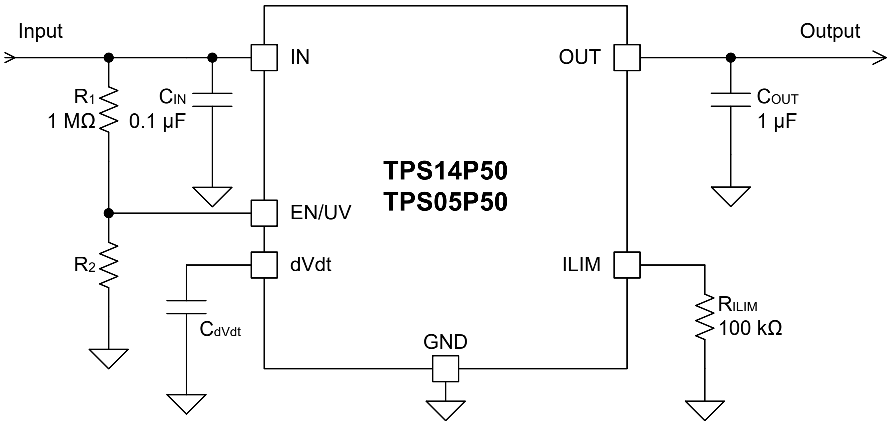


Figure 38. Typical Application Circuit

Input Capacitor and Output Capacitor

3PEAK recommends adding a 0.1 µF or grater ceramic capacitor closely at the IN pin to decouple the local noise and improve the transient performance. The voltage rating of the capacitors must be greater than the maximum input voltage.

The TPS14P50 and TPS05P50 are capacitor-free at the output. However, 3PEAK recommends adding a 1 µF or grater capacitor at the output pin to eliminate the undershoot during the large load transient condition.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, the junction temperature should meet the requirement in the Recommended Operating Conditions table. Use Equation 7 and Equation 8 to calculate the power dissipation and estimate the junction temperature.

The power dissipation (P_D) can be calculated using Equation 7.

$$P_D = I_{OUT}^2 \times R_{ON} + V_{IN} \times I_Q \tag{7}$$

Where,

- I_{OUT} is the output current,

- R_{ON} is the turn-on resistance,
- V_{IN} is the input supply voltage,
- I_Q is the quiescent current.

The junction temperature (T_J) can be estimated using Equation 8.

$$T_J = T_A + P_D \times \theta_{JA} \quad (8)$$

Where,

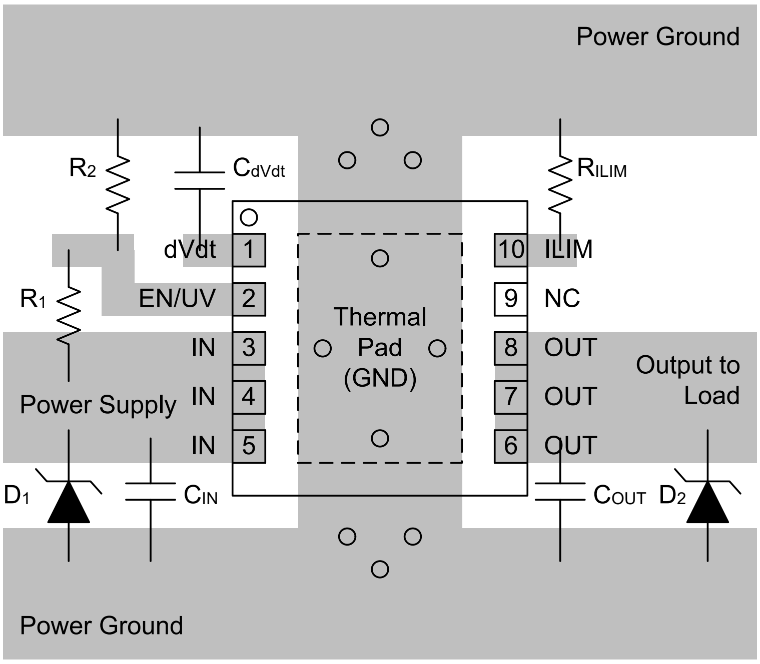
- T_A is the ambient temperature,
- P_D is the power dissipation,
- θ_{JA} is the junction-to-ambient thermal resistance.

Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed as close to the device pins as possible.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, IN pin, and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.

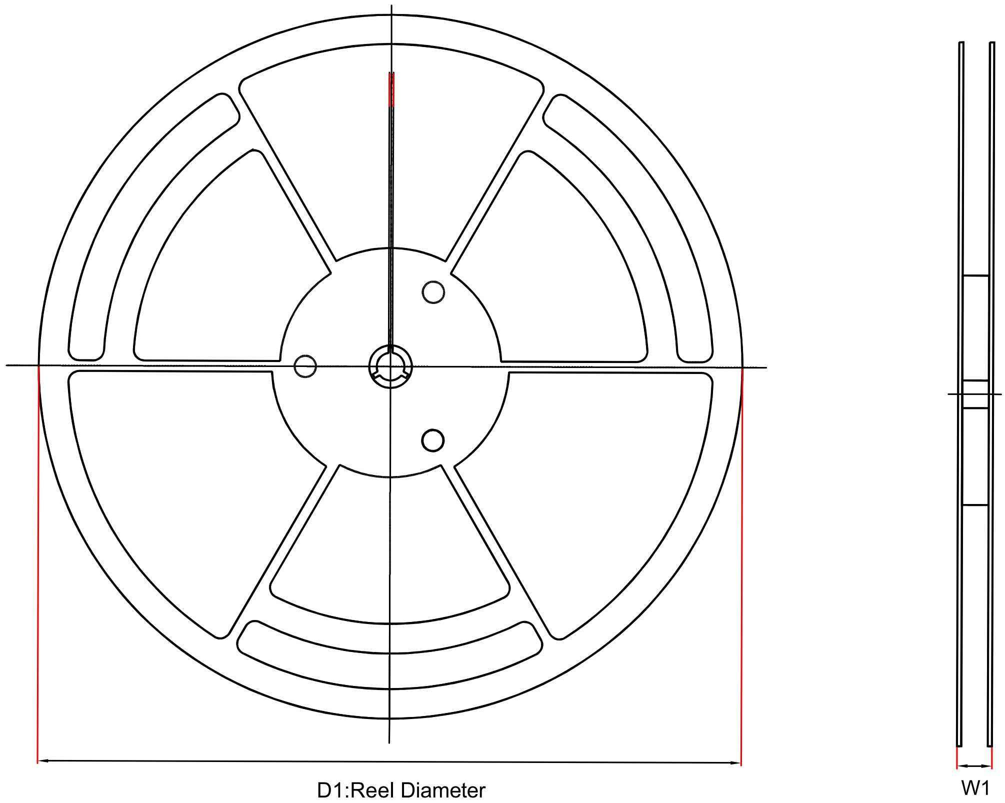
Layout Example

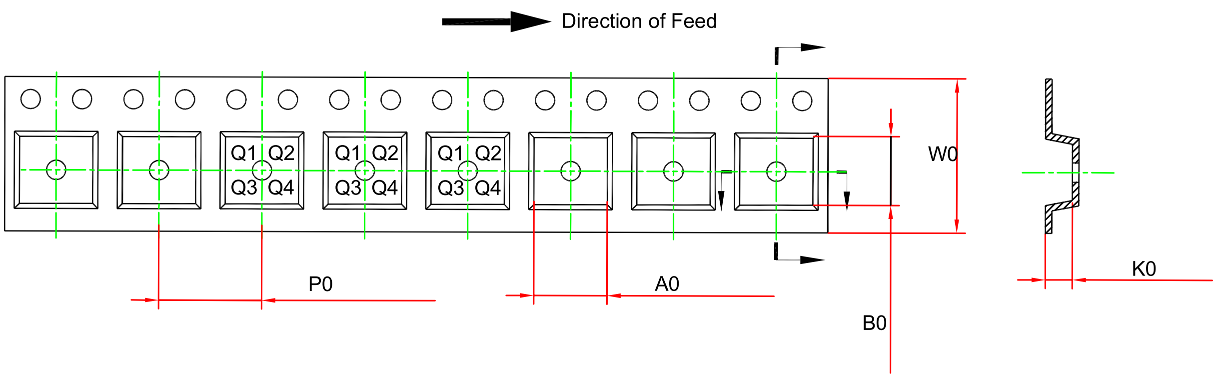


(1) D_1 and D_2 are only needed to suppress the transients caused by inductive load switching.

Figure 39. Layout Example

Tape and Reel Information





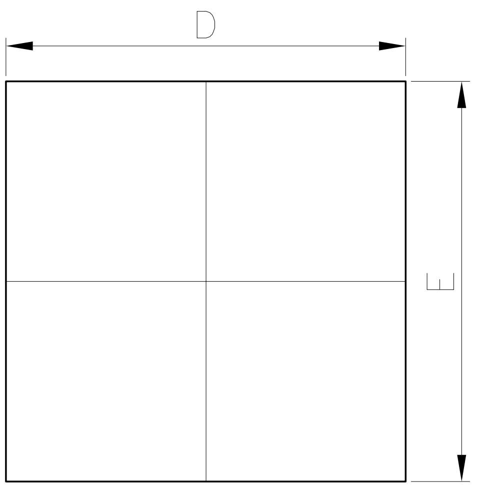
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPS05P50A-DF8R	DFN3X3-10	330	17.6	3.3	3.3	1.1	8	12	Q2
TPS05P50B-DF8R	DFN3X3-10	330	17.6	3.3	3.3	1.1	8	12	Q2
TPS14P50A-DF8R	DFN3X3-10	330	17.6	3.3	3.3	1.1	8	12	Q2

Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPS14P50B-DF8R	DFN3X3-10	330	17.6	3.3	3.3	1.1	8	12	Q2

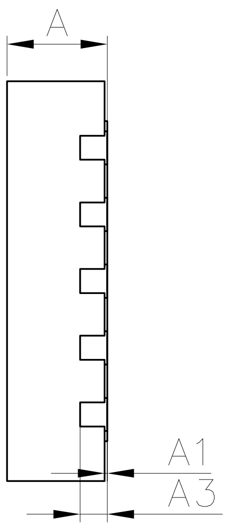
Package Outline Dimensions

DFN3X3-10-A

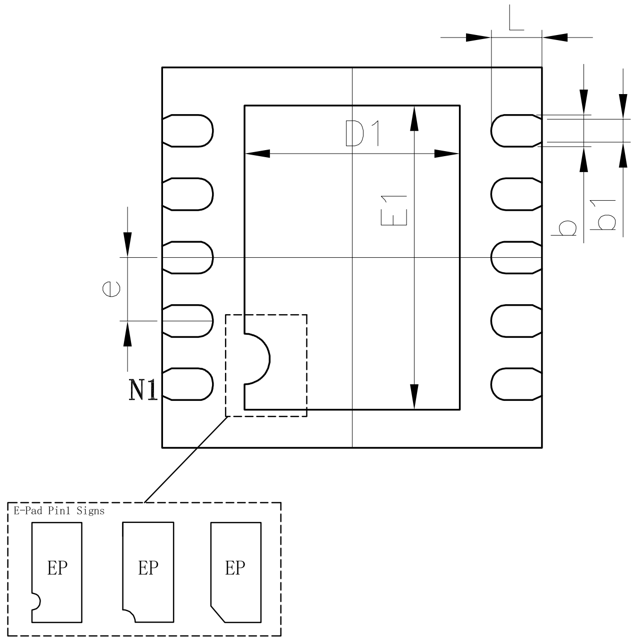
Package Outline Dimensions DF8(DFN3X3-10-A)



Top View



Side View



Bottom View

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
b1	0.180 REF		0.007 REF	
A3	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	2.300	2.500	0.091	0.098
e	0.500 BSC		0.020 BSC	
L	0.325	0.475	0.013	0.019

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPS05P50A-DF8R	−40 to 150°C	DFN3X3-10	S055A	MSL3	Tape and Reel, 4,000	Green
TPS05P50B-DF8R	−40 to 150°C	DFN3X3-10	S055B	MSL3	Tape and Reel, 4,000	Green
TPS14P50A-DF8R	−40 to 150°C	DFN3X3-10	S145A	MSL3	Tape and Reel, 4,000	Green
TPS14P50B-DF8R	−40 to 150°C	DFN3X3-10	S145B	MSL3	Tape and Reel, 4,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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