80-V, 4-A Boost Converter with Load Switch

Features

- 3.1-V to 80-V Input Voltage Range
- Internal 80-V, 110-mΩ Low Side MOSFET Switch
- 2.1-Ω Output Load Switch
- ±1% Reference Voltage Accuracy
- 0.4-mA Operating Quiescent Current
- 1-μA Shutdown Current
- Fixed Frequency Current Mode PWM Control
- Pulse Skipping at Light Loads
- Adjustable Switching Soft Startup Time
- Adjustable Frequency from 100 kHz to 2.2 MHz
- Programmable Input UVLO Threshold and Hysteresis
- Cycle-by-cycle Current Limit
- 100-ms Hiccup Mode Output Short Circuit Protection
- Operating T_J Temperature Range from −40°C ~ +125°C
- Available in 3.5 x 3.5 20-pin QFN Package

Applications

- 5-V, 12-V, 24-V, 48-V Power Conversion
- Wide Input Boost, SEPIC, and Flyback Converter
- Industrial PLC
- Flyback PoE Power Supply
- LED Power Supply
- Medical Equipment

Description

The TPQ80302 is a nonsynchronous switching boost converter with an integrated 80-V, 110-mΩ power switch, and a 2.1-Ω load switch. The device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and flyback. The device has a wide input voltage range up to 80 V to support applications with input voltage from multicell batteries or 5-V, 12-V, 24-V, and 48-V power rails.

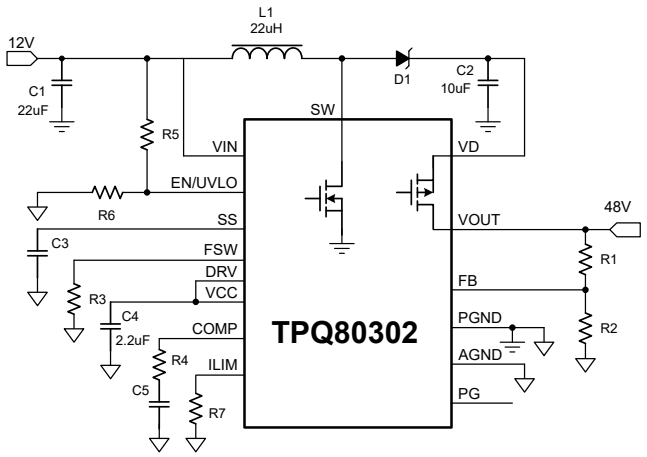
The TPQ80302 regulates the output voltage with peak current mode pulse width modulation (PWM) control. The switching frequency is programmable from 100 kHz to 2.2 MHz by an external resistor.

The TPQ80302 integrates a 80-V, 2.1-Ω load switch to disconnect the load from input voltage during shutdown. With the load switch, the device features adjustable DC startup charging current. When the output voltage is close to the input voltage, the device goes into switching mode soft startup.

The TPQ80302 has hiccup mode output short circuit protection when the output voltage at the VOUT pin is below the input voltage. The device also features cycle-by-cycle current limit in over-load condition.

The TPQ80302 is available in a 20-pin 3.5x3.5 QFN package with exposed thermal pad.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2024-01-22	Rev.A.0	Initial released.
2024-01-29	Rev.A.1	Figure 33 typo correction.
2025-02-26	Rev.A.2	Added absolute maximum transient voltage for the SW pin. Updated the Figure 17. Corrected the UVLO hysteresis current description in the EC table and the Enable and Programmable Input UVLO section. Updated the Figure 28 and the Figure 29. Corrected the Equation 2.

Pin Configuration and Functions

TPQ80302

QFN3.5X3.5-20

Top View

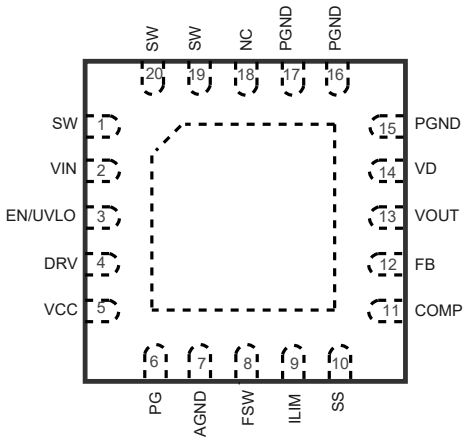


Table 1. Pin Functions: TPQ80302

Pin No.	Name	I/O	Description
1, 19, 20	SW	P	The SW pin is the drain of the internal power MOSFET switch. Connect the SW pin to the inductor and the anode of the Schottky diode in boost converter.
2	VIN	P	The input power supply for the IC. Connect the VIN pin to a supply voltage between 3.1V and 80V. It is acceptable for the voltage on the VIN pin to be different from the boost power stage input.
3	EN/UVLO	I	Enable input pin and input voltage UVLO setting. Connect to the middle tap of a resistor divider from VIN to AGND to set the input voltage UVLO threshold.
4	DRV	P	Power supply for internal MOSFET driver
5	VCC	P	Output of the internal regulator and supply voltage input of the internal control circuitry. Connect a ceramic bypass capacitor from this pin to AGND.
6	PG	O	Open drain output for power good indication. Output low voltage when the FB pin voltage is below undervoltage threshold or above the overvoltage threshold. The undervoltage could happen during startup or caused by overload or output short circuit. The overvoltage could happen when the output voltage is wrongly connected to a higher voltage than the converter's regulation outpuut. Connect a pull-up resistor between the PG pin and an IO supply power rail.
7	AGND	P	Signal ground of the IC
8	FSW	O	Switching frequency setting pin. An external resistor connected between the FSW pin and AGND sets the switching frequency.

9	ILIM	O	DC startup current limit setting pin. Connect a resister to limit the output current through the isolation MOSFET during DC startup.
10	SS	O	Soft startup time programming pin. An external capacitor sets the ramp rate of the reference voltage for the error amplifier during startup.
11	COMP	O	Output of the transconductance error amplifier. An external compensation RC network connected to this pin and AGND.
12	FB	I	Error amplifier input and the feedback pin for positive voltage regulation. Connect to the center tap of a resistor divider to program the output voltage.
13	VOUT	P	Output of the load switch
14	VD	P	Input of the load switch
15, 16, 17	PGND	P	Power ground of the IC. It is connected to the source of the internal MOSFET switch.
18	NC	-	No connection

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Voltage range at terminals	SW (DC)	−0.3	85	V
	SW (10ns transient, less than 1% duty cycle)	−4	85	V
	VIN, VD, VOUT	−0.3	80	V
	EN/UVLO	−0.3	40	V
	SS, VCC, COMP, FSW, FB, ILIM, PG	−0.3	6.0	V
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{IN}	Power Supply	3.1		80	V
V_{OUT}	Output Voltage	V_{IN}		80	V
C_{OUT}	Effective Capacitance at the output	4.7	10	1000	μF
L	Inductor	2.2	22	47	μH
T_J	Junction Temperature Range	–40		125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
QFN3.5X3.5-20L	47.2	32.1	°C/W

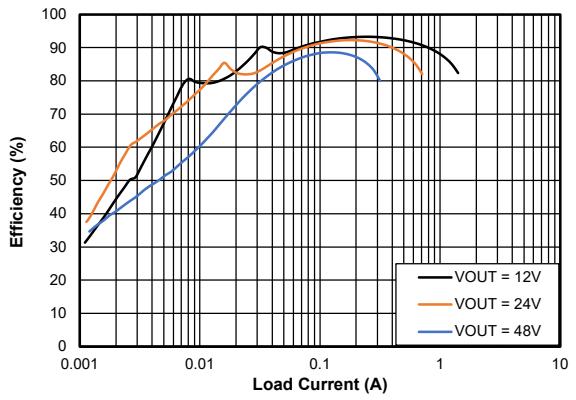
Electrical Characteristics

All test conditions: V_{IN} = 12 V, V_{CC} = 5 V, T_J = -40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
V_{IN}	IC Supply Voltage Range		3.1		80	V
I_Q	Operating Quiescent Current	No switching. V_{FB} = 2V		0.4	0.6	mA
I_{SD}	Shutdown Current	V_{EN} = 0V			2	μA
VCC Regulator						
V_{CC}	Regulator Output at VCC Pin	I_{VCC} = 10 mA	4.8	5.0	5.2	V
V_{CC_DR}	VCC Dropout	V_{IN} = 5 V, I_{VCC} = 10 mA		200	400	mV
V_{CC_UVLO}	UVLO of the VCC Regulator	V_{CC} rising	2.8	2.95	3.1	V
V_{CC_HYS}	UVLO Hysteresis of the VCC Regulator		100	200	300	mV
Power MOSFET Switch						
R_{DSON_N}	N-channel MOSFET on-Resistance	V_{CC} = 5 V		110		mΩ
I_{LIM}	Peak Current Limit	V_{CC} = 5 V	4.5	5	5.5	A
I_{SW_LKG}	N-channel MOSFET Leakage Current	V_{SW} = 12 V		1		μA
Gm_{PS}	Power Stage Transconductance	V_{COMP} = 1 V		10		S
Load Switch						
V_{ILIM}	ILIM Pin Voltage			1.208		V
R_{DSON_P}	P-channel MOSFET on-resistance	V_{CC} = 5 V		2.1		Ω
I_{LS_LKG}	P-Channel MOSFET Leakage Current	V_D = 12 V, V_{OUT} = 0 V		1		μA
Soft Start						
I_{DC}	DC Charge Current	V_{CC} = 5 V, R_{ILIM} = 14.3kΩ		600		mA
I_{SS}	Switching soft-start Current			5		μA
Reference						
V_{REF}	Reference Voltage at FB Pin	V_{CC} = 5 V	1.204	1.216	1.228	V
I_{FB_LKG}	FB Pin Leakage Current	V_{CC} = 5 V			20	nA
Error Amplifier						
I_{SINK}	COMP Pin Sink Current	V_{FB} = V_{REF} + 200 mV, V_{COMP} = 1 V		25		μA
I_{SOURCE}	COMP Pin Sink Current	V_{FB} = V_{REF} – 200 mV, V_{COMP} = 1 V		25		μA
V_{CLP_H}	COMP Pin Clamp High Voltage	VFB = 1 V , VCC = 5 V		2.1		V

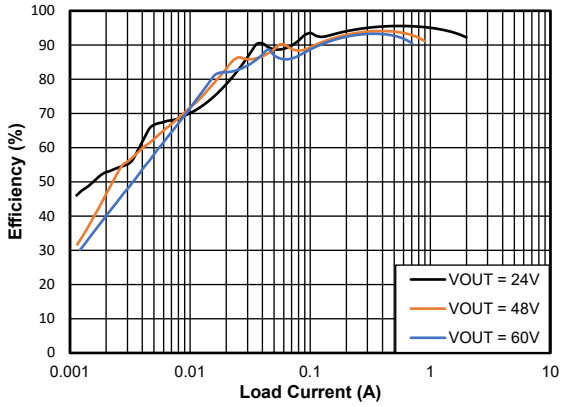
Parameter		Conditions	Min	Typ	Max	Unit
V_{CLP_L}	COMP Pin Clamp Low Voltage	VFB = 1.5 V		0.7		V
Gm_{EA}	Error Amplifier Transconductance		110	160	210	μS
Switching Frequency						
V_{FSW}	FSW Pin Voltage	V_{CC} = 5 V		1.218		V
f_{SW}	Switching Frequency	R_{FSW} = 470 kΩ		90		kHz
		R_{FSW} = 82 kΩ		500		kHz
		R_{FSW} = 39 kΩ		1000		kHz
		R_{FSW} = 18 kΩ		2000		kHz
T_{MIN_ON}	Minimum on Pulse Width	R_{FSW} = 82 kΩ		70		ns
Enable Control						
V_{EN_H}	EN Logic High Threshold (enable)	V_{CC} = 5 V			1.1	V
V_{EN_L}	EN Logic Low Threshold (disable)	V_{CC} = 5 V	0.4			V
V_{EN_HYS}	EN Threshold Hysteresis	V_{CC} = 5 V		100		mV
V_{UVLO}	UVLO Threshold	V_{CC} = 5 V	1.16	1.22	1.28	V
I_{UVLO}	UVLO Hysteresis Current Sinking into the EN Pin	0.9V < V_{EN} < 1.22V	3.8	4	4.2	μA
Power Good Output						
V_{PG_TH}	Power Good Threshold at the FB Pin	FB pin voltage rising (Good)	90%	93%	96%	V_{REF}
		FB pin voltage rising (Fault)	106%	109.5%	113%	V_{REF}
		FB pin voltage falling (Good)	103%	106%	109%	V_{REF}
		FB pin voltage falling (Fault)	86%	88.5%	92%	V_{REF}
V_{PG_OL}	PG Output Low Voltage	V_{CC} = 5 V, Sink 4mA current			0.2	V
I_{PG_LKG}	Leakage Current when Outputting High Impedance	V_{CC} = 5 V, V_{PG} = 5 V			1	μA
Junction Temperature Protection						
T_{SD}	Thermal Shutdown Protection Threshold	T_J rising		175		ºC
T_{SD_HYS}	Thermal Shutdown Hysteresis	T_J falling below T_{SD}		25		

Typical Performance Characteristics



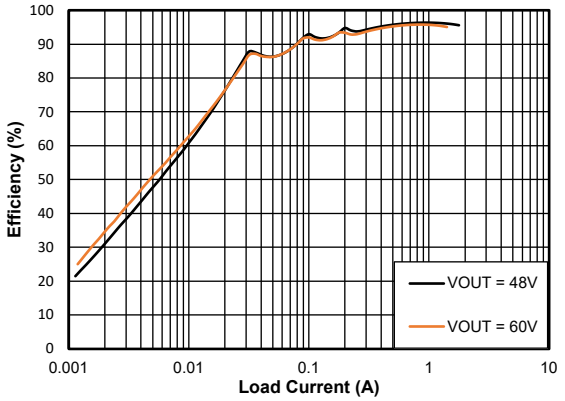
VIN = 5 V, VOUT = 12 V, 24 V, 48 V without load switch

Figure 1. Efficiency vs. Load Current



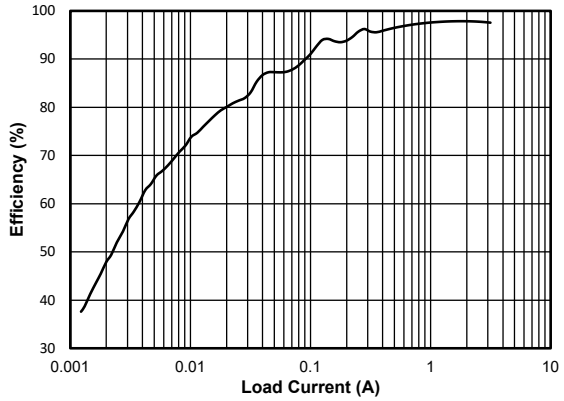
VIN = 12 V, VOUT = 24 V, 48 V, 60 V without load switch

Figure 2. Efficiency vs. Load Current



VIN = 24 V, VOUT = 48 V, 60 V without load switch

Figure 3. Efficiency vs. Load Current



VIN = 48 V, VOUT = 60 V without load switch

Figure 4. Efficiency vs. Load Current

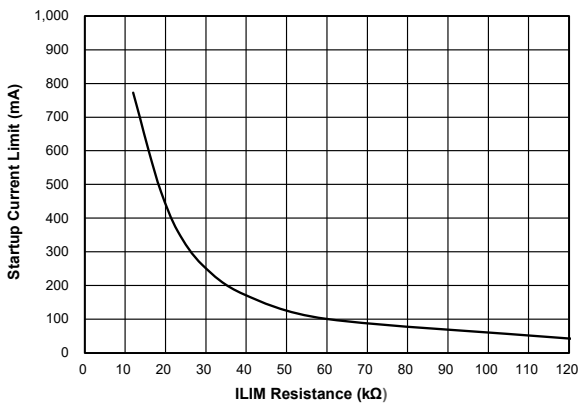


Figure 5. Startup Current Limit vs. ILIM Resistance

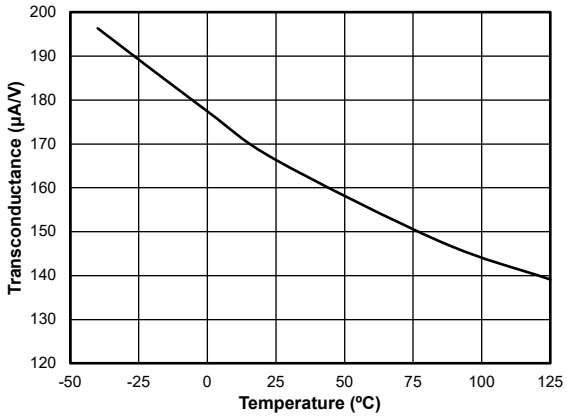


Figure 6. Error Amplifier Transconductance vs. Temperature

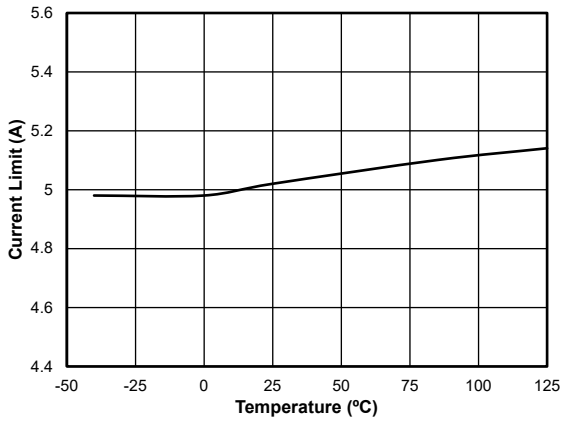


Figure 7. Switch Current Limit vs. Temperature

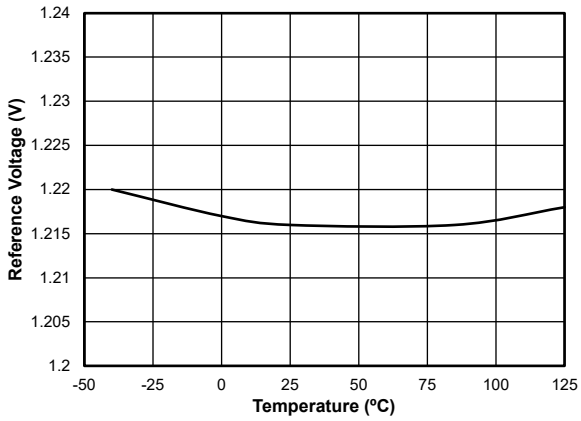


Figure 8. Voltage Reference vs. Temperature

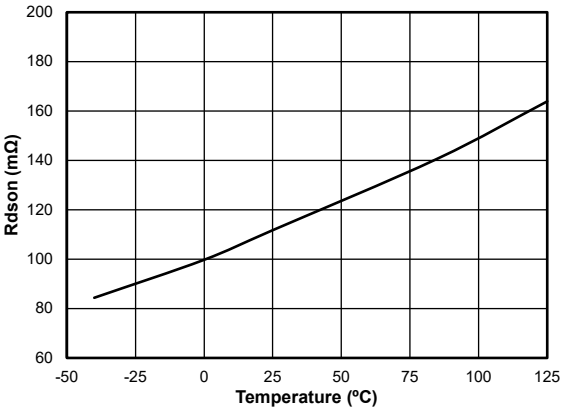


Figure 9. Rdson vs. Temperature

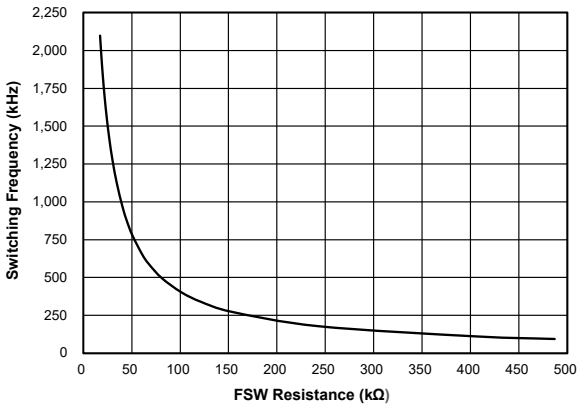


Figure 10. Switching Frequency vs. FSW Resistance

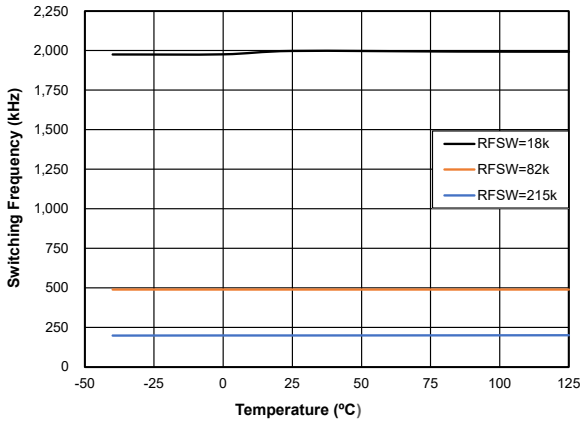


Figure 11. Switching Frequency vs. Temperature

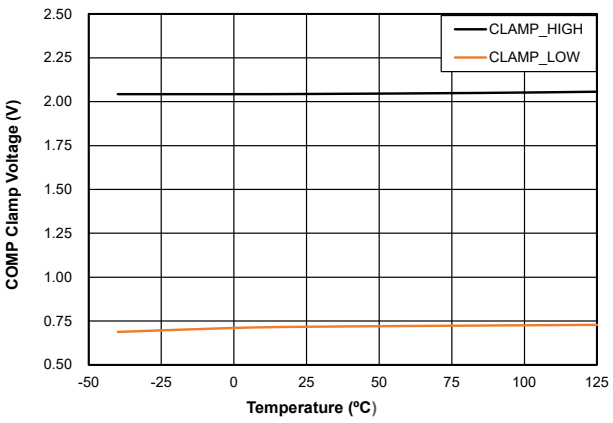


Figure 12. COMP Clamp Voltage vs. Temperature

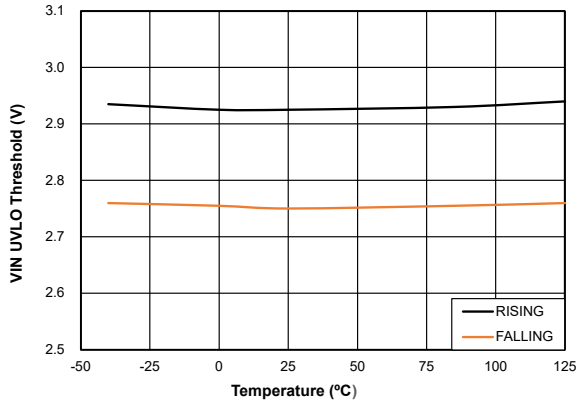


Figure 13. Input Voltage UVLO vs. Temperature

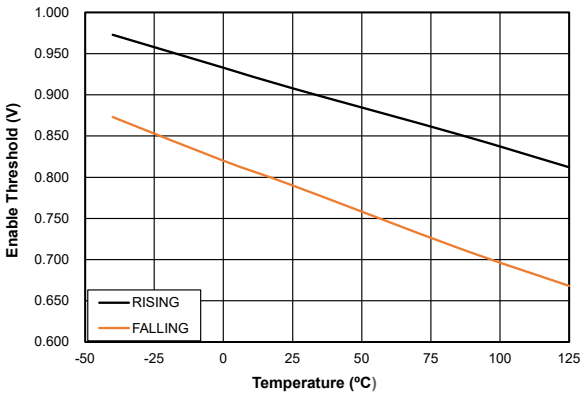


Figure 14. Enable Threshold vs. Temperature

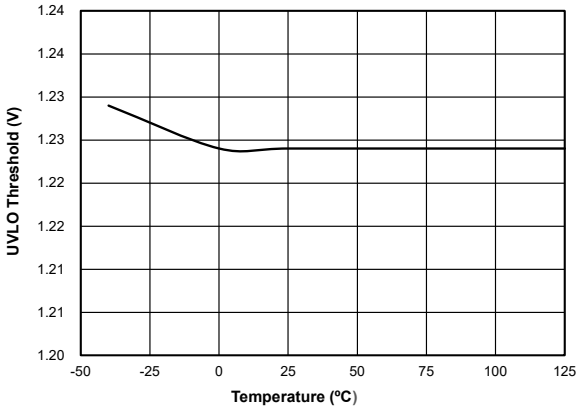


Figure 15. UVLO Threshlod vs. Temperature

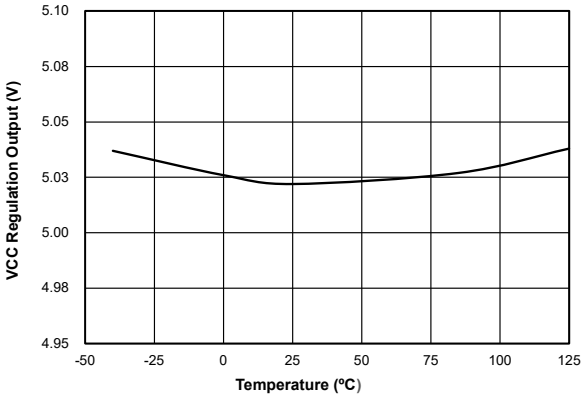
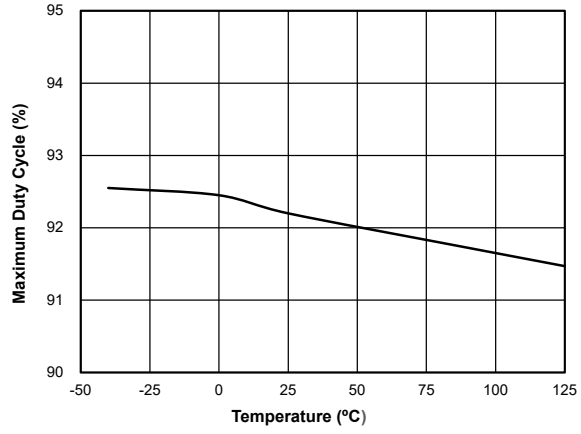
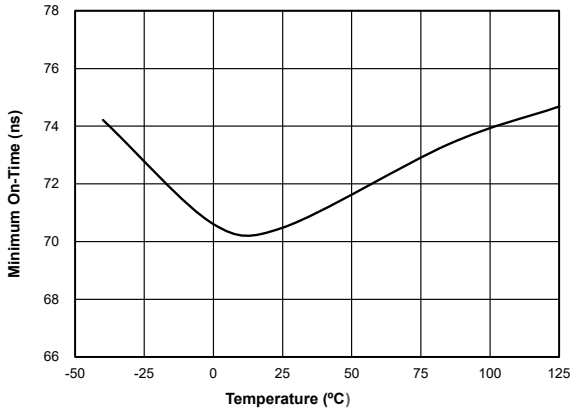


Figure 16. VCC Regulation Voltage vs. Temperature



R_{FSW} = 82 kΩ, f_{SW} = 500 kHz

Figure 17. Maximum Duty Cycle vs. Temperature



R_{FSW} = 82 kΩ, f_{SW} = 500 kHz

Figure 18. Minimum On-Time vs. Temperature

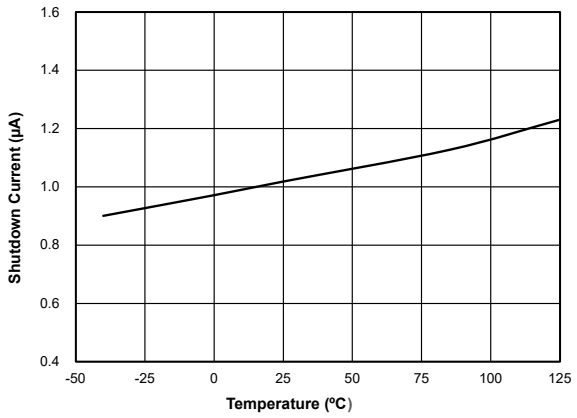


Figure 19. Shutdown Current vs. Temperature

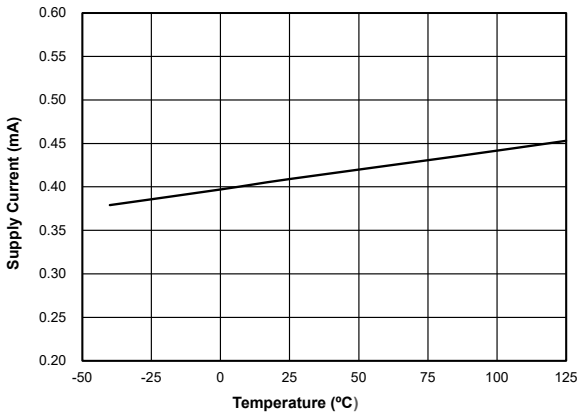
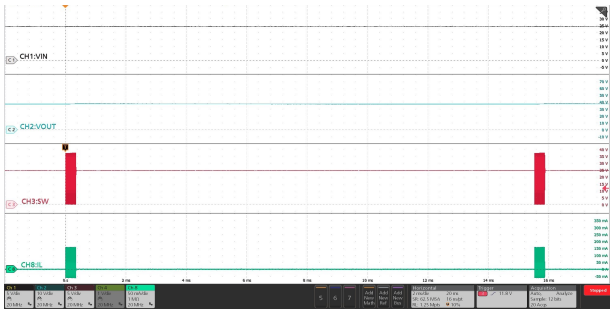
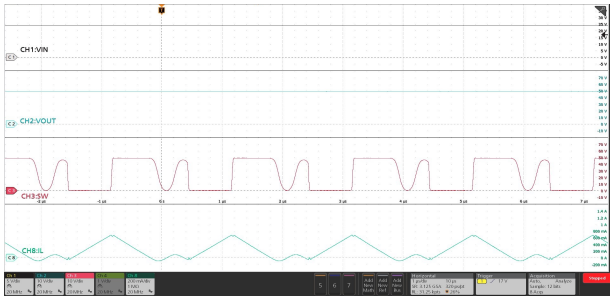


Figure 20. Supply Current vs. Temperature



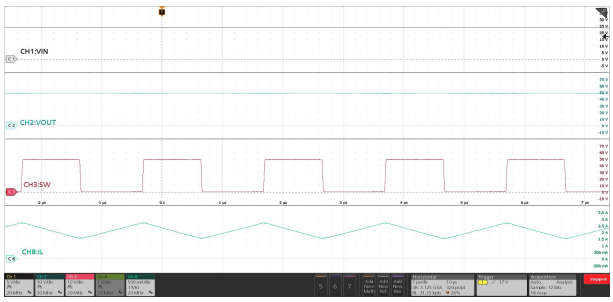
VIN = 24 V, VOUT = 36 V, IOUT = 0 A

Figure 21. Pulse Skipping Operation



VIN = 24 V, VOUT = 48 V, IOUT = 0.1 A

Figure 22. DCM PWM Operation



VIN = 24 V, VOUT = 48 V, IOUT = 1 A

Figure 23. CCM PWM Operation

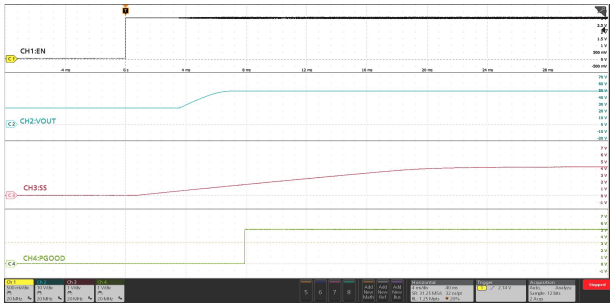


Figure 24. Statup Waveform by EN

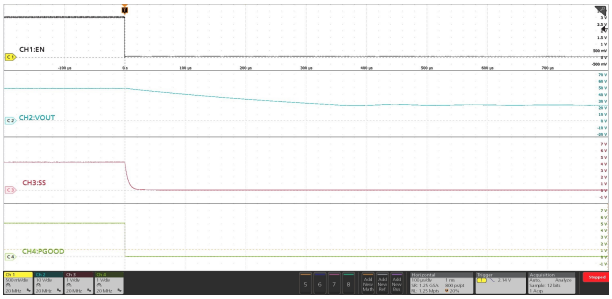


Figure 25. Shutdown Waveform by EN

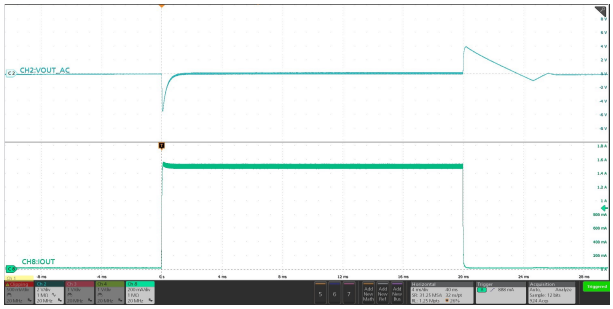


Figure 26. Load Transient Response

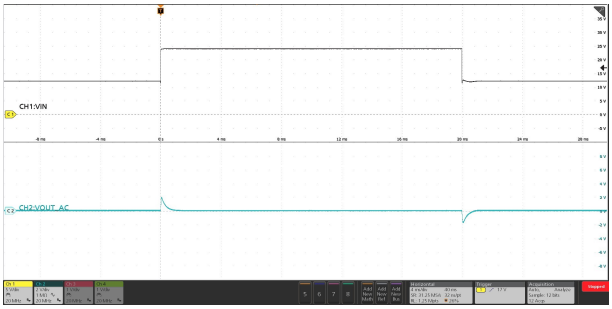


Figure 27. Line Transient

Detailed Description

Overview

The TPQ80302 is a nonsynchronous switching boost converter with an integrated 80-V, 110-mΩ power switch and a 2.1-Ω load switch. The device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and flyback. The device has a wide input voltage range up to 80 V to support applications with input voltage from multicell batteries or 5-V, 12-V, 24-V, and 48-V power rails.

The TPQ80302 uses a peak current mode pulse width modulation (PWM) control scheme which provides simplified loop compensation, rapid response to the load transients, and inherent line voltage rejection. An error amplifier compares the feedback voltage with the internal reference voltage. The output of the error amplifier determines the peak inductor current.

The internal oscillator can be configured to operate over a wide range of frequencies from 100 kHz to 2.2 MHz.

The TPQ80302 works in fixed frequency PWM mode at moderate to heavy load currents. In the light load condition, the TPQ80302 works in skip mode to maintain the output regulation.

The TPQ80302 provides hiccup mode short circuit protection to reduce the heating in the power components when an output short circuit happens. In output short circuit condition, the TPQ80302 turns off for 100 ms, discharges the SS pin and starts soft startup again.

Functional Block Diagram

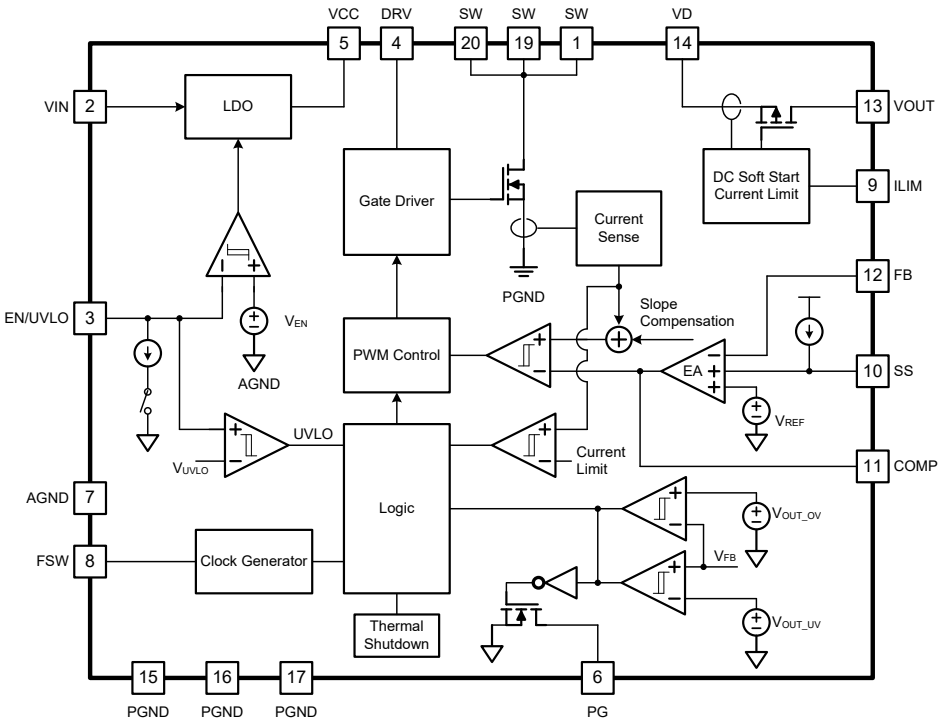


Figure 28. Functional Block Diagram

Feature Description

Enable and Programmable Input UVLO

The TPQ80302 has a dual function enable and undervoltage lockout (UVLO) circuit. When the input voltage at the VIN pin is above 3.1 V and the EN/UVLO pin is pulled above 1.1 V but less than the enable UVLO threshold of 1.22 V, the TPQ80302 is enabled but still in standby mode. The EN/UVLO pin has an accurate UVLO voltage threshold to support programmable input undervoltage lockout with hysteresis. When the EN/UVLO pin voltage is above typical 0.9 V and less than 1.22 V, the EN/UVLO pin sinks a typical 4-μA hysteresis current. When the EN/UVLO pin voltage goes up above 1.22 V, the 4-μA hysteresis current stops immediately. With external resistor divider, the hysteresis current I_{UVLO} provides programmable hysteresis voltage at the EN/UVLO pin that prevents on/off from chattering in the presence of noise with a slowly changing input voltage. When the voltage at the EN/UVLO pin is higher than the UVLO threshold of 1.22 V, the TPQ80302 is enabled.

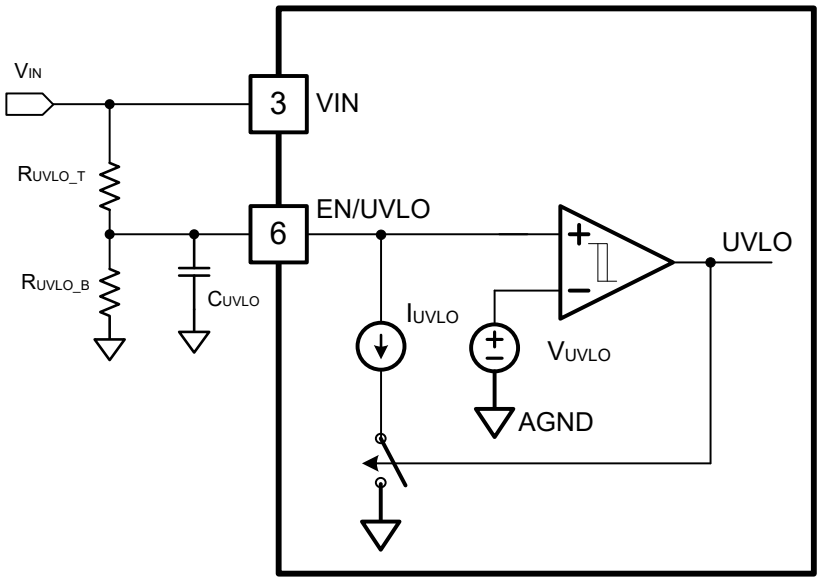


Figure 29. Input UVLO Threshold Setting

The input UVLO threshold can be programmed by using a resistor divider as shown in Figure 29. By setting the desired turn-on input voltage V_{IN_ON} and turn-off input voltage V_{IN_OFF}, the resistance of the resistor divider is calculated by Equation 1 and Equation 2.

$$R_{UVLO\_T} = \frac{V_{IN\_ON} - V_{IN\_OFF}}{I_{UVLO}} \quad (1)$$

$$R_{UVLO\_B} = \frac{V_{UVLO} \times R_{UVLO\_T}}{V_{IN\_OFF} - V_{UVLO}} \quad (2)$$

Where

- V_{UVLO} is the UVLO threshold voltage at the EN/UVLO pin.
- I_{UVLO} is the hysteresis current sinking into the EN/UVLO pin.

A UVLO glitch filtering capacitor (C_{UVLO}) is required in case that the input voltage drops below the V_{IN_OFF} momentarily during the start-up or during a severe load transient at the low input voltage. The UVLO filtering capacitor should be less than 1nF to allow the voltage at the EN/UVLO pin quickly raised when the 4-μA hysteresis current turns off.

Do not leave the EN/UVLO pin floating. Connect it to a high voltage above UVLO threshold if not used.

Soft Startup

The TPQ80302 has a two-step startup that limits the inrush current during startup. The first step is the DC pre-charge phase. During DC pre-charge, the isolation MOSFET is turned on with the current limit set by the resistor at the ILIM pin. When the output capacitor at the VOUT pin is charged to a voltage close to the input voltage, the device starts switching. The soft-start system progressively increases the on-time as a function of the input-to-output voltage ratio. As soon as the output voltage is reached, the regulation loop takes control.

In boost topology, the soft-start time (t_{SS}) varies with the input supply voltage. The soft-start time in boost topology is calculated as shown in Equation 3.

$$t_{ss} = \frac{C_{SS}}{I_{SS}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times V_{REF} \quad (3)$$

After DC startup, the isolation MOSFET is fully turned on. The resistor at the ILIM pin doesn't limit the current through the isolation MOSFET.

Adjustable Switching Frequency

This TPQ80302 features a wide adjustable switching frequency ranging from 100 kHz to 2.2 MHz. The switching frequency is set by a resistor connected between the FSW pin and the AGND pin of the TPQ80302. A resistor must always be connected from the FSW pin for proper operation. The resistor value required for a desired frequency can be calculated using Equation 4.

$$R_{FSW} = \frac{4.3 \times 10^{10}}{f_{SW(TYPICAL)}} - 3500 \quad (4)$$

Power Good Indication

The PG pin output is an open drain MOSFET. The output is pulled low when the FB pin voltage enters the fault condition by falling below 88.5% or rising above 109.5% of the nominal internal reference voltage. There is an approximate 4% hysteresis on the threshold voltage, so when the FB pin voltage rises to good condition above 93% or falls below 106% of the internal voltage reference, the PG output MOSFET is turned off. It is recommended to use a pull-up resistor between the values of 1 kΩ and 500 kΩ to an IO voltage that is below 5.5 V. The PG is in a valid state once the VCC voltage is greater than 0.8 V, typically.

Hiccup Mode Overload Protection

To protect the converter during prolonged current limit conditions, the TPQ80302 provides hiccup mode overload protection. The internal hiccup mode fault timer of the device counts the PWM clock cycles when the cycle-by-cycle current limit occurs after soft start is finished. When the hiccup mode fault timer detects 64 cycles of current limiting, an internal hiccup mode off timer forces the device to stop switching and pulls down the SS pin. Then the device restarts after 100 ms hiccup mode off time. The 64-cycle mode fault timer is reset if eight consecutive switching cycles occur without exceeding the current limit threshold.

Output Short Circuit Protection

After the TPQ80302 completes the DC soft startup, if the voltage at the VOUT pin is still 2 V lower than the input voltage, the TPQ8032 turns off the isolation MOSFET for 100 ms and pulls down the SS pin. Then the device restarts after 100 ms hiccup mode off time.

Switching Current Limit

The TPQ80302 provides cycle-by-cycle peak current limit protection that turns off the internal power MOSFET when the inductor current trips the current limit threshold.

Thermal Shutdown Protection

A thermal shutdown is implemented to prevent damage due to excessive heat and power dissipation. Typically the thermal shutdown happens at a junction temperature of 175°C. When the thermal shutdown is triggered, the device stops switching until the junction temperature falls below typically 150°C, then the device starts switching again.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPQ80302 is designed for outputting voltage up to 80 V. It adopts peak current mode pulse width modulation (PWM) control scheme to achieve fast transient response.

Typical Application

Figure 30 shows the typical application schematic of 12-V to 48-V boost converter.

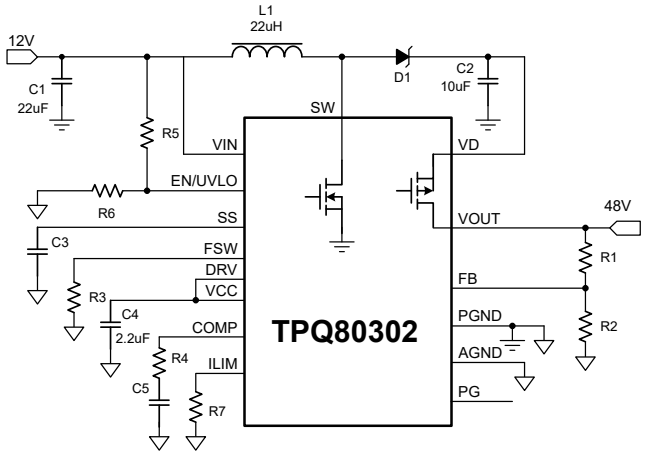


Figure 30. TPQ80302 12-V to 48-V Boost Application Circuit

Selecting the Switching Frequency

Connect a resistor between the FSW pin and the AGND pin to set the switching frequency. The resistance can be calculated by Equation 4.

Setting Output Voltage

The output voltage is set by an external resistor divider with the center tap connecting to the FB pin. Typically a minimum current of 10 μA flowing through the feedback divider gives good accuracy and noise covering. A resistor of less than 120 kΩ is typically selected for low-side resistor R2.

When the output voltage is regulated, the typical voltage at the FB pin is VREF. Thus, the value of R1 is calculated as:

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \quad (5)$$

Switching Duty Cycle

The duty cycle of the converter in continuous conduction mode (CCM) is related primarily to the input and output voltages as computed by Equation 6.

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D} \quad (6)$$

Where,

V_D is the forward voltage drop of the Schottky diode

At light load, the converter operates in discontinuous conduction mode (DCM). In this case, the duty cycle is a function of the load, input and output voltages, inductance, and switching frequency as computer by Equation 7.

$$D = \frac{\sqrt{2 \times (V_{OUT} + V_D - V_{IN}) \times L \times I_{OUT} \times f_{SW}}}{V_{IN}} \quad (7)$$

Selecting the Inductor

The selection of the inductor affects steady-state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications: inductor value, dc resistance, and saturation current. Considering inductor value alone is not enough. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, the effective inductance can fall to a fraction of the zero current value.

The following Equation 8, Equation 9, and Equation 10 calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, it is recommended to use the minimum switching frequency, the inductor value with -20% tolerance, and a low-power conversion efficiency for the calculation.

In a boost regulator, calculate the inductor DC current as in Equation 8.

$$I_{DC} = \frac{(V_{OUT} + V_D) \times I_{OUT}}{V_{IN} \times \eta} \quad (8)$$

Where,

V_D is the forward voltage drop of the Schottky diode

η is the power conversion efficiency

Calculate the inductor current peak-to-peak ripple as in Equation 9.

$$I_{LPP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} + V_D - V_{IN}} + \frac{1}{V_{IN}}\right) \times f_{SW}} \quad (9)$$

Therefore, the peak current of the inductor can be calculated by Equation 10.

$$I_{LPEAK} = I_{DC} + \frac{I_{LPP}}{2} \quad (10)$$

The calculated peak current of the inductor must be less than the current limit of the TPQ80302. Select an inductor with saturation current higher than the calculated peak current.

Maximum Output Current

The overcurrent limit of the TPQ80302 limits the maximum input current and thus the maximum input power for a given input voltage. The maximum output power is less than the maximum input power due to power conversion losses. Because of the TPQ80302's peak inductor current limit, the maximum output current can be calculated by Equation 11.

A smaller inductor can increase the high current ripple thus reducing the maximum output current.

$$I_{OUT(MAX)} = \frac{\left(I_{LIM} - \frac{I_{LPP}}{2}\right) \times V_{IN(MIN)} \times \eta}{V_{OUT}} \quad (11)$$

Where,

I_{LIM} is the switching current limit of the TPQ80302

Selecting the Output Capacitors

At least 4.7-μF capacitance of ceramic X5R or X7R capacitor is recommended at the output. The output capacitance is mainly selected to meet the requirements for the output ripple and voltage change during a load transient. Then the loop is compensated for the output capacitor selected. The output capacitance should be chosen based on the most stringent of these criteria. The output ripple voltage is related to the capacitance and equivalent series resistance (ESR) of the output capacitor. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given output ripple voltage can be calculated by Equation 12. If high ESR capacitors are used, it will contribute additional ripple. The maximum ESR for a specified ripple is calculated with Equation 13. ESR ripple can be neglected for ceramic capacitors but must be considered if electrolytic capacitors are used. The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated by Equation 14.

$$C_{OUT} \geq \frac{D_{MAX} \times I_{OUT}}{V_{RIPPLE} \times f_{SW}} \quad (12)$$

$$R_{ESR} \leq \frac{\left(V_{RIPPLE} - \frac{D_{MAX} \times I_{OUT}}{f_{SW} \times C_{OUT}}\right)}{\Delta I_L} \quad (13)$$

$$C_{OUT} \geq \frac{\Delta I_{TRAN}}{2\pi \times f_C \times \Delta V_{TRAN}} \quad (14)$$

Where,

V_{RIPPLE} is the output ripple voltage

f_C is the crossover frequency of the open loop of the converter

ΔI_{TRAN} is the output current change during load transient

ΔV_{TRAN} is the output voltage change during load transient

Selecting the Input Capacitors

At least 4.7-μF capacitance of ceramic input capacitor is recommended. Additional input capacitance may be required to meet ripple and/or transient requirements. High-quality ceramic, type X5R or X7R are recommended to minimize capacitance variations over temperature.

Selecting the Schottky Diode

The high switching frequency of the TPQ80302 demands high-speed rectification for optimum efficiency. Ensure that the average and peak current ratings of the Schottky diode exceed the average output current. In addition, the reverse breakdown voltage of the diode must exceed the regulated output voltage. The diode must also be rated for the power dissipated which can be calculated with Equation 15.

$$P_D = V_D \times I_{OUT} \quad (15)$$

Control Loop Compensation for Stability

The TPQ80302 requires external compensation which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. A external compensation network composed of resistor and capacitors is connected to the COMP pin to provide poles and a zero as shown in. These poles and zero, along with the inherent pole and zero of a boost converter, determine the closed-loop frequency response.

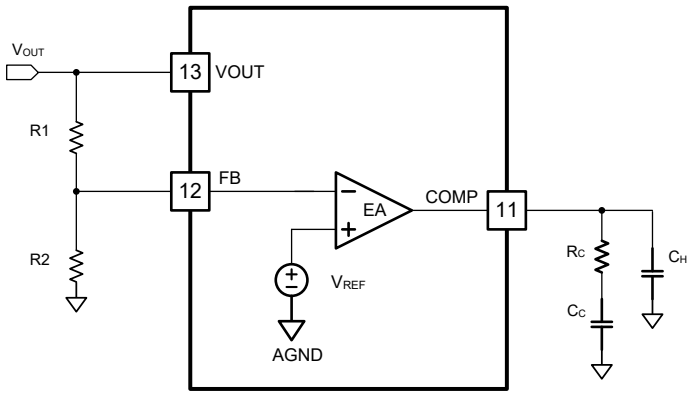


Figure 31. Type II Compensation Network

In CCM mode, approximately, the small signal frequency response of the power stage of the peak current mode boost converter can be modeled by Equation 16.

$$G_{PS}(S) = \frac{R_O \times (1 - D) \times G_{mps}}{2} \times \frac{\left(1 + \frac{S}{2\pi \times f_{ESRZ}}\right) \times \left(1 - \frac{S}{2\pi \times f_{RHPZ}}\right)}{1 + \frac{S}{2\pi \times f_P}} \quad (16)$$

Where,

D is the switching duty cycle

R_O is the output load resistance

Gm_{PS} is the transconductance of the power stage

f_P is the pole's frequency

f_{ESRZ} is the zero's frequency

f_{RHPZ} is the right-half-plane-zero's frequency

The f_P, f_{ESRZ} and f_{RHPZ} can be calculated by following equations.

$$f_P = \frac{2}{2\pi \times R_O \times C_{OUT}} \quad (17)$$

Where

C_{OUT} is the effective capacitance of the output capacitor

$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (18)$$

Where

R_{ESR} is the equivalent series resistance of the output capacitor

$$f_{RHPZ} = \frac{R_O \times (1 - D)^2}{2\pi \times L} \quad (19)$$

The COMP pin is the output of the internal transconductance amplifier. Equation (20) shows the small signal transfer function of the compensation network

$$G_C(S) = \frac{G_{mEA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{S}{2\pi \times f_{COMZ}}\right)}{\left(1 + \frac{S}{2\pi \times f_{COMP1}}\right) \times \left(1 + \frac{S}{2\pi \times f_{COMP2}}\right)} \quad (20)$$

Where

Gm_{EA} is the amplifier's transconductance

R_{EA} is the amplifier's output resistance

V_{REF} is the reference voltage at the FB pin

V_{OUT} is the output voltage

f_{COMP1}, f_{COMP2} are the poles' frequency of the compensation network

f_{COMZ} is the zero's frequency of the compensation network

The next step is to choose the loop crossover frequency, f_C. The higher in frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the crossover frequency no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}.

At the crossover frequency, the open loop gain is 0dB. Thus the value of the R_C can be calculated by Equation 21. Then set the values of C_C and C_H by Equation 22, and Equation 23.

$$R_C = \frac{2\pi \times V_{OUT} \times f_C \times C_{OUT}}{(1 - D) \times V_{REF} \times G_{mPS} \times G_{mEA}} \quad (21)$$

$$C_C = \frac{R_O \times C_{OUT}}{2 \times R_C} \quad (22)$$

$$C_H = \frac{R_{ESR} \times C_{OUT}}{R_C} \quad (23)$$

If the calculated C_H is less than 10pF, it can be left open.

Designing the open loop frequency response with greater the 45º phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

Application Examples

120-V Voltage Regulator

By following a charge pump voltage doubler, the TPQ80302 can be configured to output 120V voltage for some applications requiring high voltage power supply.

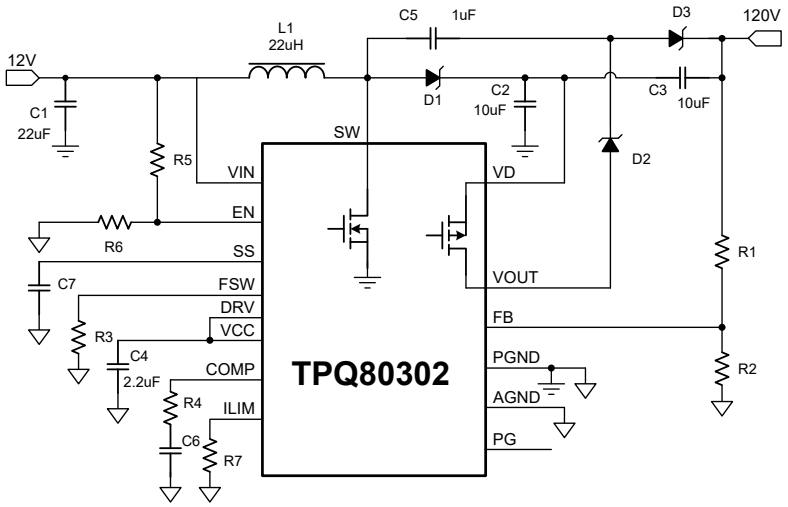


Figure 32. 120-V Output from 12-V Input

SEPIC Application

SEPIC converter is used for its output voltage can be set to higher or lower than the input voltage. Figure 33 shows a typical application schematic of SEPIC converter.

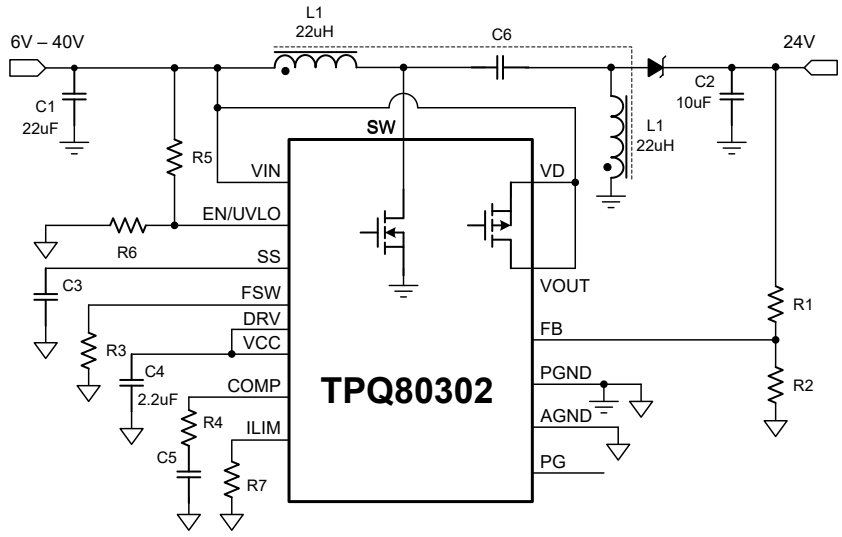


Figure 33. 6-V to 40-V Input, 24-V Output SEPIC Application

Layout

Layout Guideline

Because the TPQ80302 runs at high frequency and high currents, layout is an important design step to get the good performance. If layout is not carefully done, the regulator could go into instability as well as noise problems. The TPQ80302 runs at fast switching rise and fall at switch node to maximize the efficiency. To prevent radiation of high frequency noise, proper layout of the high frequency switching path is essential.

- Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling.
- The most critical current path for all boost converters is from the switching FET, through the rectifier Schottky diode, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the VD pin, but also to the PGND pin to reduce the overshoot at the SW pin and the VD pin.
- The input capacitor needs to be close to the VIN pin and PGND pin to reduce the input supply current ripple.
- Connect the AGND and PGDN pins to thermal pad directly on the same layer

Layout Example

Figure 34 shows the location of external components as they appear on the PCB.

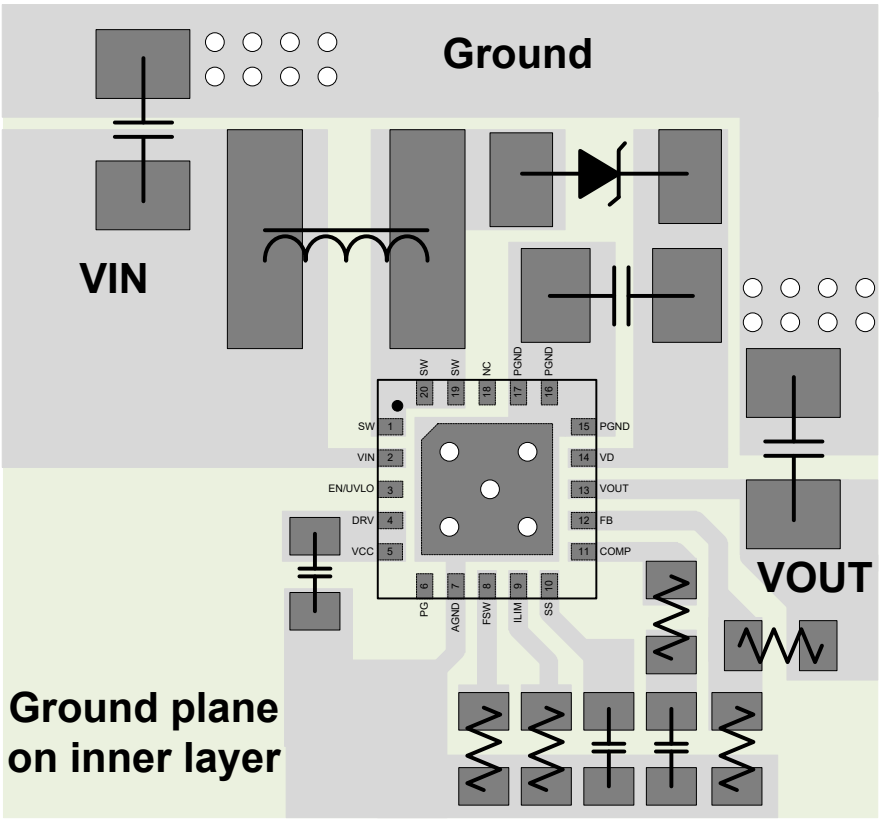
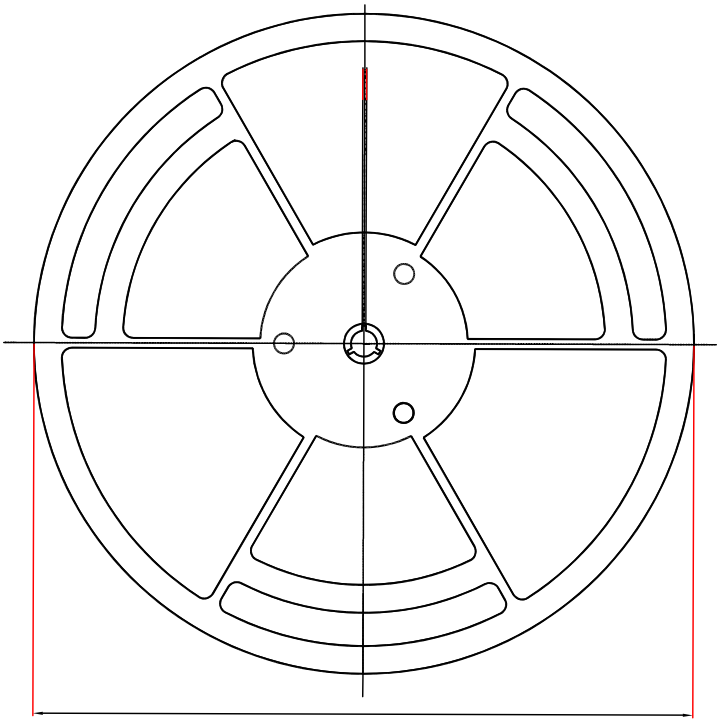
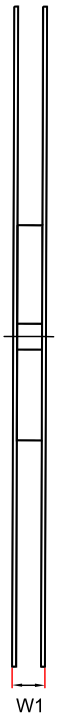
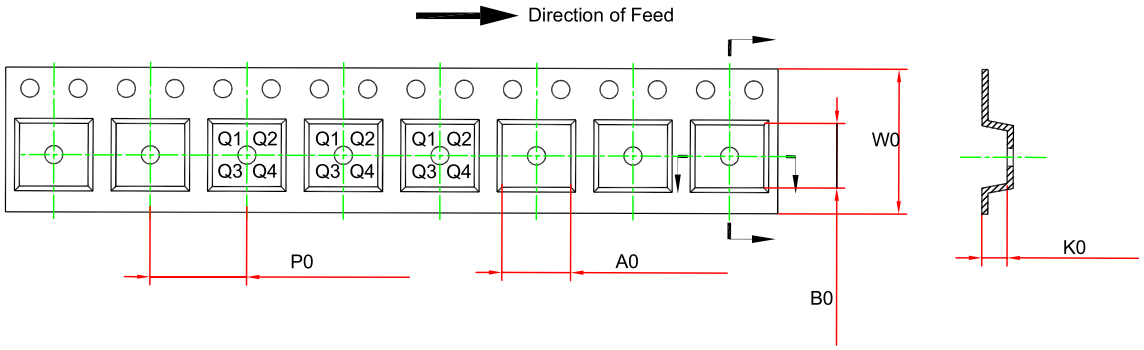


Figure 34. TPQ80302 Layout Example

Tape and Reel Information





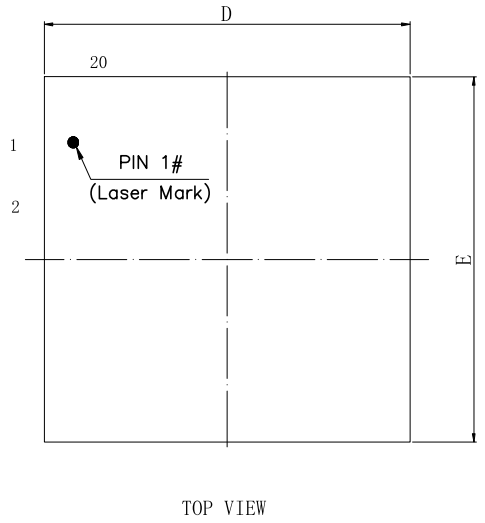


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPQ80302-QF6R-S	QFN3.5X3.5-20	330	17.6	3.8	3.8	1.1	8	12	Q1

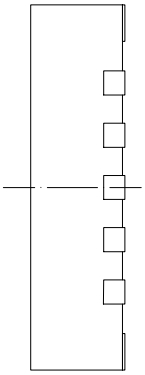
Package Outline Dimensions

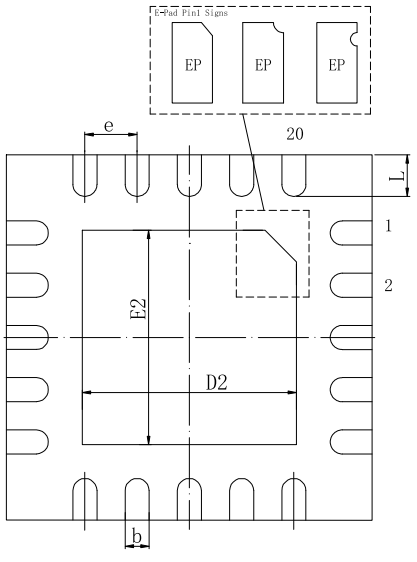
QFN3.5X3.5-20

Package Outline Dimensions QF6(QFN3.5X3.5-20-C)

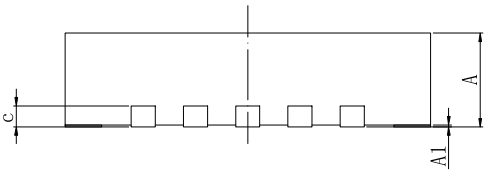


TOP VIEW





BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
c	0.203 REF		0.008 REF	
D	3.400	3.600	0.134	0.142
E	3.400	3.600	0.134	0.142
e	0.500 BSC		0.020 BSC	
L	0.350	0.450	0.014	0.018
D2	2.000	2.100	0.079	0.083
E2	2.000	2.100	0.079	0.083

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPQ80302-QF6R-S	−40ºC – 125ºC	QFN3.5X3.5-20	80302	MSL3	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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