75-V, PSR Flyback DC/DC Converter with 100-V, 1.5-A Internal Switch

Features

- AEC-Q100-Qualified for Automotive Applications
  - Grade 1 T_A Range: −40ºC to 125ºC
- 4.5-V to 75-V Input Voltage
- ±1.5% Output Regulation Accuracy
- Optional VOUT Temperature Compensation
- Integrated 100-V, 0.4-Ω Power MOSFET
- 6-ms Internal or Programable Soft Start
- Adjustable Input UVLO Protection
- Hiccup-Mode Overcurrent Fault Protection
- No Opto-Coupler or Transformer Auxiliary Winding Required for VOUT Regulation
- Quasi-Resonant Switching in Boundary Conduction Mode (BCM) at Heavy Load
- External Bias Option for Improved Efficiency
- Available in DFN4X4-8 Package

Applications

- Automotive Body Electronics
- Automotive Power Train Systems
- Isolated Bias Power Rails

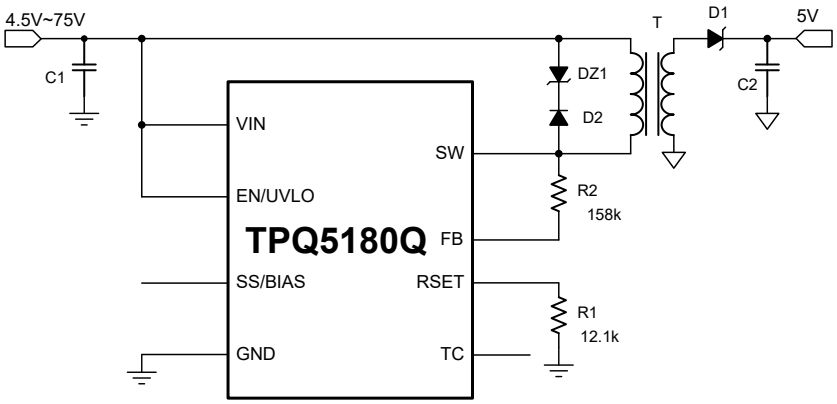
Description

The TPQ5180Q is a primary-side regulated (PSR) flyback converter with high efficiency over a wide input voltage range of 4.5 V to 75 V. The isolated output voltage is sampled from the primary-side flyback voltage, eliminating the need for an optocoupler, voltage reference, or third winding from the transformer for output voltage regulation. The high-level integration results in a simple, reliable, and high-density design with only one component crossing the isolation barrier. Boundary conduction mode (BCM) switching enables a compact magnetic solution and better than ±1.5% load and line regulation performance. An integrated 100-V power MOSFET provides output power up to 7 W with enhanced headroom for line transients.

The TPQ5180Q converter simplifies the implementation of isolated DC/DC supplies with optional features to optimize performance for the target-end equipment. The output voltage is set by one resistor, while an optional resistor improves the output voltage accuracy by negating the thermal coefficient of the flyback diode voltage drop. Additional features include an internally fixed or externally programmable soft start, optional bias supply connection for higher efficiency, precision enable input with hysteresis for adjustable line UVLO, hiccup-mode overload protection, and thermal shutdown protection with automatic recovery.

The TPQ5180Q is qualified to automotive AEC-Q100 grade 1 and is available in DFN4x4-8 package.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2025-03-11	Rev.A.0	Initial release

Pin Configuration and Functions

TPQ5180Q
DFN4X4-8
Top View

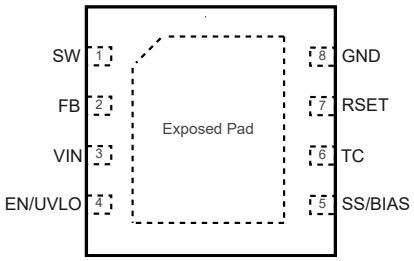


Table 1. Pin Functions

Pin No.	Name	I/O	Description
1	SW	P	Switch node that is internally connected to the drain of the N-channel power MOSFET. Connect to the primary-side switching terminal of the flyback transformer.
2	FB	I	Primary-side feedback pin. Connect a resistor from the FB pin to the SW pin. The ratio of the FB resistor to the resistor at the RSET pin sets the output voltage.
3	VIN	P	Input supply connection. Source for internal bias regulators and the input voltage sensing pin. Connect directly to the input supply of the converter with short, low-impedance paths.
4	EN/UVLO	I	Enable input and under-voltage lockout (UVLO) programming pin. If the EN/UVLO voltage is below typical 1 V, the converter is in shutdown mode with all functions disabled. If the EN/UVLO voltage is greater than typical 1 V and below 1.5 V, the converter is in standby mode with the internal regulator operational and no switching. If the EN/UVLO voltage is above 1.5 V, the start-up sequence begins.
5	SS/BIAS	I	Soft-start or bias input. Connect a capacitor from the SS/BIAS pin to GND to adjust the output start-up time and input inrush current. If the SS/BIAS pin is left open, the internal 6-ms soft-start timer is activated. Connect an external supply to the SS/BIAS pin to supply bias to the internal voltage regulator and enable the internal soft start.
6	TC	I	Temperature compensation pin. Tie a resistor from the TC pin to the RSET pin to compensate for the temperature coefficient of the forward voltage drop of the secondary diode, thus improving regulation at the secondary-side output.
7	RSET	I	Reference resistor tied to GND to set the reference current for FB. Connect a 12.1-kΩ resistor from RSET to GND.
8	GND	GND	Analog and power ground. Ground connection of internal control circuits and the power MOSFET.
	E-pad		Exposed pad for thermal enhancement. Connect the e-pad to ground plane for better thermal performance.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Voltage Range at Terminals (Refer to GND)	SW (DC)	−1.5	100	V
	SW (20ns transient, less than 1% duty cycle)	−3	100	V
	VIN, EN/UVLO, FB	−0.3	80	V
	FB to VIN	−0.3	0.3	V
	SS/BIAS	−0.3	20	V
	TC, RSET	−0.3	3.5	V
T_J	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
V_{HBM}	Human Body Model ESD	AEC-Q100-002 (1)	2000	V
V_{CDM}	Charged Device Model ESD	AEC-Q100-011	750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{IN}	Input Voltage	4.5		75	V
V_{SW}	SW Voltage			95	V
$V_{EN/UVLO}$	EN/UVLO Voltage			75	V
$V_{SS/BIAS}$	SS/BIAS Voltage			18	V
T_J	Junction Temperature Range	–40		150	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
DFN4X4-8	41.1	13.2	28.9	°C/W

Electrical Characteristics

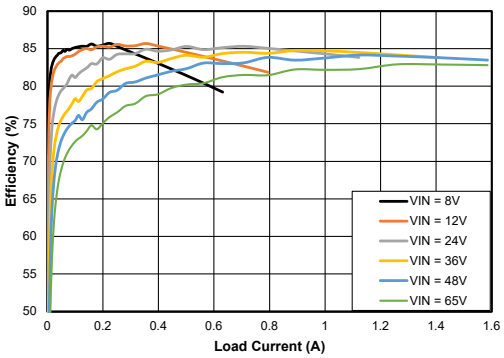
All test conditions: V_{IN} = 24 V, $V_{EN/UVLO}$ = 2 V, T_J = −40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Current						
$I_{SHUTDOWN}$	VIN Shutdown Current	$V_{EN/UVLO}$ = 0 V		3		μA
I_{ACTIVE}	VIN Active Current	$V_{EN/UVLO}$ = 2.5 V, V_{RSET} = 1.8 V		350	400	μA
$I_{ACTIVE-BIAS}$	VIN Current with BIAS Connected	$V_{SS/BIAS}$ = 6 V		25	52	μA
$V_{SD-FALLING}$	Shutdown Threshold	$V_{EN/UVLO}$ falling	0.5			V
Enable and Input UVLO						
$V_{SD-RISING}$	Standby Threshold	$V_{EN/UVLO}$ rising		1	1.2	V
$V_{UV-RISING}$	Enable Threshold	$V_{EN/UVLO}$ rising	1.45	1.5	1.55	V
$V_{UV-HYST}$	Enable Voltage Hysteresis	$V_{EN/UVLO}$ falling	36	46		mV
$I_{UV-HYST}$	Enable Current Hysteresis	$V_{EN/UVLO}$ = 1.6 V	4.2	5	5.5	μA
Feedback						
I_{RSET}	RSET Current	R_{RSET} = 12.1 kΩ		100		μA
V_{RSET}	RSET Regulation Voltage	R_{RSET} = 12.1 kΩ	1.191	1.21	1.224	V
$V_{FB-VIN1}$	FB to VIN Voltage	I_{FB} = 80 μA	–60			mV
$V_{FB-VIN2}$	FB to VIN Voltage	I_{FB} = 120 μA			60	mV
Switching Frequency						
F_{SW-MIN}	Minimum Switching Frequency			12		kHz
F_{SW-MAX}	Maximum Switching Frequency			350		kHz
t_{ON-MIN}	Minimum Switch On-time			140		ns
Diode Thermal Compensation						
V_{TC}	TC Voltage	I_{TC} = ±10 μA, T_J = 25°C		1.2	1.27	V
Power Switches						
$R_{DS(on)}$	MOSFET On-State Resistance	I_{SW} = 100 mA		0.43		Ω
Soft-Start and Bias						
I_{SS}	SS Ext Capacitor Charging Current			5		μA
t_{SS}	Internal SS Time			6		ms
$V_{BIAS-UVLO-RISE}$	BIAS Enable Voltage	$V_{SS/BIAS}$ rising		5.5	5.7	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{BIAS-UVLO-HYST}$	BIAS UVLO Hysteresis	$V_{SS/BIAS}$ falling		156		mV
Current Limit						
I_{SW_LIMIT}	Peak Current Limit Threshold		1.3	1.5	1.7	A
Junction Temperature Protection						
T_{SD}	Thermal Shutdown Protection Threshold	T_J rising		170		ºC
T_{SD_HYS}	Thermal Shutdown Hysteresis	T_J falling below T_{SD}		20		ºC

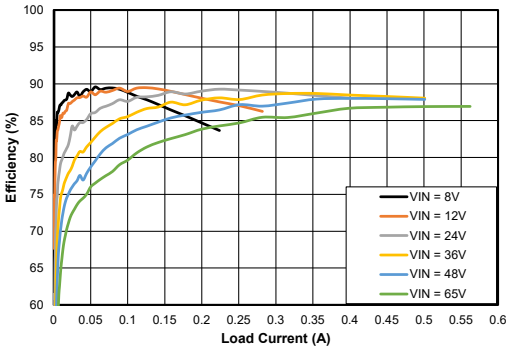
Typical Performance Characteristics

All test conditions: V_{IN} = 24 V, T_A = +25°C, unless otherwise noted.



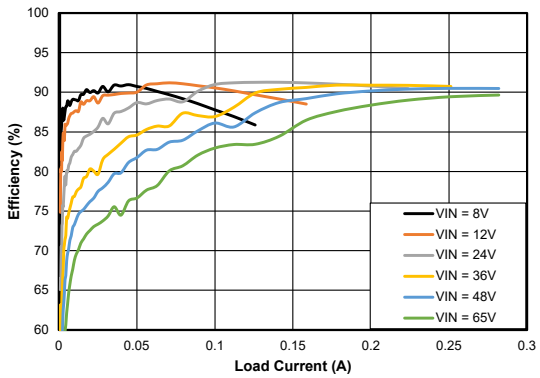
V_{OUT} = 5 V

Figure 1. Efficiency vs. Load Current



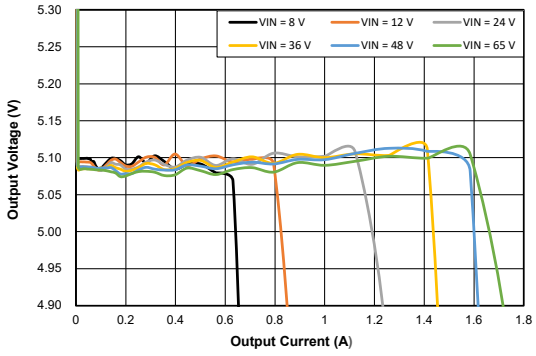
VOUT = 14 V

Figure 2. Efficiency vs. Load Current



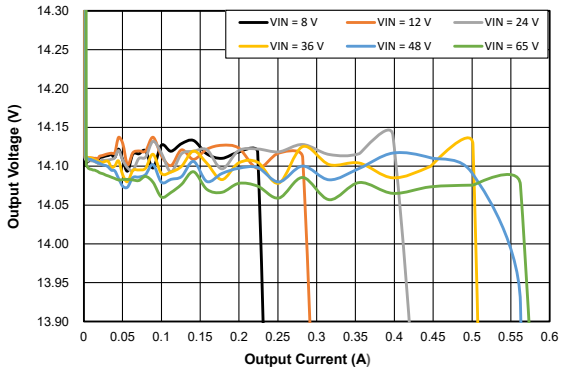
V_{OUT} = 24 V

Figure 3. Efficiency vs. Load Current



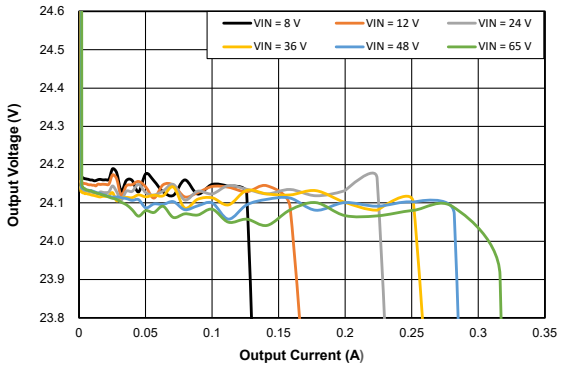
V_{OUT} = 5 V

Figure 4. Output Voltage vs. Load Current



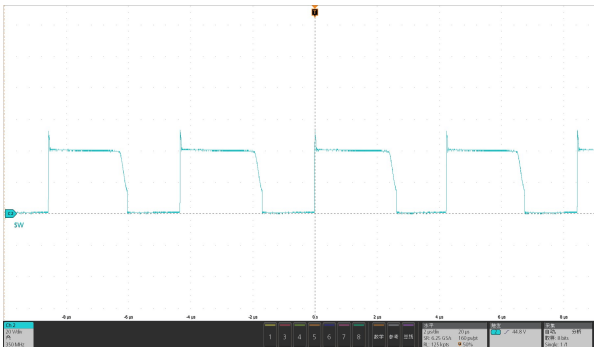
V_{OUT} = 14 V

Figure 5. Output Voltage vs. Load Current



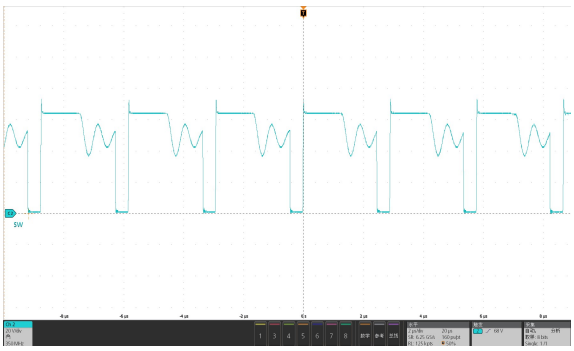
V_{OUT} = 24 V

Figure 6. Output Voltage vs. Load Current



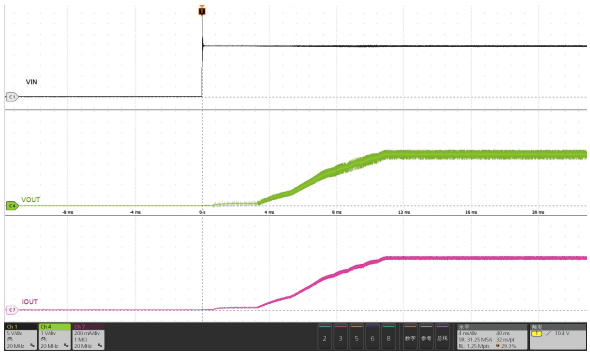
V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 1 A

Figure 7. Switching Waveform in BCM



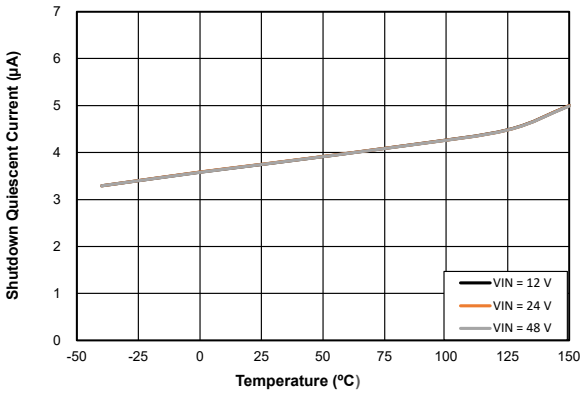
V_{IN} = 48 V, V_{OUT} = 5 V, I_{OUT} = 1 A

Figure 8. Switching Waveform in DCM



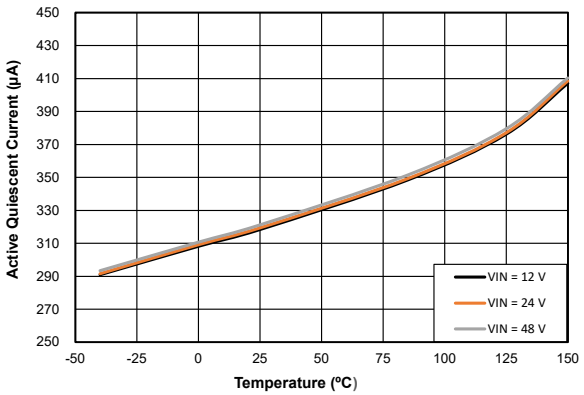
V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 1 A (5ohm resistor load)

Figure 9. Startup Waveform by V_{IN}



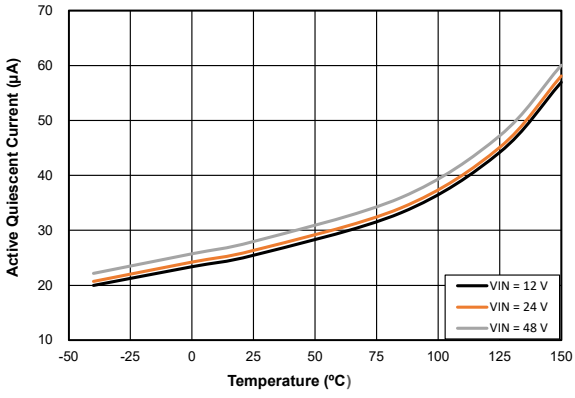
V_{EN} = 0 V

Figure 10. Shutdown Quiescent Current vs. Temperature



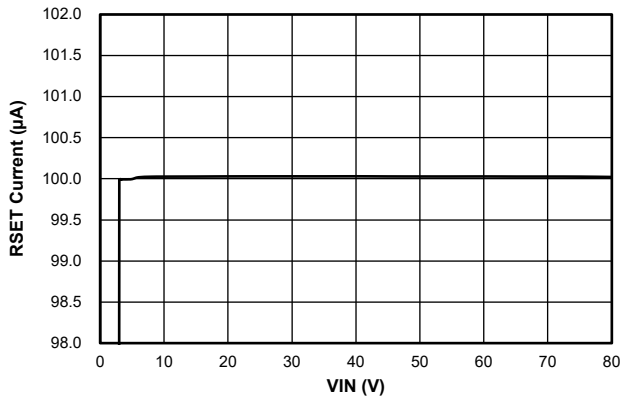
V_{EN} = 2 V

Figure 11. Active Quiescent Current vs. Temperature



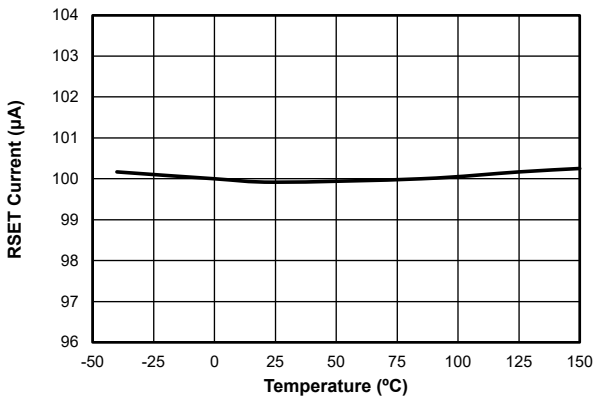
V_{EN} = 2 V, $V_{SS/BIAS}$ = 6 V

Figure 12. Active Quiescent Current with BIAS vs. Temperature



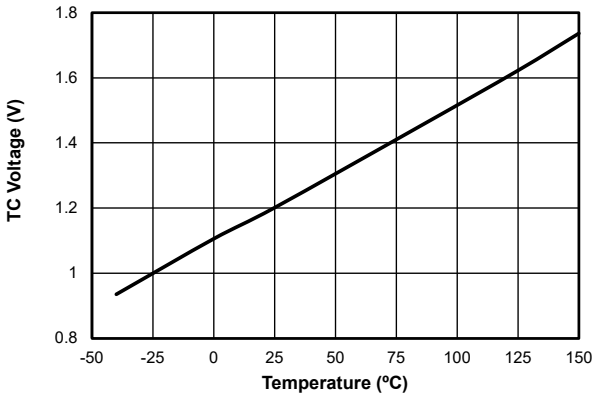
RSET = 12.1 kΩ

Figure 13. RSET Current vs. Input Voltage



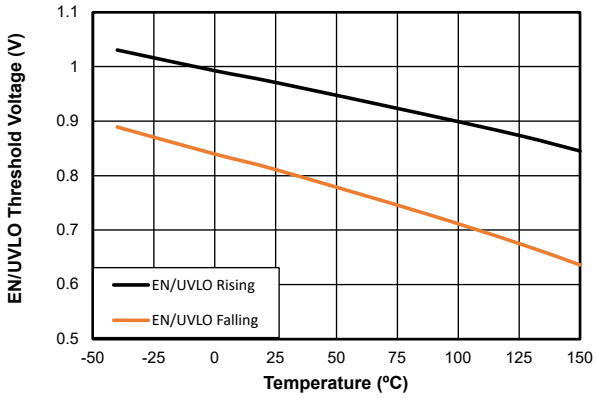
V_{IN}= 24 V, RSET = 12.1 kΩ

Figure 14. RSET Current vs. Temperature



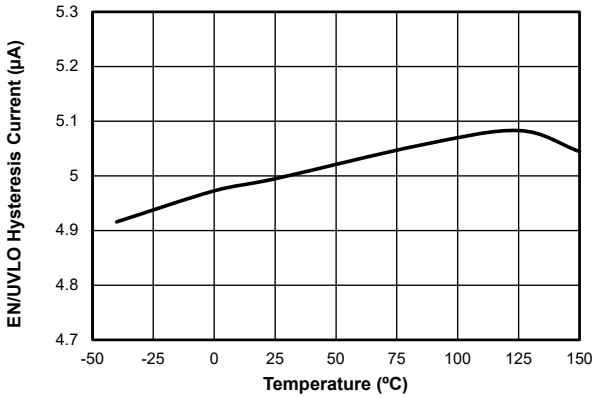
V_{IN}= 24 V, RSET = 12.1 kΩ

Figure 15. TC Voltage vs. Temperature



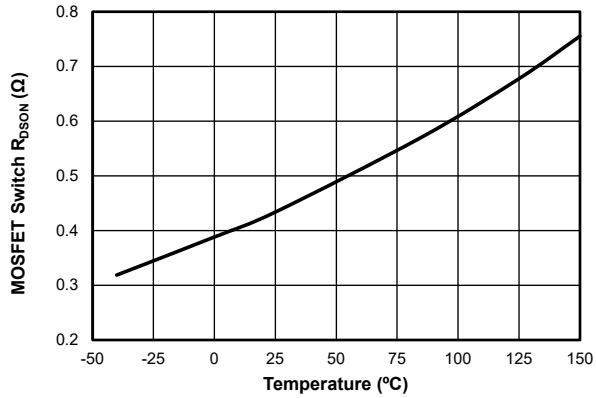
V_{IN}= 24 V, RSET = 12.1 kΩ

Figure 16. EN/UVLO Threshold Voltage vs. Temperature



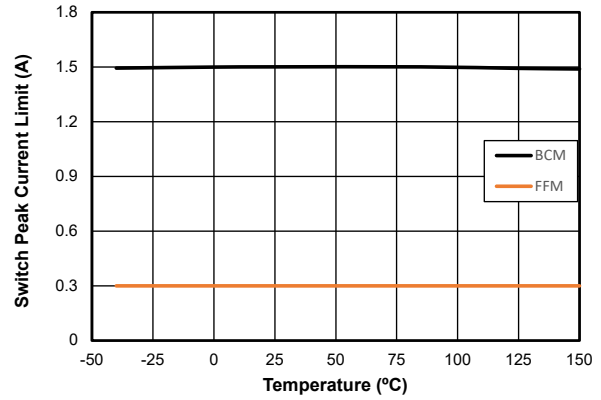
V_{IN}= 24 V, RSET = 12.1 kΩ

Figure 17. EN/UVLO Hysteresis Current vs. Temperature



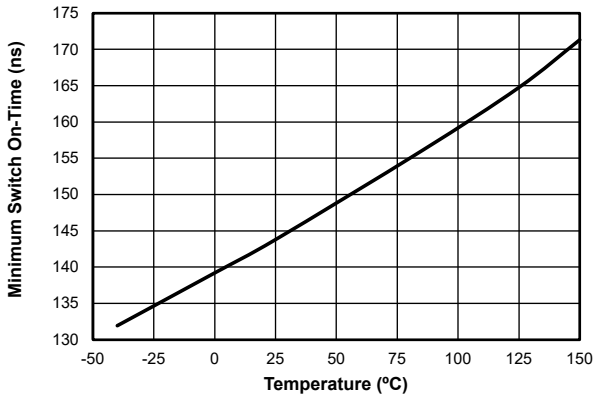
V_{IN}= 24 V, RSET = 12.1 kΩ

Figure 18. Switch Rds (on) vs. Temperature



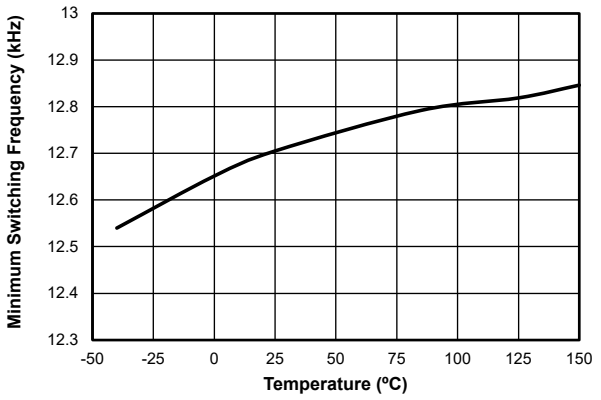
V_{IN}= 24 V, RSET = 12.1 kΩ

Figure 19. Switch Peak Current Limits vs. Temperature



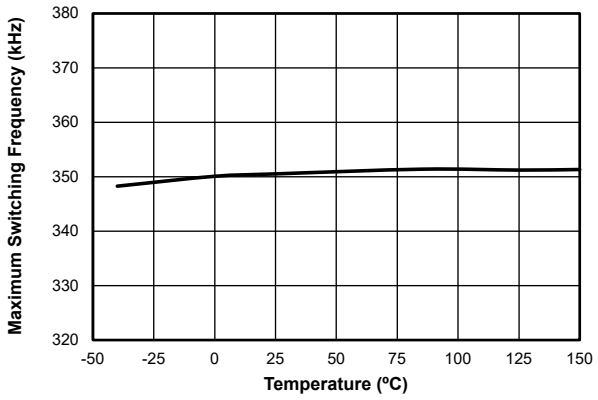
V_{IN}= 24 V, RSET = 12.1 kΩ

Figure 20. Minimum Switch On-Time vs. Temperature



V_{IN}= 24 V, RSET = 12.1 kΩ

Figure 21. Minimum Switching Frequency vs. Temperature



V_{IN}= 24 V, RSET = 12.1 kΩ

Figure 22. Maximum Switching Frequency vs. Temperature

Detailed Description

Overview

The TPQ5180Q primary-side regulated (PSR) flyback converter is a high-density, cost-effective solution for automotive and industrial systems requiring less than 7 W of isolated DC/DC power. This compact, easy-to-use flyback converter with low I_Q can be applied over a wide input voltage range from 4.5 V to 75 V, with operation down to 3.5 V after startup. The innovative frequency and current amplitude modulation enables high conversion efficiency across the entire load and line range. Primary-side regulation of the isolated output voltage using sampled values of the primary winding voltage eliminates the need for an opto-coupler or an auxiliary transformer winding for feedback. Regulation performance that rivals that of traditional opto-coupler solutions is achieved without associated cost, solution size and reliability concerns. The TPQ5180Q converter serves a wide range of applications including automotive on-board chargers and IGBT-based motor drives for HEV/EV systems.

Functional Block Diagram

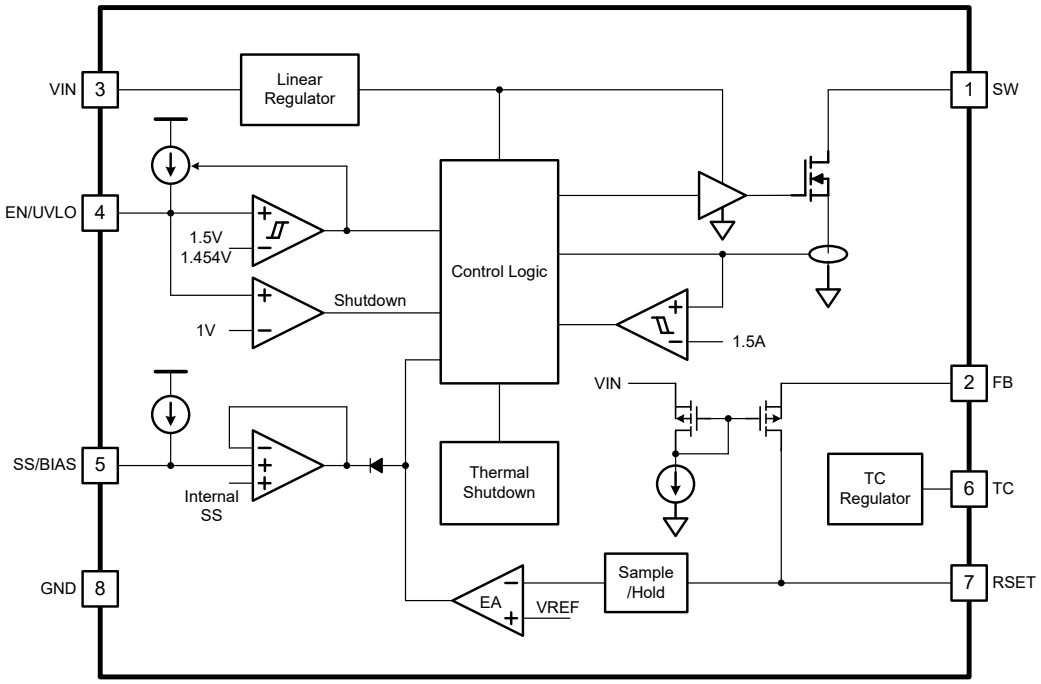


Figure 23. Functional Block Diagram

Feature Description

Integrated Power MOSFET

The TPQ5180Q is a flyback DC/DC converter with an integrated 100-V, 1.5-A N-channel power MOSFET. During the MOSFET on-time, the transformer primary current increases from zero with slope V_{IN} / L_{PR} (where L_{PR} is the transformer primary-referred magnetizing inductance) while the output capacitor supplies the load current. When the low-side MOSFET is turned off by the control logic, the SW voltage V_{SW} swings up to approximately V_{IN} + (N_{PS} × V_{OUT}), where N_{PS} = N_P / N_S is the primary-to-secondary turns ratio of the transformer. The magnetizing current flows in the secondary side through the flyback

diode, charging the output capacitor and supplying currents to the load. Duty cycle D is defined as t_{ON} / t_{SW}, where t_{ON} is the MOSFET conduction time and t_{SW} is the switching period.

PSR Flyback Modes of Operation

The TPQ5180Q uses a variable-frequency, peak current-mode (VFPCM) control architecture with three possible modes of operation as shown in Figure 24.

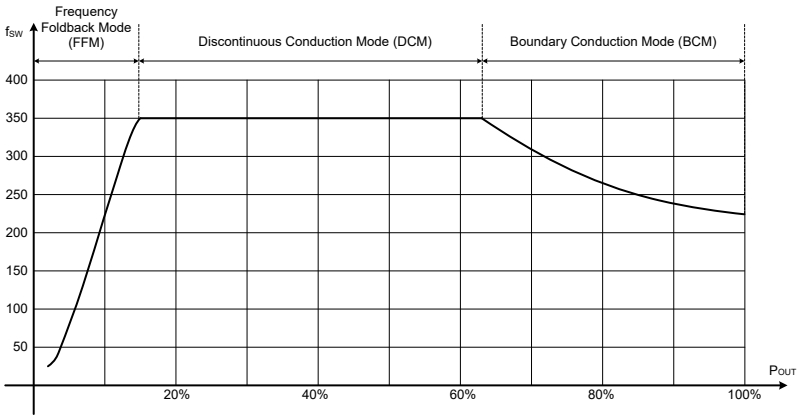


Figure 24. The Switching Frequency of Three Operation Modes Varied with Load

The TPQ5180Q operates in boundary conduction mode (BCM) at heavy loads. The power MOSFET turns on when the current in the secondary winding reaches zero; And the MOSFET turns off when the peak primary current reaches the level dictated by the output of the internal error amplifier. As the load decreases, the frequency increases to maintain BCM operation. The duty cycle of the flyback converter is given by Equation 1, where V_D is the forward voltage drop of the flyback diode when its current approaches zero.

$$D_{BCM} = \frac{(V_{OUT} + V_D) \times N_{PS}}{V_{IN} + (V_{OUT} + V_D) \times N_{PS}} \quad (1)$$

The output power in BCM is given by Equation 2, where the applicable switching frequency and peak primary current in BCM are specified by Equation 3 and Equation 4, respectively.

$$P_{OUT(BCM)} = \frac{L_{PR} \times I^2_{PRI\_PK(BCM)} \times f_{SW(BCM)}}{2} \quad (2)$$

$$f_{SW(BCM)} = \frac{1}{I_{PRI\_PK(BCM)} \times \left(\frac{L_{PR}}{V_{IN}} + \frac{L_{PR}}{N_{PS} \times (V_{OUT} + V_D)} \right)} \quad (3)$$

$$I_{PRI\_PK(BCM)} = \frac{2 \times (V_{OUT} + V_D) \times I_{OUT}}{V_{IN} \times D} \quad (4)$$

As the load decreases, the TPQ5180Q clamps the maximum switching frequency to 350 kHz, and the converter enters discontinuous conduction mode (DCM). The power delivered to the output in DCM is proportional to the peak primary current squared as given by Equation 5 and Equation 6. Thus, as the load decreases, the peak current drops to maintain the regulation at 350-kHz switching frequency.

$$P_{OUT(DCM)} = \frac{L_{PR} \times I^2_{PRI\_PK(DCM)} \times f_{SW(DCM)}}{2} \quad (5)$$

$$I_{PRI\_PK(DCM)} = \sqrt{\frac{2 \times I_{OUT} \times (V_{OUT} + V_D)}{L_{PR} \times f_{SW(DCM)}}} \quad (6)$$

$$D_{DCM} = \frac{L_{PR} \times I_{PRI\_PK(DCM)} \times f_{SW(DCM)}}{V_{IN}} \quad (7)$$

At even lighter loads, the primary-side peak current set by the internal error amplifier decreases to a minimum level of 0.3 A, or 20% of its 1.5-A peak value, and the MOSFET off-time extends to maintain the output load requirements. The system operates in frequency foldback mode (FFM), and the switching frequency decreases as the load current drops. Other than a fault condition, the lowest frequency of operation of the TPQ5180Q is 12 kHz, which sets a minimum load requirement of approximately 0.5% full load.

Setting the Output Voltage

To minimize output voltage regulation error, the TPQ5180Q senses the reflected secondary voltage when the secondary current reaches zero. The feedback (FB) resistor which is connected between the SW pin and the FB pin as shown in Figure 27, is determined using Equation 8, where R_{SET} is nominally 12.1 kΩ.

$$R_{FB} = (V_{OUT} + V_D) \times N_{PS} \times \frac{R_{SET}}{V_{REF}} \quad (8)$$

Diode Thermal Compensation

The TPQ5180Q employs a unique thermal compensation circuit that adjusts the feedback setpoint based on the thermal coefficient of the forward voltage drop of the flyback diode. Even though the output voltage is measured when the secondary current is effectively zero, there is still a non-zero forward voltage drop associated with the flyback diode. Select the thermal compensation resistor using Equation 9.

$$R_{TC} = \frac{R_{FB}}{N_{PS}} \times \frac{4.1mV/°C}{TC_{DIODE}} \quad (9)$$

The temperature coefficient of the diode voltage drop may not be explicitly provided in the diode datasheet, so the effective value can be estimated based on the measured output voltage shift over temperature when the TC resistor is not installed.

Control Loop Error Amplifier

The inputs of the error amplifier include a level-shifted version of the FB voltage and an internal 1.21-V reference set by the resistor at the RSET pin. A type-2 internal compensation network stabilizes the converter. In BCM operation, an on-time interval is initiated when the output voltage is in regulation and the secondary current reaches zero. The power MOSFET is subsequently turned off when an amplified version of the peak primary current exceeds the error amplifier output.

Precision Enable

The precision EN/UVLO input supports adjustable input under-voltage lockout (UVLO) with hysteresis for application specific power-up and power-down requirements. The EN/UVLO pin connects to a comparator with a 1.5-V reference voltage and 46-mV hysteresis. An external logic signal can be used to drive the EN/UVLO input to toggle the output on and off for system sequencing or protection. The simplest way to enable the TPQ5180Q is to connect the EN/UVLO pin directly to V_{IN}. This allows the TPQ5180Q to start up when V_{IN} is within its valid operating range. However, many applications benefit from using a resistor divider R_{UVLO_T} and R_{UVLO_B} as shown in Figure 25 to establish a precision input UVLO level.

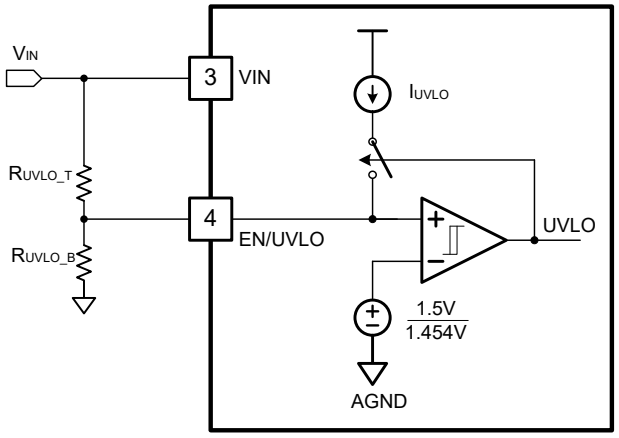


Figure 25. Programmable Input Voltage UVLO with Hysteresis

Use Equation 10 and Equation 11 to calculate resistor divider for the desired input UVLO voltages.

$$R_{UVLO\_T} = \frac{V_{IN(ON)} \times \frac{V_{UVLO\_F}}{V_{UVLO\_R}} - V_{IN(OFF)}}{I_{UVLO\_HYS}} \quad (10)$$

$$R_{UVLO\_B} = R_{UVLO\_T} \times \frac{V_{UVLO\_R}}{V_{IN(ON)} - V_{UVLO\_R}} \quad (11)$$

Where

- $V_{IN(ON)}$ is the desired start-up voltage of the converter;
- $V_{IN(OFF)}$ is the desired turn-off voltage of the converter.

The TPQ5180Q also provides a low quiescent current shutdown mode when the EN/UVLO voltage is pulled below typical 1 V. If the EN/UVLO voltage is below this hard shutdown threshold, the internal LDO regulator powers off, and the internal bias-supply rail collapses, shutting down the bias currents of the TPQ5180Q. The TPQ5180Q operates in the standby mode when the EN/UVLO voltage is between the hard shutdown and precision-enable thresholds.

Configurable Soft Start

The TPQ5180Q has a flexible, easy-to-use and soft-start control pin, SS/BIAS. The soft-start feature prevents the inrush current from impacting the TPQ5180Q and the input supply when power is first applied. This is achieved by controlling the voltage at the output of the internal error amplifier. Soft start is achieved by slowly ramping up the target regulation voltage when the device is first enabled or powered up. Selectable and adjustable start-up timing options include a 6-ms internally fixed soft start time and an externally programmable soft start time.

The simplest way to use the TPQ5180Q is to leave the SS/BIAS pin floating. The TPQ5180Q employs an internal soft-start control ramp and starts up to the regulated output voltage in 6 ms.

In applications with a large amount of output capacitance, higher V_{OUT}, or other special requirements, the soft-start time can be extended by connecting an external capacitor C_{SS} from the SS/BIAS pin to GND. A longer soft-start time further reduces the supply current needed to charge the output capacitors while sourcing the required load current. When the EN/UVLO voltage exceeds the UVLO rising threshold and a delay of 20 µs expires, an internal current source I_{SS} of 5 µA charges C_{SS} and generates a ramp to control the primary current amplitude. Calculate the soft-start capacitance for a desired soft-start time, t_{SS}, using Equation 12.

$$C_{SS} = 5(\mu A) \times t_{SS} \quad (12)$$

External Bias Supply

The TPQ5180Q has an external bias supply feature that reduces the input quiescent current and increases efficiency. When the voltage at the SS/BIAS pin exceeds a rising threshold of 5.5 V, the bias power for the internal LDO regulator can be derived from an external voltage source or from a transformer auxiliary winding as shown in Figure 26. With a bias supply connected, the TPQ5180Q then uses its internal soft-start ramp to control the primary current during start-up.

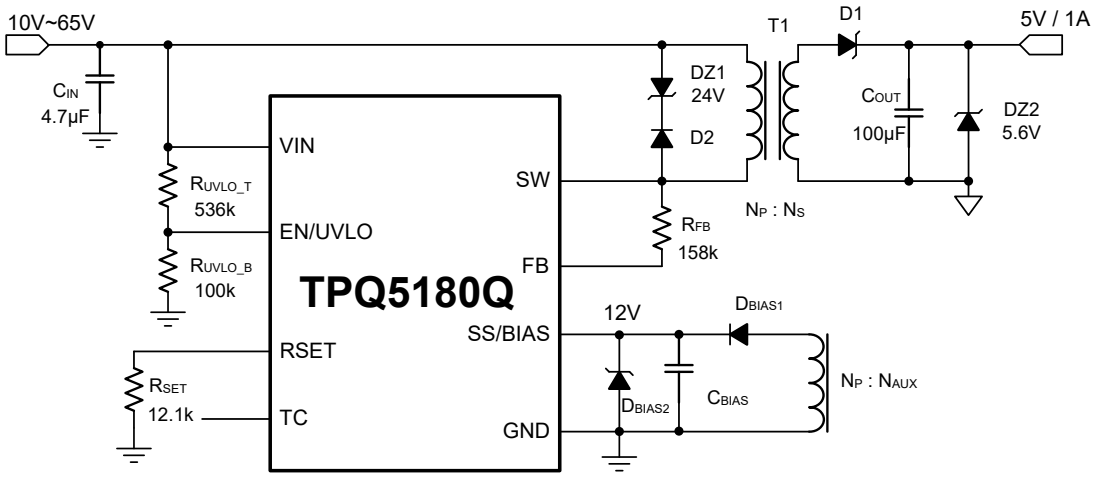


Figure 26. External Bias Supply Using Transformer Auxiliary Winding

When using a transformer auxiliary winding for the bias power, the total leakage current related to diodes D_{BIAS1} and D_{BIAS2} in Figure 26 should be less than 1 µA across the full operating temperature range.

Minimum On-Time and Off-Time

When the internal power MOSFET is turned off, the leakage inductance of the transformer resonates with the SW node parasitic capacitance. The resultant ringing behavior can be excessive with large transformer leakage inductance and may corrupt the secondary zero-current detection. To prevent such a situation, a minimum switch off-time, designated as $t_{OFF-MIN}$, of maximum 450 ns is set internally to ensure proper functionality. This sets a lower limit for the transformer magnetizing inductance as discussed in the Typical Application section.

Furthermore, noise effects as a result of the power MOSFET turn-on can impact the internal current sense circuit measurement. To mitigate this effect, the TPQ5180Q provides a blanking time after the MOSFET turns on. This blanking time forces a minimum on-time, t_{ON-MIN}, of 140 ns.

Overcurrent Protection

In case of an overcurrent condition on the isolated output(s), the output voltage drops lower than the regulation level since the maximum power delivered is limited by the peak current capability on the primary side. The peak primary current is maintained at 1.5 A (plus an amount related to the 100-ns propagation delay of the current limit comparator) until the output decreases to the secondary diode voltage drop to impact the reflected signal on the primary side. At this point, the TPQ5180Q assumes the output cannot be recovered and re-calibrates its switching frequency to 12 kHz until the overload condition is removed. The TPQ5180Q responds with similar behavior to an output short circuit condition.

For a given input voltage, Equation 13 gives the maximum output current prior to the engagement of overcurrent protection. The typical threshold value for $I_{SW-LIMIT}$ from Electrical Characteristics is 1.5 A.

$$I_{OUT} = \frac{I_{SW\_LIMIT}}{2 \times \left(\frac{V_{OUT} + V_D}{V_{IN}} + \frac{1}{N_{PS}} \right)} \quad (13)$$

Thermal Shutdown

Thermal shutdown is an integrated self-protection to limit the junction temperature and prevent any damage related to overheating. When the junction temperature exceeds 170°C, the thermal shutdown turns off the device to prevent further power dissipation and temperature rise. The junction temperature decreases after the shutdown, and the TPQ5180Q restarts when the junction temperature falls to 150°C.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPQ5180Q requires only a few external components to convert from a wide range of supply voltages to one or more isolated output rails. The following sections discuss the design procedures for both single- and dual-output implementations using specific circuit design examples.

As mentioned previously, the TPQ5180Q also integrates several optional features to meet system design requirements, including precision enable, input UVLO, programmable soft start, output voltage thermal compensation, and external bias supply connection. Each application incorporates these features as needed for a more comprehensive design.

The application circuits detailed in Typical Application show TPQ5180Q configuration options suitable for several application cases.

Typical Application

Wide VIN, Low I_Q PSR Flyback Converter Rated at 5 V, 1 A

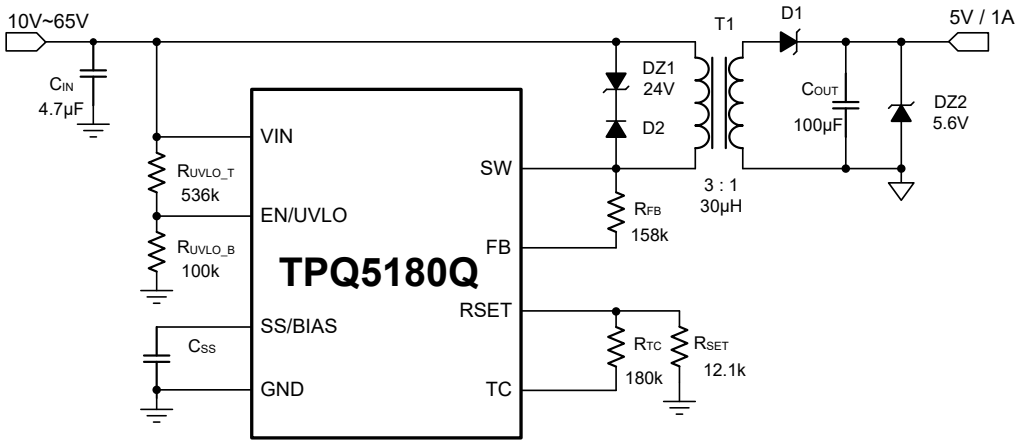


Figure 27. 24-V Input, 5-V/1-A Output Application Circuit

Flyback Transformer

Choose a turns ratio based on an approximate 60% max duty cycle at the minimum input voltage using Equation 14, rounding up or down as needed.

$$N_{PS} = \frac{D_{MAX}}{1 - D_{MAX}} \times \frac{V_{IN(MIN)}}{V_{OUT} + V_D} = 3 \quad (14)$$

Select a magnetizing inductance based on the minimum off-time constraint using Equation 15. Choose a value of 30 μH with a saturation current of minimum 2 A for this application.

$$L_{PR} > \frac{(V_{OUT} + V_D) \times N_{PS} \times t_{OFF(MIN)}}{I_{PRI\_PK(FFM)}} = 23.9\mu H \quad (15)$$

Note that a higher magnetizing inductance provides a larger operating range for BCM and FFM, but the leakage inductance may increase based on a higher number of primary turns, N_P. The primary and secondary winding RMS currents are given by Equation 16 and Equation 17, respectively.

$$I_{PRI(RMS)} = \sqrt{\frac{D}{3}} \times I_{PRI\_PK} \quad (16)$$

$$I_{SEC(RMS)} = \sqrt{\frac{2 \times I_{OUT} \times I_{PRI\_PK} \times N_{PS}}{3}} \quad (17)$$

Find the maximum output current for a given turns ratio using Equation 18, where the typical value for $I_{PRI-PK(max)}$ is the switch current peak threshold of 1.5 A. Iterate by increasing the turns ratio if the output current capability is too low at the minimum input voltage.

$$I_{OUT(MAX)} = \frac{I_{PRI\_PK(MAX)}}{2 \times \left(\frac{V_{OUT} + V_D}{V_{IN}} + \frac{1}{N_{PS}}\right)} \quad (18)$$

Flyback Diode

The flyback diode reverse voltage is given by Equation 19.

$$V_{D\_REV} \geq \frac{V_{IN(MAX)}}{N_{PS}} + V_{OUT} = 27(V) \quad (19)$$

Select a 40-V, 3-A Schottky diode for this application to account for inevitable diode voltage overshoot and ringing related to the resonance of transformer leakage inductance and diode parasitic capacitance. Connect an appropriate RC snubber circuit (for example, 100 Ω and 22 pF) across the flyback diode if needed. Also, choose a flyback diode with a current rating greater than the maximum peak secondary winding current of N_{PS}x$I_{PRI-PK(MAX)}$.

Zener Clamp Circuit

Connect a diode-Zener clamping circuit across the primary winding to limit the peak switch-node voltage after MOSFET turn-off below the maximum level of 95 V, as given by Equation 20.

$$V_{DZ1} < V_{SW(MAX)} - V_{IN(MAX)} \quad (20)$$

Choose the Zener diode with the clamp voltage of approximately 1.5 times the reflected output voltage, as specified by Equation 21. Provide a balance between the maximum SW voltage excursion and the leakage inductance demagnetization time.

$$V_{DZ1} = 1.5 \times N_{PS} \times (V_{OUT} + V_D) = 24V \quad (21)$$

Select an ultra-fast switching diode or Schottky diode for D2 with rated voltage greater than the maximum input voltage and with low forward recovery voltage drop.

Output Capacitor

The output capacitor determines the voltage ripple at the converter output, limits the voltage excursion during a load transient, and sets the dominant pole of the small-signal response of the converter. For a flyback converter specifically, the output capacitor supplies the load current when the main switch is on, and therefore the output voltage ripple is a function of load current and duty cycle.

$$C_{OUT} \geq \frac{I_{OUT(MAX)}}{\Delta V_{OUT}} \times \frac{L_{PR} \times I_{PRI\_PK(MAX)}}{V_{IN}} \quad (22)$$

Select an output capacitance using Equation 22 to limit the ripple voltage amplitude to less than 1% of the output voltage at the minimum input voltage.

Substitute the maximum load current at the minimum input voltage from Equation 18, transformer inductance, peak switch current and peak-to-peak ripple voltage specification gives C_{OUT} greater than 72 µF.

Pay attention to the voltage coefficient of ceramic capacitors, and select a 100-µF, 6.3-V capacitor in 1210 case size with X5R or better dielectric. Equation 23 gives the output capacitor RMS ripple current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{2 \times N_{PS} \times I_{PRI\_PK}}{3 \times I_{OUT}} - 1} \tag{23}$$

Input Capacitor

Select an input capacitance using Equation 24 to limit the ripple voltage amplitude to less than 5% of the input voltage when operating at the nominal input voltage.

$$C_{IN} \geq \frac{I_{PRI\_PK} \times D \times \left(1 - \frac{D}{2}\right)^2}{2 \times f_{SW} \times \Delta V_{IN}} \tag{24}$$

Substitute the input current at full load, switching frequency, peak primary current and peak-to-peak ripple specification gives C_{IN}greater than 2 µF. Pay attention to the voltage coefficient of ceramic capacitors, and select a 4.7-µF, 100-V ceramic input capacitor with X7S dielectric in 1210 case size. Equation 25 gives the input capacitor RMS ripple current.

$$I_{CIN(RMS)} = \frac{D \times I_{PRI\_PK}}{2} \times \sqrt{\frac{4}{3 \times D} - 1} \tag{25}$$

Feedback Resistor

Select a feedback resistor, designated R_{FB}, of 158 kΩ based on the secondary winding voltage at the end of the flyback conduction interval (the sum of the 5-V output voltage and the Schottky diode forward voltage drop) reflected by the transformer turns ratio of 3:1. The forward voltage drop of the flyback diode is 0.3 V as its current approaches zero.

$$R_{FB} = (V_{OUT} + V_D) \times N_{PS} \times \frac{R_{SET}}{V_{REF}} = 158k\Omega \tag{26}$$

Thermal Compensation Resistor

Select a resistor for output voltage thermal compensation, designated R_{TC}, based on Equation 27.

$$R_{TC} = \frac{R_{FB}}{N_{PS}} \times \frac{4.1mV/°C}{TC_{DIODE}} = 180k\Omega \tag{27}$$

UVLO Resistor Divider

Given $V_{IN(ON)}$ and $V_{IN(OFF)}$ as the input voltage turn-on and turn-off thresholds of 9.5 V and 6.5 V, respectively, select the upper and lower UVLO resistors using the following expressions:

$$R_{UVLO\_T} = \frac{V_{IN(ON)} \times \frac{V_{UVLO\_F}}{V_{UVLO\_R}} - V_{IN(OFF)}}{I_{UVLO\_HYS}} = 536k\Omega \tag{28}$$

$$R_{UVLO\_B} = R_{UVLOT} \times \frac{V_{UVLO\_R}}{V_{IN(ON)} - V_{UVLO\_R}} = 100k\Omega \tag{29}$$

Soft-Start Capacitor

Connect an external soft-start capacitor for a specific soft-start time. In this example, select a soft-start capacitance of 47 nF based on Equation 12 to achieve a soft-start time of 9 ms.

Application Examples

PSR Flyback Converter with Dual Outputs of 15 V and −7.7 V at 200 mA

The schematic diagram of a dual-output flyback converter intended for isolated IGBT and SiC MOSFET gate drive power supply applications is given in Figure 28.

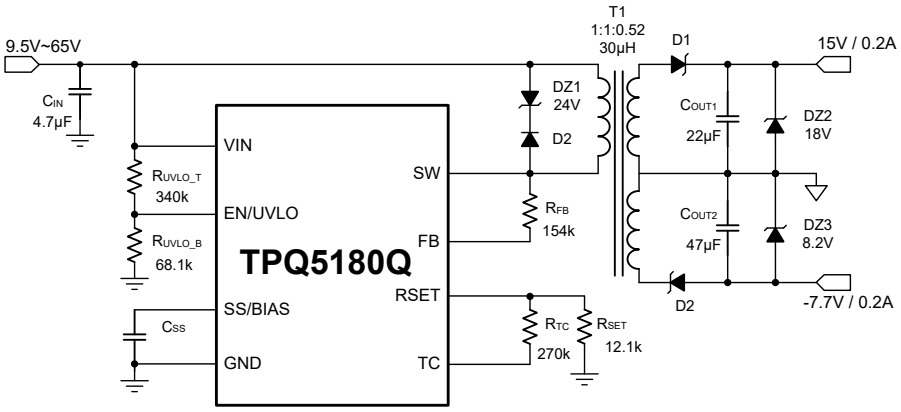


Figure 28. 48-V Input, 15-V/0.2-A and −7.7-V/0.2-A Output Application Circuit

PSR Flyback Converter with Stacked Dual Outputs of 24 V and 5 V

The schematic diagram of a dual-output flyback converter with high-voltage secondary stacked on the low-voltage secondary winding is given in Figure 29. This configuration reduces the number of turns for the high-voltage output, resulting in lower secondary-to-secondary leakage inductance for improved output voltage cross regulation.

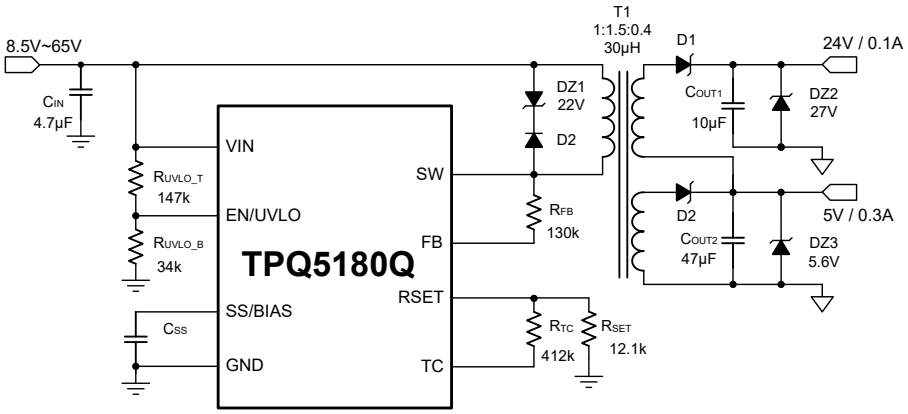


Figure 29. 24-V Input, 24-V/0.1-A and 5-V/0.3-A Output Application Circuit

Layout

Layout

The performance of any switching converter depends as much upon the PCB layout as it does the component selection. The following guidelines are provided to assist with designing a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

Layout Guideline

PCB layout is a critical for good power supply design. There are several paths that conduct high slew-rate currents or voltages that can interact with transformer leakage inductance or parasitic capacitance to generate noise and EMI or degrade the performance of the power supply.

1. Bypass the VIN pin to GND with a low-ESR ceramic capacitor, preferably of X7R or X7S dielectric. Place C_{IN} as close as possible to the TPQ5180Q VIN and GND pins. Ground return paths for the input capacitor(s) must consist of localized top-side planes that connect to the GND pin and exposed PAD.
2. Minimize the loop area formed by the input capacitor connections and the VIN and GND pins.
3. Locate the transformer close to the SW pin. Minimize the area of the SW trace or plane to prevent excessive e-field or capacitive coupling.
4. Minimize the loop area formed by the diode-Zener clamp circuit connections and the primary winding terminals of the transformer.
5. Minimize the loop area formed by the flyback rectifying diode, output capacitor, and the secondary winding terminals of the transformer.
6. Tie the GND pin directly to the power pad under the device and to a heat-sinking PCB ground plane.
7. Use a ground plane in one of the middle layers as a noise shielding and heat dissipation path.
8. Have a single-point ground connection to the plane. Route the return connections for the reference resistor, soft-start, and enable components directly to the GND pin. This prevents any switched or load currents from flowing in analog ground traces. If not properly handled, poor grounding results in degraded load regulation or erratic output voltage ripple behavior.
9. Make V_{IN+}, V_{OUT+} and ground bus connections short and wide. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
10. Minimize trace length to the FB pin. Locate the feedback resistor close to the FB pin.
11. Locate components R_{SET}, R_{TC} and C_{SS} as close as possible to their respective pins. Route with minimal trace lengths.
12. Place a capacitor between input and output return connections to route common-mode noise currents directly back to their source.
13. Provide adequate heatsinking for the TPQ5180Q to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed PAD to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes. The connection to V_{OUT+} provides heatsinking for the flyback diode.

Layout Example

The Figure 30 shows the location of external components of the typical single output appication circuit as they appears on the PCB.

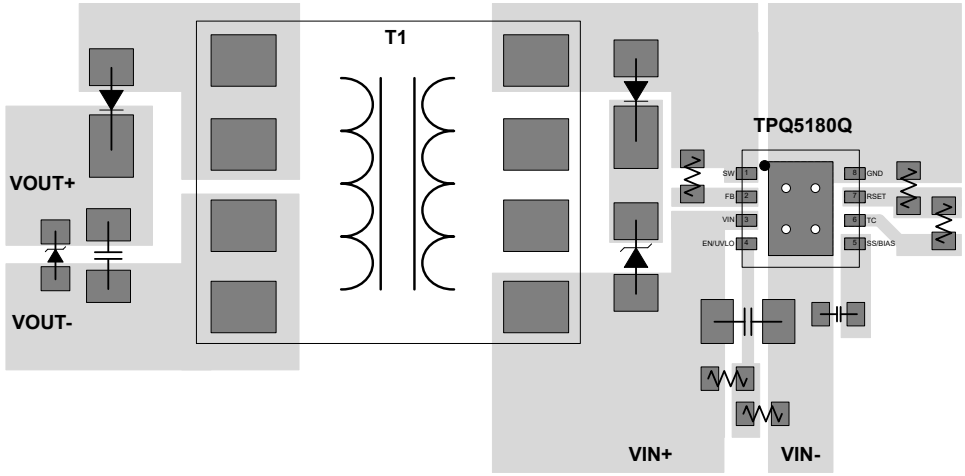
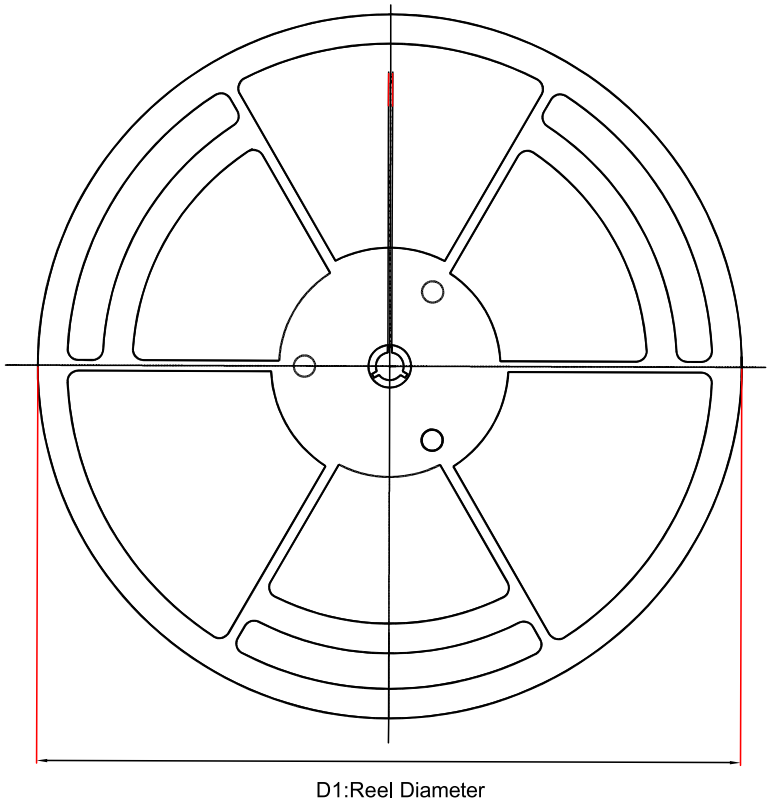
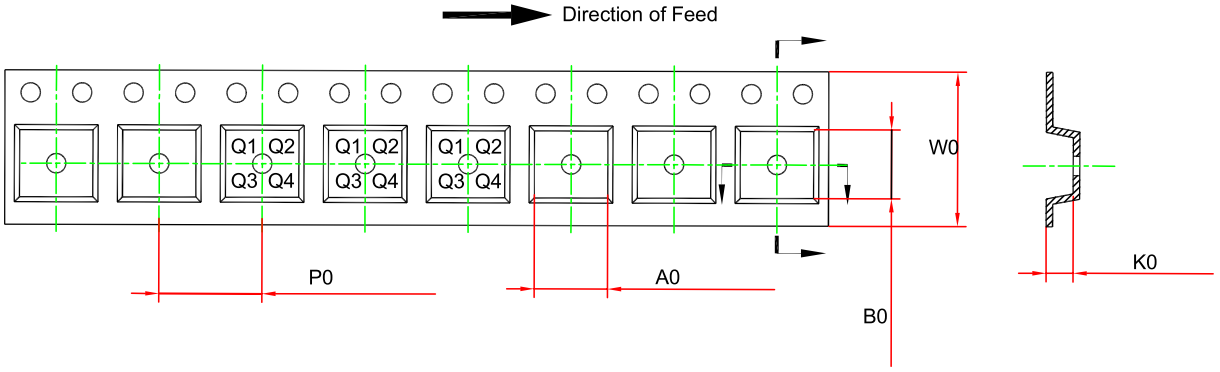


Figure 30. TPQ5180Q PCB Layout Example

Tape and Reel Information



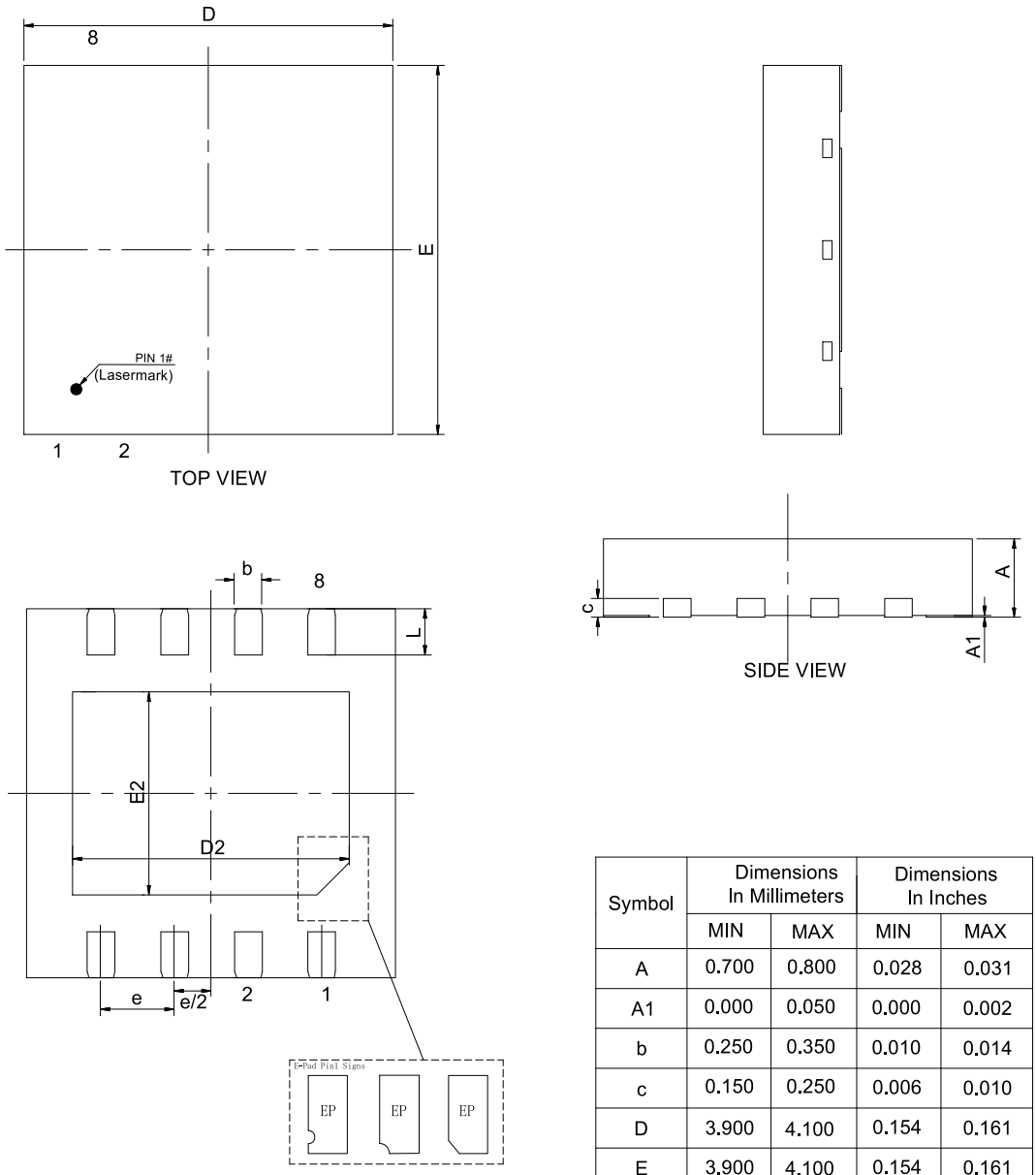


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPQ5180Q-DFMR-S	DFN4X4-8	330	17.6	4.3	4.3	1.1	8	12	Q1

Package Outline Dimensions

DFN4X4-8

Package Outline Dimensions DFM(DFN4X4-8-B)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.250	0.350	0.010	0.014
c	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D2	2.900	3.100	0.114	0.122
E2	1.880	2.080	0.074	0.082
e	0.800 BSC		0.031 BSC	
L	0.300	0.500	0.012	0.020

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPQ5180Q-DFMR-S	−40 to 125°C	DFN4X4-8	5180Q	2	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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