2.2-MHz Wide Input Nonsynchronous Boost/SEPIC/Flyback Converter

Features

- 2.9-V to 45-V Input Supply Voltage Range
- Minimum Boost Supply Voltage of 1.5 V when V_{IN} > 2.9 V
- Low Shutdown Current (Typical 2.6 μA)
- Low Operating Current (Typical 570 μA)
- Programmable Switching Frequency Range from 100 kHz to 2.2 MHz
- 39-mΩ R_{DSON} Power Switch
- Optional External Clock Synchronization
- ±1% Reference Voltage Accuracy
- Power Good Indicator
- Optional Hiccup Short-Circuit Protection
- Optional Spread-Spectrum to Reduce EMI
- Programmable Input Voltage UVLO
- Adjustable Soft Start Time
- Available in QFN3X3-16 Package

Applications

- Power Module
- Multiple-output Flyback without Optocoupler
- LED Power Supply
- Portable Speaker
- General Boost, SEPIC, Flyback Applications

Description

The TPQ5057x (TPQ5057 or TPQ50571) is a wide-input-range, non-synchronous boost converter with an integrated 48-V, 7-A power switch. The device can be used in boost, SEPIC, and flyback topologies.

The TPQ5057x uses a peak current control scheme. The device can start up from a minimum voltage of 2.9 V. When the VIN pin is powered by an auxiliary supply voltage above 2.9 V, the supply voltage for the power stage can be down to 1.5 V.

The TPQ5057x integrates a wide input LDO that supports the input voltage of up to 45 V and outputs 5 V at the VCC pin. The switching frequency is either set by an external resistor or synchronized to an external clock from 100 kHz to 2.2 MHz. Switching at 2.2 MHz allows for a small solution size and fast transient response. The TPQ5057x supports the use of an external VCC supply to improve efficiency. Low operating current and pulse-skipping operation improve efficiency at light loads.

The device has built-in protection features such as cycle-by-cycle current limit, overvoltage protection, hiccup mode overload protection, and thermal shutdown. Additional features include low shutdown current, programmable soft start, programmable input UVLO, spread spectrum, and power-good indicator.

The TPQ5057x is available in a 3-mm x 3-mm, 16-pin QFN3x3 package.

Typical Application Circuit

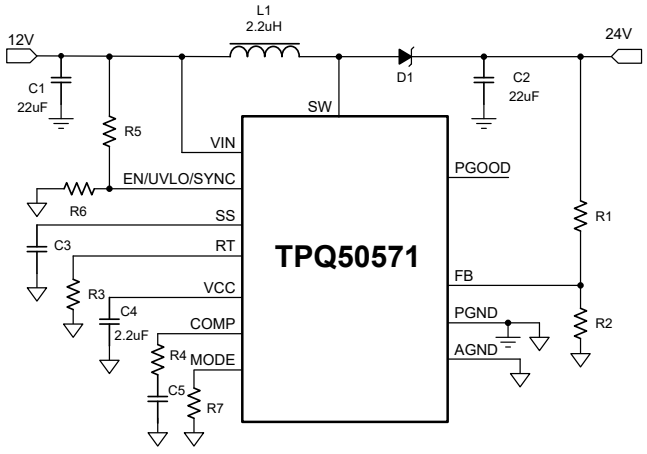


Table of Contents

Product Family Table

Part Number	Minimum Current Limit	Package
TPQ5057 (1)	6.5 A	QFN3x3-16
TPQ50571	5.3 A	QFN3x3-16

(1) Future product

Revision History

Date	Revision	Notes
2025-02-25	Rev. A.0	Initial release

Pin Configuration and Functions

TPQ5057x

QFN3X3-16

Top View

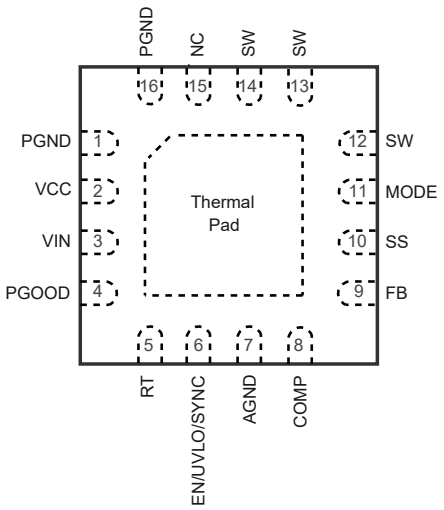


Table 1. Pin Functions: TPQ5057x

Pin No.	Name	I/O	Description
1, 16	PGND	GND	Power ground of the IC. It is connected to the source of the internal MOSFET switch. Connect the PGND pin directly to the AGND pin through a low inductance wide and short path.
2	VCC	P	Output of the internal linear regulator and supply voltage input of the MOSFET driver. Connect a ceramic bypass capacitor from this pin to PGND.
3	VIN	P	Supply voltage input to the VCC linear regulator. Connect a bypass capacitor from this pin to PGND.
4	PGOOD	O	Power-good indicator with open-drain output. Output low impedance when the voltage at the FB pin is below the under-voltage threshold. Output high impedance when the voltage at the FB pin is above the under-voltage threshold.
5	RT	I	Switching frequency setting pin. The switching frequency is programmed by an external resistor between the RT pin and AGND.
6	EN/UVLO/ SYNC	I	1. Enable pin. When the voltage at this pin falls below the enable threshold for more than 40 μs, the device turns off 2. Undervoltage lockout programming pin. The converter start-up and shutdown levels can be programmed by connecting this pin to the center tap of a resistor divider between the supply voltage and ground. 3. The internal clock can be synchronized to an external clock by applying a negative pulse signal to the EN/UVLO/SYNC pin. This pin must not be left floating. Connect to the VIN pin if not used.

7	AGND	GND	Signal ground pin. Connect to the ground plane at one point through a wide and short path.
8	COMP	O	Output of the internal transconductance error amplifier. Connect the external loop compensation RC network between this pin and AGND.
9	FB	I	Inverting input of the error amplifier. Connect to the center tap of a feedback resistor divider between the output and AGND to set output voltage in boost/SEPIC topologies.
10	SS	I	Soft-start time programming pin. An external capacitor between the SS pin and AGND is charged by an internal current source to set the ramp rate of reference voltage for the internal error amplifier during soft start.
11	MODE	I	Operation mode setting by the resistance between the MODE pin and AGND pin 0Ω：Hiccup mode protection is disabled and spread spectrum is disabled. 37.4kΩ: Hiccup mode protection is enabled and spread spectrum is enabled 62.0kΩ: Hiccup mode protection is enabled and spread spectrum is disabled >100kΩ: Hiccup mode protection is disabled and spread spectrum is enabled
12, 13, 14	SW	O	The drain of the internal power MOSFET switch. Connect the SW pin to the external inductor or transformer.
15	NC		No internal connection
	Thermal Pad		The underneath exposed pad for thermal enhancement. Connect the thermal pad to the ground plane for better thermal performance of the device.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Voltage Range at Terminals (Refer to AGND)	VIN	−0.3	48	V
	EN/UVLO/SYNC	−0.3	VIN+0.2	V
	SS, RT, FB, COMP, MODE, VCC	−0.3	5.5	V
	SW (DC)	−0.3	48	V
	SW (10ns transient, less than 1% duty cycle)	−4	55	V
	PGND	−0.3	0.3	V
	PGOOD	−0.3	18	V
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
V_{HBM}	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
V_{CDM}	Charged Device Model ESD	ANSE/ESDA/JEDEC JS-002 (2)	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{IN}	VIN Input	2.9		45	V
V_{SUPPLY}	Boost Converter Input Voltage	1.5		45	V
V_{OUT}	Boost Converter Output Voltage	V_{SUPPLY}		45	V
V_{UVLO}	UVLO Input	0		45	V
V_{FB}	FB Input	0		5.0	V
f_{SW}	Typical Switching Frequency	100		2200	kHz
f_{SYNC}	Synchronization Pulse Frequency	100		2200	kHz
T_J	Junction Temperature Range	–40		150	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC(top)}$	Unit
QFN3X3-16	50.9	16	39.3	°C/W

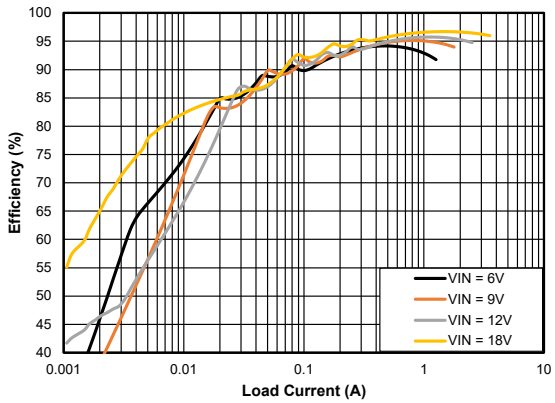
Electrical Characteristics

All test conditions: V_{IN} = 12 V, RT = 9.09 kΩ, T_J = −40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Current						
$I_{SHUTDOWN(VIN)}$	VIN Shutdown Current	V_{IN} = 12 V, V_{UVLO} = 0 V		2.6	5	μA
$I_{OPERATING(VIN)}$	VIN Operating Current	V_{IN} = 12 V, V_{UVLO} = 2.0 V, V_{FB} = V_{REF}, RT = 220 kΩ		570	775	μA
VCC Regulation						
V_{VCC_REG}	VCC Regulation	V_{IN} = 8 V, I_{CC} = 18 mA	4.8	5.0	5.2	V
$V_{CC\_UVLO(RISING)}$	VCC UVLO Threshold	V_{CC} rising	2.7	2.8	2.9	V
$V_{CC\_UVLO\_HYS}$	VCC UVLO Hysteresis	V_{CC} falling		0.1		V
Enable						
V_{EN_R}	Enable Threshold	EN rising	0.6	0.9	1.05	V
V_{EN_F}	Enable Threshold	EN falling	0.46	0.78	0.95	V
V_{EN_HYS}	Enable Hysteresis	EN falling		0.12		V
UVLO/SYNC						
V_{UVLO_R}	UVLO/SYNC Threshold	UVLO rising	1.425	1.5	1.575	V
V_{UVLO_F}	UVLO/SYNC Threshold	UVLO falling	1.37	1.45	1.52	V
V_{UVLO_HYS}	UVLO/SYNC Threshold Hysteresis	UVLO falling		0.05		V
I_{UVLO}	UVLO Hysteresis Current	V_{UVLO} = 1.6 V	4	5	6	μA
Spread Spectrum						
f_{MOD}	Modulation Frequency (upper limit)			8%		f_{SW}
	Modulation Frequency (lower limit)			−7%		f_{SW}
SOFT START						
I_{SS}	Soft-start Current		8.8	10	11.2	μA
R_{SS_PD}	SS Pulldown Switch R_{DSON}			19		Ω
Pulse Width Modulation						
f_{SW}	Switching Frequency	RT = 220 kΩ	85	100	115	kHz
		RT = 49.3 kΩ	388	440	492	kHz
		RT = 9.09 kΩ	1980	2200	2420	kHz
$t_{ON(MIN)}$	Minimum on Time	RT = 9.09 kΩ		80		ns
D_{MAX}	Maximum Duty Cycle Limit	RT = 9.09 kΩ	85%	92%	98%	

Parameter		Conditions	Min	Typ	Max	Unit
		RT = 220 kΩ	90%	94%	98%	
V_{RT}	RT Regulation Voltage			0.5		V
Current Limit						
I_{LIMIT}	Internal MOSFET Current Limit	TPQ5057	6.5	7.5	8.5	A
		TPQ50571	5.3	6.2	7.1	A
Hiccup Mode Protection						
t_{HICCUP_EN}	Hiccup Enable Cycles			64		Cycles
t_{HICCUP_RST}	Hiccup Timer Reset Cycles			8		Cycles
Error Amplifier						
V_{REF}	FB Reference		0.99	1	1.01	V
G_{mEA}	Transconductance			2		mA/V
$I_{SOURCING}$	COMP Sourcing Current	V_{COMP} = 1.2 V	155			μA
V_{CLAMP_H}	High COMP Clamp Voltage	COMP rising (V_{UVLO} = 2.0 V)	1.7	2.3		V
V_{CLAMP_L}	Low COMP Clamp Voltage	COMP falling		0.9	1.0	V
A_{CS}	ΔV_{COMP} / ΔI_{SW}			0.099		V/A
OVP						
V_{OVTH}	Overvoltage Threshold	FB rising (reference to V_{REF})	107%	110%	113%	V_{REF}
V_{OVTL}	Overvoltage Threshold	FB falling (reference to V_{REF})		105%		V_{REF}
PGOOD						
R_{PG_PD}	PGOOD Pulldown Switch R_{DSON}	1-mA sinking		55		Ω
V_{UVTL}	Undervoltage Threshold	FB falling (reference to V_{REF})	87%	90%	93%	V_{REF}
V_{UVTH}	Undervoltage Threshold	FB rising (reference to V_{REF})		95%		V_{REF}
Power Switch						
R_{DSON}	Internal MOSFET on-resistance	V_{IN} = 12 V		39	75	mΩ
		V_{IN} = 3.5 V		41	80	mΩ
I_{LKG}	Leakage Current	V_{SW} = 12 V			3.0	μA
Thermal Protection						
T_{SD}	Thermal Shutdown Protection Threshold	T_J rising		175		ºC
T_{SD_HYS}	Thermal Shutdown Hysteresis	T_J falling below T_{SD}		15		ºC

Typical Performance Characteristics



V_{IN} = 6V, 9V, 12V, 18V, V_{OUT} = 24V, f_{SW} = 400 kHz

Figure 1. Efficiency vs. Load Current

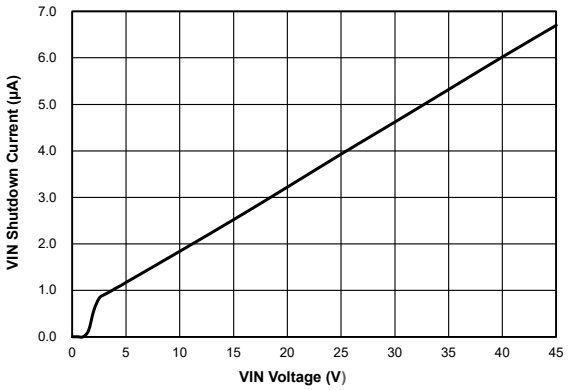


Figure 2. VIN Shutdown Current vs VIN

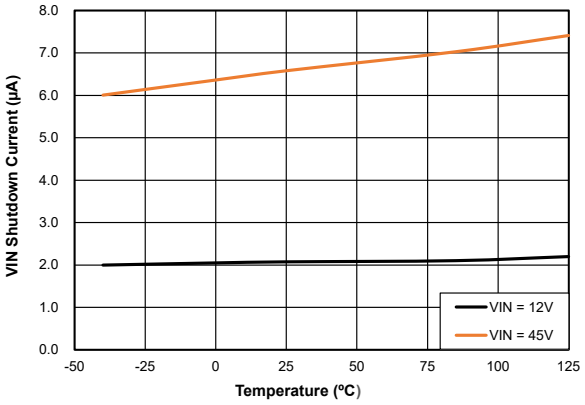


Figure 3. VIN Shutdown Current vs Temperature

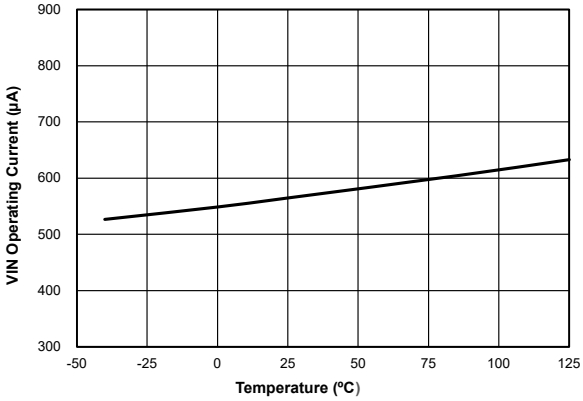


Figure 4. VIN Operating Current vs Temperature

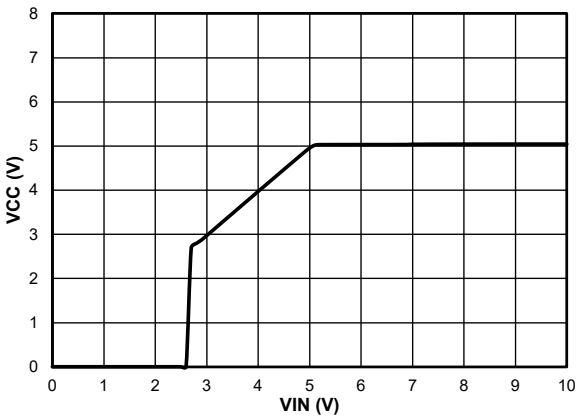


Figure 5. V_{CC} vs V_{IN} (No Load)

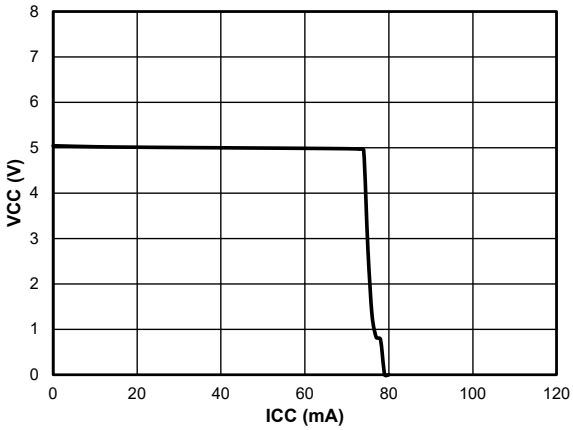


Figure 6. V_{CC} vs I_{CC}

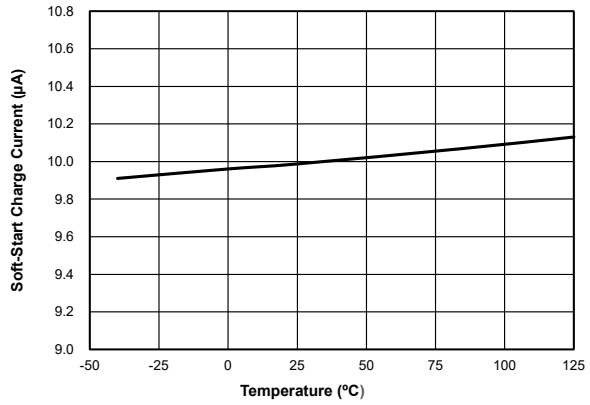


Figure 7. I_{SS} vs Temperature

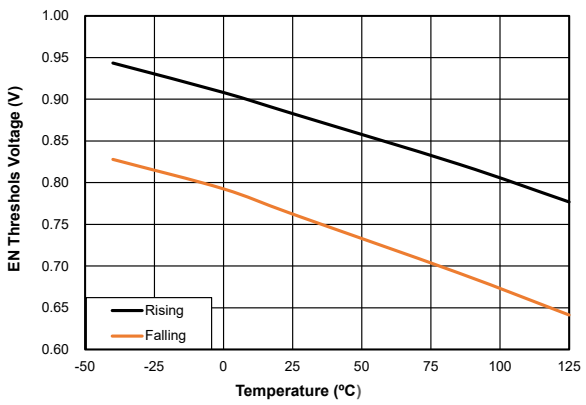


Figure 8. EN Threshold vs Temperature

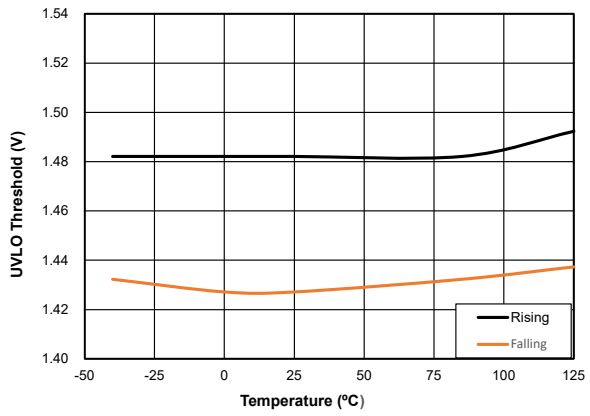


Figure 9. UVLO Threshold vs Temperature

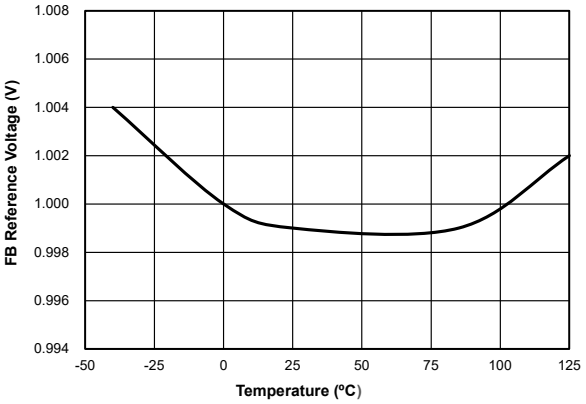


Figure 10. FB Reference vs Temperature

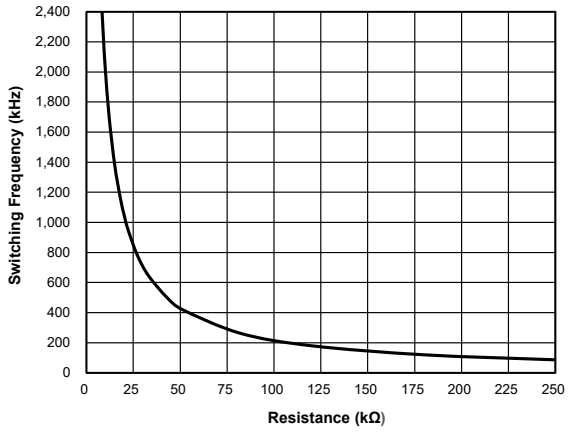


Figure 11. Frequency vs. RT Resistance

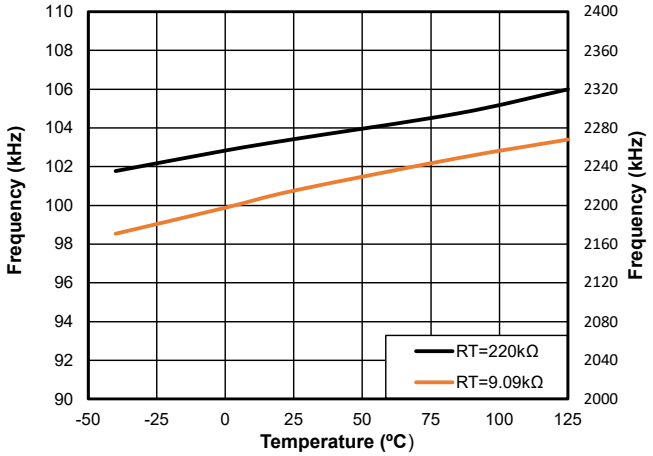


Figure 12. Frequency vs Temperature

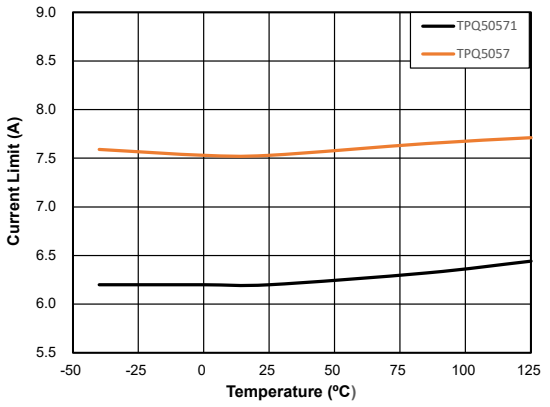
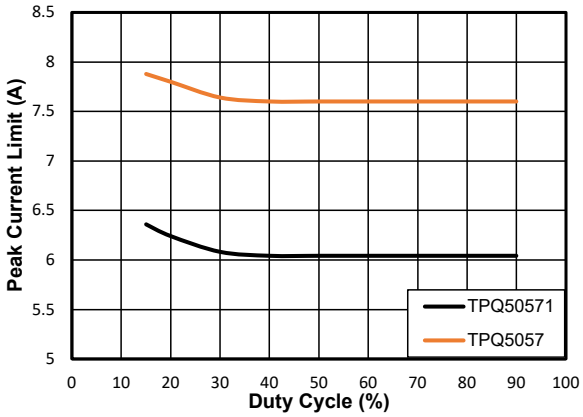


Figure 13. Current Limit Threshold vs Temperature



f_{SW} = 1 MHz, L = 4.7 µH, V_{IN} = 6 V

Figure 14. Peak Current Limit vs Duty Cycle

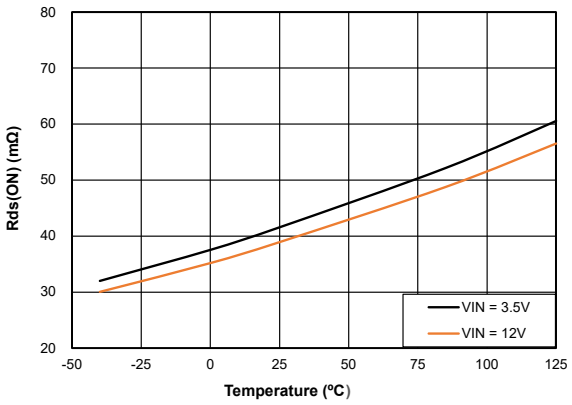


Figure 15. Internal MOSFET R_{DSON} vs Temperature

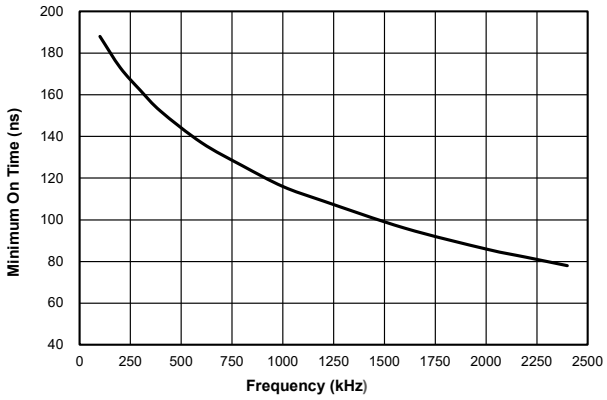


Figure 16. $t_{ON(MIN)}$ vs Frequency

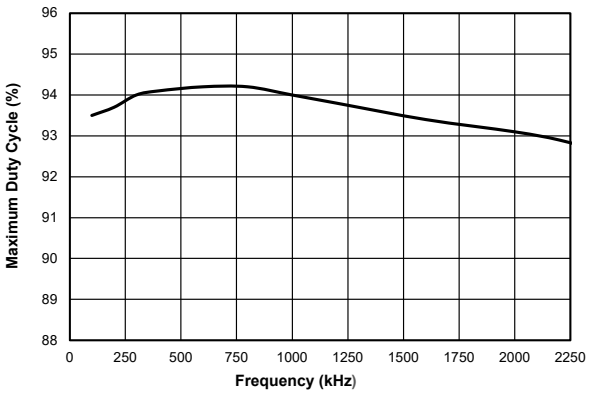


Figure 17. Maximum Duty Cycle vs Frequency

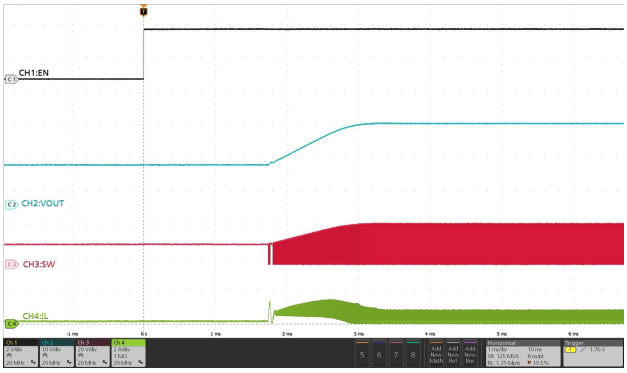


Figure 18. Startup Waveform by EN

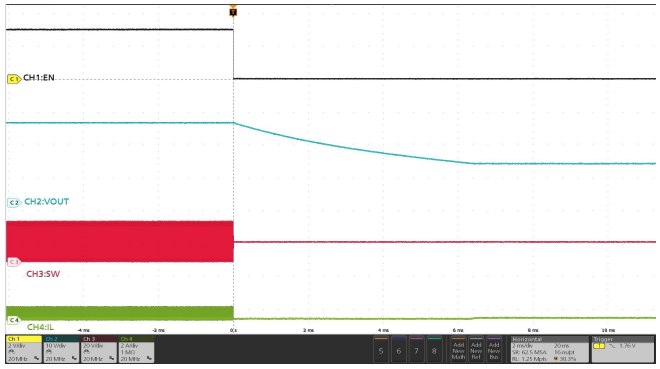


Figure 19. Shutdown Waveform EN

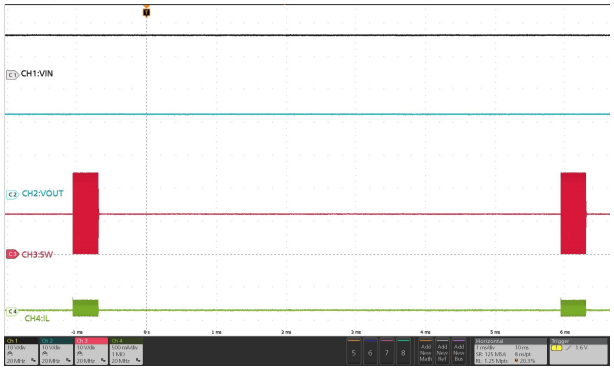


Figure 20. Switching Waveform at 0-A Load Current

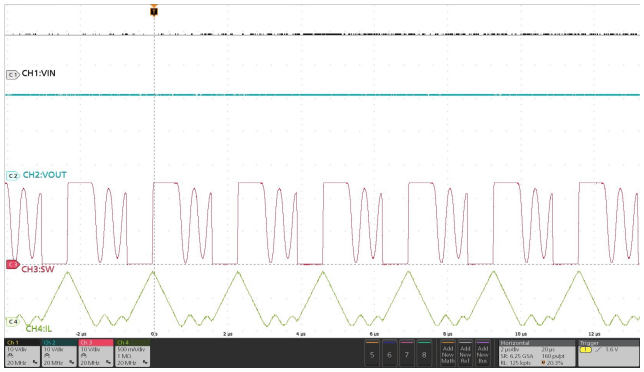


Figure 21. Switching Waveform at 0.1-A Load Current

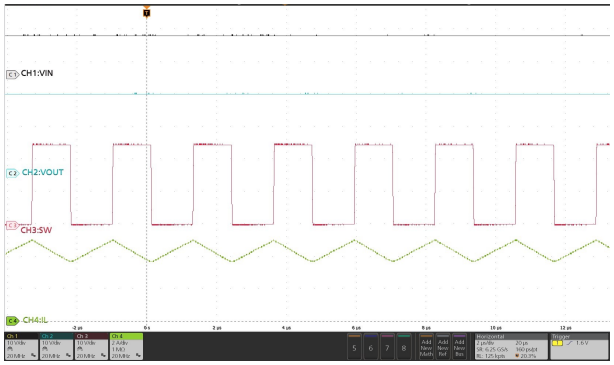


Figure 22. Switching Waveform at 2-A Load Current

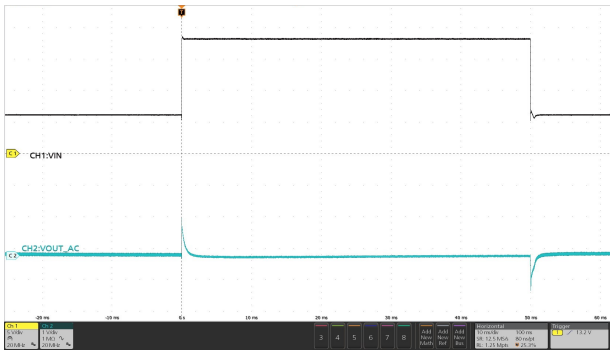


Figure 23. Line Transient

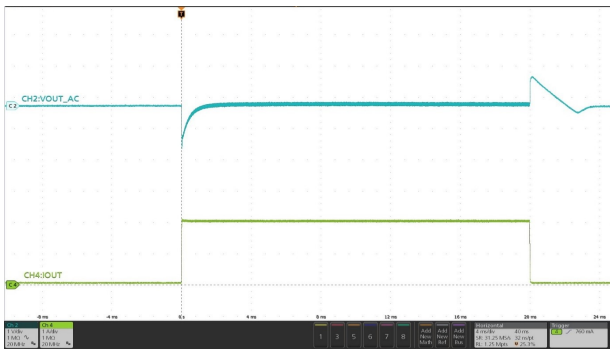


Figure 24. Load Transient

Detailed Description

Overview

The TPQ5057x is a wide input range, non-synchronous switching regulator with an integrated 48-V, 7-A power MOSFET switch. The TPQ5057x uses a peak-current-mode control scheme. The device can be used in boost, SEPIC, and flyback topologies.

The TPQ5057x can operate with the input supply voltage from 2.9 V to 45 V. An internal LDO output of 5 V at the VCC pin to supply the internal circuit. When the VIN pin is supplied with a voltage greater than 2.9 V. The supply voltage for the switching power stage can be down to 1.5 V.

The switching frequency is either set by an external resistor or synchronized to an external clock from 100 kHz to 2.2 MHz. Switching at 2.2 MHz allows for a small solution size and fast transient response.

The TPQ5057x supports the use of an external VCC supply to improve efficiency. Low operating current and pulse-skipping operation improve efficiency at light loads.

The device has built-in protection features such as cycle-by-cycle current limit, overvoltage protection, hiccup mode overload protection, and thermal shutdown. Additional features include low shutdown current, programmable soft start, programmable input UVLO, spread spectrum, and power-good indicator.

Functional Block Diagram

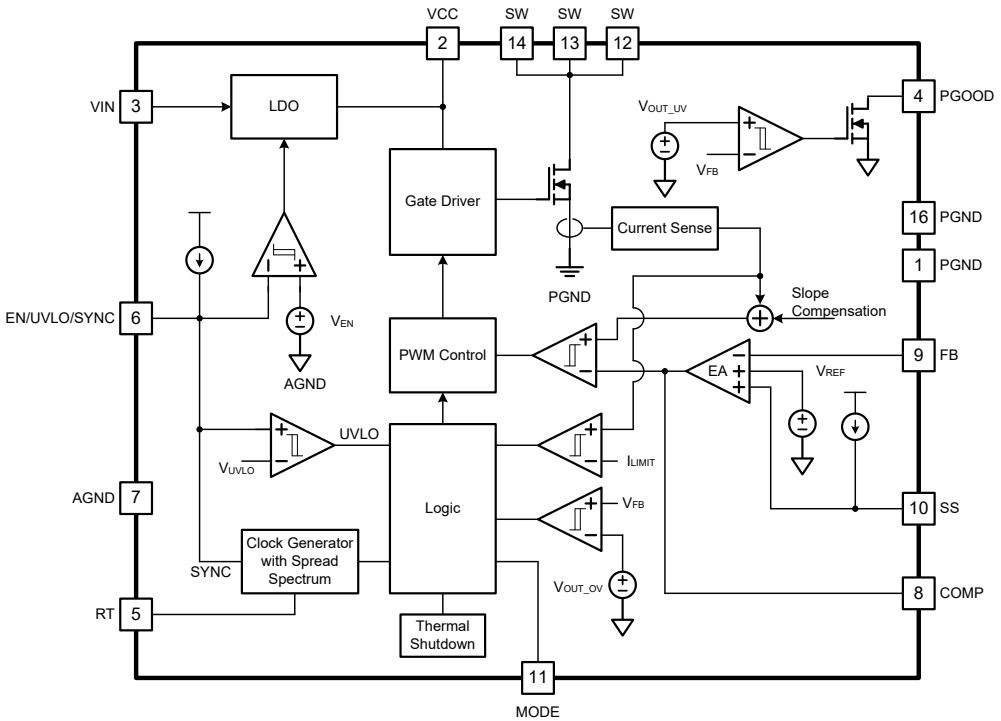


Figure 25. Functional Block Diagram

Feature Description

Enable and Programmable Input Undervoltage Lockout

The TPQ5057x has a dual function enable and input undervoltage lockout (UVLO) circuit. During power-on, when the VIN pin voltage is greater than 2.9 V and the voltage at the EN/UVLO/SYNC pin is in between the enable threshold (V_{EN}) and the UVLO threshold (V_{UVLO}) for more than 1.5μs, the device starts up and an internal configuration starts. The device typically requires 65-μs for internal start-up and then goes into standby mode. In standby mode, the VCC regulator and the RT regulator are active, the SS pin is grounded, and there is no switching at the SW pin.

When the EN/UVLO/SYNC pin voltage continues to go up above the UVLO rising threshold, the device enters run mode. In run mode, a soft-start sequence starts when the VCC voltage is greater than the VCC UVLO threshold ($V_{CC-UVLO}$). The UVLO threshold has 50-mV hysteresis and an additional 5-μA current source is switched on or off at the EN/UVLO/SYNC pin to make a desired hysteresis for input voltage. When the EN/UVLO/SYNC pin voltage exceeds the UVLO rising threshold, the current source is enabled to quickly raise the voltage at the EN/UVLO/SYNC pin. When the EN/UVLO/SYNC pin voltage falls below the UVLO falling threshold, the current source is disabled, causing the voltage at the EN/UVLO/SYNC pin to fall quickly. When the UVLO pin voltage is less than the enable threshold (V_{EN}), the device enters shutdown mode after a 40-μs (typical) delay with all functions disabled.

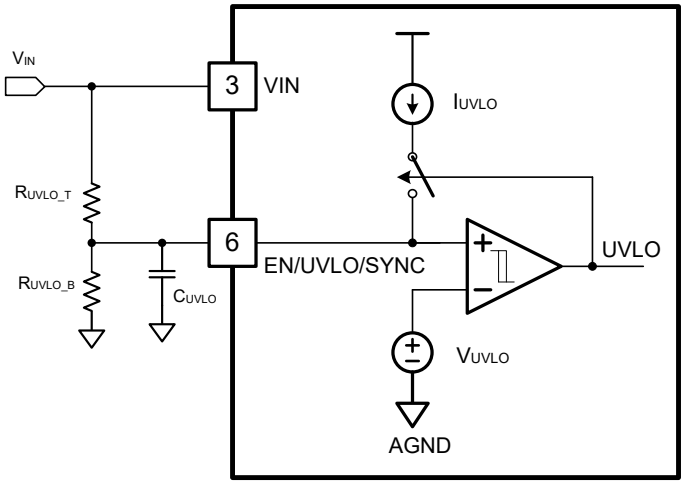


Figure 26. Input UVLO Threshold Setting

The external UVLO resistor divider must be designed so that the voltage at the EN/UVLO/SYNC pin is greater than 1.5 V (typical) when the input voltage is in the desired operating range. The values of two resistors, R_{UVLO_T} and R_{UVLO_B} can be calculated as shown in Equation 1 and Equation 2.

$$R_{UVLO\_T} = \frac{V_{IN\_ON} \times \frac{V_{ULVO\_F}}{V_{ULVO\_R}} - V_{IN\_OFF}}{I_{UVLO}} \quad (1)$$

$$R_{UVLO\_B} = \frac{V_{UVLO\_R} \times R_{UVLO\_T}}{V_{IN\_ON} - V_{UVLO\_R}} \quad (2)$$

Where

- V_{IN_ON} is the desired start-up voltage of the converter.
- V_{IN_OFF} is the desired turnoff voltage of the converter.

A UVLO glitch filtering capacitor (C_{UVLO}) is required in case the input voltage drops below the V_{IN_OFF} momentarily during the start-up or during a severe load transient at the low input voltage. The UVLO filtering capacitor should be less than 1nF to allow the voltage at the UVLO pin to be quickly raised when the 5-μA hysteresis current turns on.

Do not leave the EN/UVLO/SYNC pin floating. Connect it to the VIN pin if not used.

High Voltage VCC Regulator

The device has an internal wide input linear regulator which is sourced from the VIN pin. The VIN pin can be connected directly to supply voltages from 2.9 V to 45 V. The regulator outputs regulated 5-V voltage at the VCC pin with 30-mA output current capability. The recommended capacitor at the VCC pin is from 1 μF to 4.7 μF.

The linear regulator turns on when the device is enabled. When the VIN pin voltage is below the VCC regulation target, the VCC output tracks the VIN pin voltage with a small dropout voltage. When the VIN pin voltage is greater than 5 V, the VCC regulator provides a 5-V supply for the device and the internal N-channel MOSFET driver.

The minimum supply voltage for the power stage after start-up can be further decreased by supplying the VIN pin from the boost converter output or from an external power supply as shown in Figure 27.

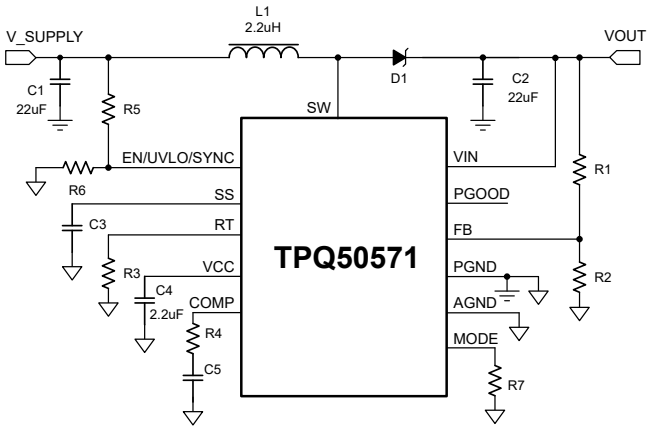


Figure 27. Decreasing the Minimum Operating Voltage after Start-up

In the flyback topology, the internal power dissipation of the device can be decreased by supplying the VCC using an additional transformer winding. In this configuration, the external VCC supply voltage must be greater than the VCC regulation target ($V_{CC\text{-}REG}$), and the VIN pin voltage must be always greater than 2.9 V.

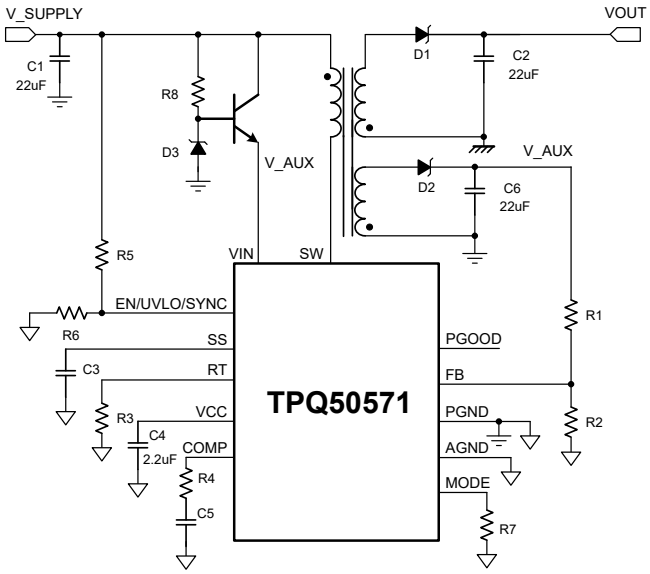


Figure 28. External VIN Supply (PSR Flyback)

Soft Start

When the TPQ5057x is enabled to start up, an internal 10-μA soft-start current source (I_{SS}) turns on after the VCC voltage exceeds the 2.8-V UVLO threshold. The soft-start current gradually increases the voltage on an external soft-start capacitor connected to the SS pin. The TPQ5057x regulates the FB pin voltage to the SS pin voltage when the SS pin voltage is below the internal reference voltage. This results in a gradual rise of the output voltage. When the SS pin voltage reaches the internal reference voltage and above, the FB pin voltage is regulated to the internal reference voltage.

The SS pin is pulled down to GND by an internal switch when the VCC voltage is less than the VCC UVLO threshold or the UVLO pin voltage is less than the UVLO threshold during hiccup mode off-time or thermal shutdown.

In boost topology, the soft-start time (t_{SS}) varies with the input supply voltage. The soft-start time in boost topology is calculated as shown in Equation 3.

$$t_{SS} = \frac{C_{SS}}{I_{SS}} \times \left(1 - \frac{V_{SUPPLY}}{V_{OUT}}\right) \quad (3)$$

In SEPIC topology, the soft-start time (t_{SS}) is calculated as shown in Equation 4.

$$t_{SS} = \frac{C_{SS}}{I_{SS}} \quad (4)$$

It is recommended to choose a soft-start time long enough so that the converter can start up without going into an overcurrent state.

In primary side flyback topology, a PNP transistor can be used by connecting the base to the SS pin and emitter to the COMP pin to achieve soft start. Figure 29 shows the implementation.

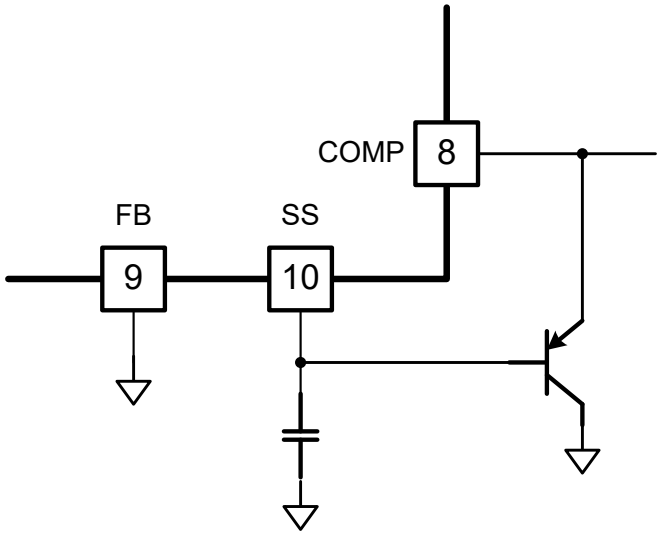


Figure 29. Soft Start Configuration in Primary Side Flyback Topology

In secondary side flyback topology, the soft start is implemented by external RC circuit as shown in Figure 30.

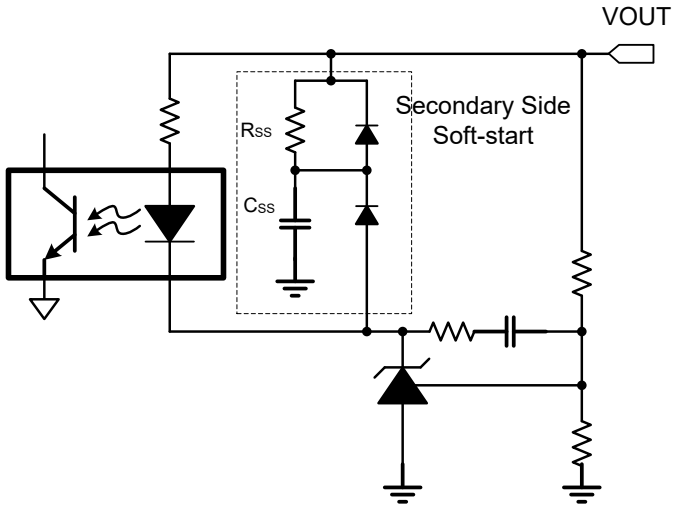


Figure 30. Soft Start Configuration in Secondary Side Flyback Topology

Switching Frequency

The switching frequency is set by an external resistor connected between the RT pin and the AGND pin. The resistor value to set the switching frequency (f_{RT}) is calculated using Equation 5.

$$R_T = \frac{2.21 \times 10^{10}}{f_{RT(TYPICAL)}} - 955 \quad (5)$$

The RT pin is regulated to 0.5 V by the internal regulator when the device is enabled.

Dual Triangle Spread Spectrum

The device provides a digital spread spectrum which reduces the EMI of the power supply over a wide frequency range. This function is enabled by a single resistor (37.4 kΩ or >100 kΩ) connected between the MODE pin and the AGND pin or by programming the MODE pin voltage (370 mV or greater than 1.0 V) during initial power up. When the spread spectrum is enabled, the internal modulator dithers the internal clock. When an external synchronization clock is applied to the EN/UVLO/SYNC pin, the internal spread spectrum is disabled. The dual Triangle spread spectrum combines a low-frequency triangular modulation profile with a high-frequency triangular modulation profile. The low-frequency triangular modulation improves performance in lower radio frequency bands (for example, AM band), while the high-frequency triangular modulation improves performance in higher radio frequency bands (for example, FM band). In addition, the frequency of the triangular modulation is further modulated to reduce the likelihood of any audible tones. In order to minimize output voltage ripple caused by the spread spectrum, the duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled (see Figure 31.)

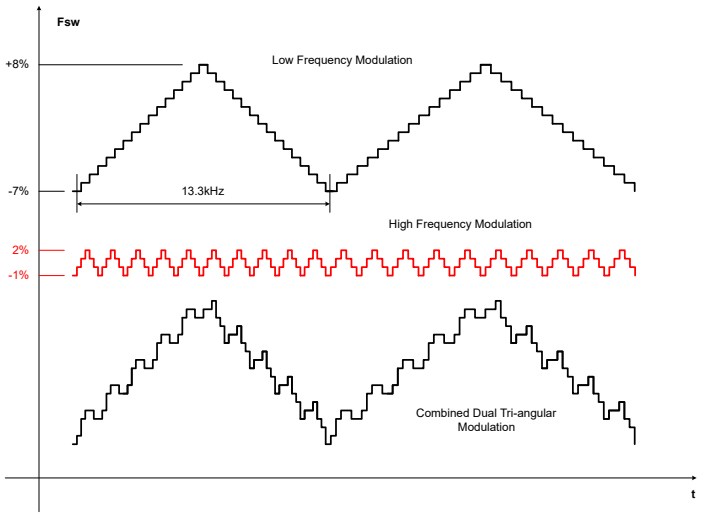


Figure 31. Dual Tri-angular Switching Frequency Dithering

Clock Synchronization

The switching frequency of the device can be synchronized to an external clock by feeding the clock into the EN/UVLO/SYNC pin. The internal clock of the device is synchronized at the falling edge but ignores the falling edge input during the forced off-time which is determined by the maximum duty cycle limit. The external synchronization clock must pull down the EN/UVLO/SYNC pin voltage below 1.45 V (typical). The duty cycle of the pulldown pulse is not limited, but the minimum pulldown pulse width must be greater than 150 ns, and the minimum pull-up pulse width must be greater than 250 ns.

When the input UVLO is not required, the external synchronization clock can connect to the EN/UVLO/SYNC pin directly. In this configuration, it is recommended to apply the external clock pulses after the VIN is supplied. By limiting the current flowing into the EN/UVLO/SYNC pin below 1 mA using a current-limiting resistor, the external clock pulses can be supplied before the VIN is supplied.

When the input UVLO is also required with an external resistor divider connected, Figure 32 shows an implementation of the enable function and the external clock synchronization together with the programmable UVLO function. The EN/UVLO/SYNC pin is pulled down by a discrete MOSFET or an open-drain output of an MCU. In this configuration, the device stops switching immediately after the EN/UVLO/SYNC pin is grounded, and the device shuts down in 35 µs (typical) after the EN/UVLO/SYNC pin is grounded.

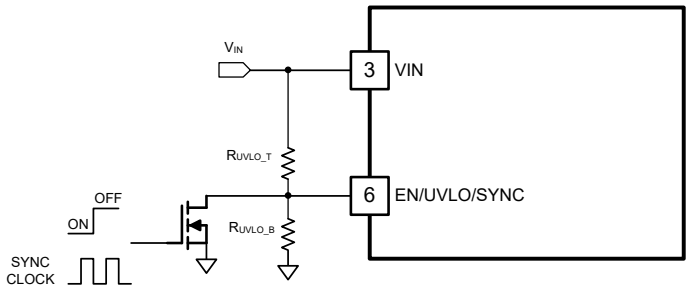


Figure 32. Enable and External Clock Synchronization with Input UVLO Function

The external clock frequency (f_{SYNC}) must be within +25% and –30% of the setting switching frequency $f_{RT(TYPICAL)}$. Because the maximum duty cycle limit and the peak current limit are affected by the clock synchronization, take extra care when using the clock synchronization function.

Current Sense and Slope Compensation

The device senses switch current which flows into the SW pin, and provides a fixed internal slope compensation ramp, helping to prevent subharmonic oscillation at the high-duty cycle. The internal slope compensation ramp is added to the sensed inductor current input for the PWM operation, but no slope compensation ramp is added to the current limit for an accurate peak current limit operation over the input supply voltage.

According to peak current mode control theory, the slope of the compensation ramp must be greater than half of the sensed inductor current falling slope to prevent subharmonic oscillation at the high-duty cycle. Therefore, the minimum amount of slope compensation in boost topology should satisfy the following inequality:

$$0.5 \times \frac{(V_{OUT} + V_D) - V_{SUPPLY}}{L} \times A_{CS} \times \text{Margin} < V_{SLOPE} \times f_{SW} \quad (6)$$

where

- V_D is the forward voltage drop of D1, the external diode.
- V_{SUPPLY} is the input voltage to the inductor of the power stage
- V_{SLOPE} is the peak slope voltage. For TPQ5057, V_{SLOPE} is 750 mV. For TPQ50571, V_{SLOPE} is 620 mV
- f_{SW} is the switching frequency
- A_{CS} is the gain of the current sense

Typically, 82% of the sensed inductor current falling slope is known as an optimal amount of slope compensation. By increasing the margin to 1.6, the amount of slope compensation becomes close to the optimal amount.

If clock synchronization is not used, the switching frequency f_{SW} equals the f_{RT} frequency. If clock synchronization is used, the f_{SW} equals the f_{SYNC} frequency.

Current Limit and Minimum On-time

The device provides cycle-by-cycle peak current limit protection that turns off the MOSFET when the inductor current reaches the current limit threshold (I_{LIMIT}). To avoid an unexpected hiccup mode operation during a harsh load transient condition, it is recommended to have more margin when considering the maximum load current.

Boost converters have a natural pass-through path from the supply to the load through the high-side power diode (D1). Because of this path and the minimum on-time limitation of the device, boost converters cannot provide current limit protection when the output voltage is close to or less than the input supply voltage. The minimum on-time is calculated as Equation 7.

$$t_{ON(MIN)} \approx \frac{1}{\frac{65}{R_T} + 5.4 \times 10^{-3}} \text{ (ns)} \quad (7)$$

Feedback and Error Amplifier

The feedback resistor divider is connected to an internal transconductance error amplifier which features high output resistance and wide bandwidth. The internal transconductance error amplifier sources current which is proportional to the difference between the FB pin and the SS pin voltage or the internal reference, whichever is lower. The internal transconductance error amplifier provides symmetrical sourcing and sinking capability during normal operation and reduces its sinking capability when the FB is greater than the OVP threshold.

To set the output regulation target, select the feedback resistor values as shown in Equation 8.

$$V_{OUT} = V_{REF} \times \left(\frac{R_{FB\_T}}{R_{FB\_B}} + 1 \right) \quad (8)$$

The output of the error amplifier is connected to the COMP pin, allowing the use of a Type 2 loop compensation network. R_C, C_C, and optional C_H loop compensation components configure the error amplifier gain and phase characteristics to achieve a stable loop response. The absolute maximum voltage rating of the FB pin is 5.5 V. If necessary, the feedback resistor divider input can be clamped with an external zener diode.

The COMP pin features internal clamps. The maximum COMP clamp limits the maximum COMP pin voltage below its absolute maximum rating even in shutdown. The minimum COMP clamp limits the minimum COMP pin voltage in order to start switching as soon as possible during no load to heavy load transition. The minimum COMP clamp is disabled when the FB pin is connected to GND in the flyback topology.

Power Good Indicator

The device has a power-good indicator (PGOOD) to simplify sequencing and supervision. The PGOOD switches to a high impedance open-drain state when the FB pin voltage is greater than the feedback undervoltage threshold (V_{UVTH}), the VCC is greater than the VCC UVLO threshold and the EV/UVLO/SYNC voltage is greater than the EN threshold. A 25-µs deglitch filter prevents any false pulldown of the PGOOD due to transients. The recommended minimum pullup resistor value is 10 kΩ.

Due to the internal diode path from the PGOOD pin to the VIN pin, the PGOOD pin voltage cannot be above the VIN voltage of more than 0.3 V.

Hiccup Mode Overload Protection

To further protect the converter during prolonged current limit conditions, the device provides an optional hiccup mode overload protection. This function is enabled by a single resistor (37.4 kΩ or 62.0 kΩ) between the MODE pin and the AGND pin or by programming the MODE pin voltage (370 mV or 620 mV) during initial power up. The internal hiccup mode fault timer counts the PWM clock cycles when the cycle-by-cycle current limiting occurs. When the hiccup mode fault timer detects 64 cycles of current limiting, an internal hiccup mode off timer forces the device to stop switching and pulls down SS. Then, the device will restart after 32768 cycles of hiccup mode off-time. The 64-cycle hiccup mode fault timer is reset if eight consecutive switching cycles occur without exceeding the current limit threshold. The soft-start time must be long enough not to trigger the hiccup mode protection during soft-start time because the hiccup mode fault timer is enabled during the soft start.

Maximum Duty Cycle Limit and Minimum Input Supply Voltage

When designing boost converters, the maximum duty cycle happens at the minimum supply voltage. The minimum input supply voltage that can achieve the target output voltage is limited by the maximum duty cycle limit, and it can be estimated as follows.

$$V_{SUPPLY(MIN)} \approx (V_{LOAD} + V_F) \times (1 - D_{MAX}) + I_{SUPPLY(MAX)} \times (R_{DCR} + 110m \times D_{MAX}) \quad (9)$$

where

- $I_{SUPPLY(MAX)}$ is the maximum input current.
- R_{DCR} is the DC resistance of the inductor.
- D_{MAX} can be estimated in Figure 17 at different switching frequencies.

Internal Power MOSFET

The device provides an internal switch with an $R_{DS(ON)}$ that is typically 39 mΩ when the VIN pin is greater than 5 V. The $R_{DS(ON)}$ of the internal switch is increased when the VIN pin is less than 5 V. The device temperature must be checked at the minimum supply voltage especially when the VIN pin is less than 5 V.

The dV/dt of the SW pin must be limited during the 90-µs internal start-up delay to avoid a false turn-on, which is caused by the coupling through C_{GD} parasitic capacitance of the internal MOSFET switch.

Overvoltage Protection

The device has overvoltage protection (OVP) for the output voltage. OVP is sensed at the FB pin. If the voltage at the FB pin rises above the overvoltage threshold (V_{OVTH}), OVP is triggered, and switching stops. During OVP, the internal error amplifier is operational, but the maximum source and sink capability is decreased to 60 µA.

Thermal Shutdown

An internal thermal shutdown turns off the VCC regulator, disables switching, and pulls down the SS when the junction temperature exceeds the thermal shutdown threshold (T_{SD}). After the temperature is decreased by 15°C, the VCC regulator is enabled again, and the device performs a soft start.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPQ5057x is a wide-input-range, non-synchronous switching regulator with an integrated 48-V, 7-A power MOSFET switch. The TPQ5057x uses a peak-current-mode control scheme. The device can be used in boost, SEPIC, and flyback topologies.

Typical Application

Figure 33 shows a typical circuit of a boost converter.

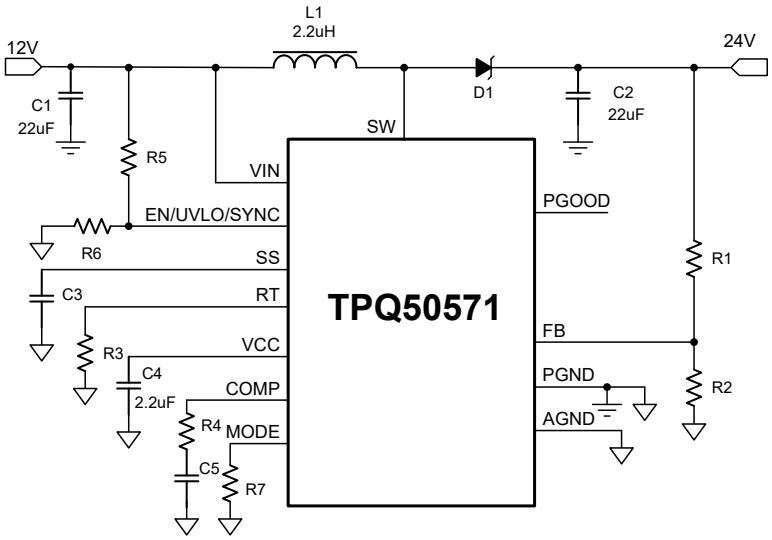


Figure 33. TPQ50571 12-V to 24-V Boost Converter Application Circuit

Selecting the Switching Frequency

Connect a resistor between the RT pin and the AGND pin to set the switching frequency. The resistance can be calculated by Equation 5.

Setting Output Voltage

The output voltage is set by an external resistor divider with the center tap connecting to the FB pin. Typically, a minimum current of 10 μA flowing through the feedback divider gives good accuracy and noise covering. A resistor of less than 100 kΩ is typically selected for low-side resistor R2.

When the output voltage is regulated, the typical voltage at the FB pin is V_{REF}. Thus, the value of R1 is calculated as:

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \quad (10)$$

Switching Duty Cycle

The duty cycle of the converter in continuous conduction mode (CCM) is related primarily to the input and output voltages as computed by Equation 11.

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D} \quad (11)$$

Where,

V_D is the forward voltage drop of the Schottky diode

At light load, the converter operates in discontinuous conduction mode (DCM). In this case, the duty cycle is a function of the load, input and output voltages, inductance, and switching frequency as computer by Equation 12.

$$D = \frac{\sqrt{2 \times (V_{OUT} + V_D - V_{IN}) \times L \times I_{OUT} \times f_{SW}}}{V_{IN}} \quad (12)$$

Selecting the Inductor

The selection of the inductor affects steady-state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications: inductor value, DC resistance, and saturation current. Considering inductor value alone is not enough. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, the effective inductance can fall to a fraction of the zero current value.

The following Equation 13, Equation 14, and Equation 15 calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, it is recommended to use the minimum switching frequency, the inductor value with -20% tolerance, and a low-power conversion efficiency for the calculation.

In a boost regulator, calculate the inductor DC current as in Equation 13.

$$I_{DC} = \frac{(V_{OUT} + V_D) \times I_{OUT}}{V_{IN} \times \eta} \quad (13)$$

Where,

V_D is the forward voltage drop of the Schottky diode

η is the power conversion efficiency

Calculate the inductor current peak-to-peak ripple as in Equation 14.

$$I_{LPP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} + V_D - V_{IN}} + \frac{1}{V_{IN}}\right) \times f_{SW}} \quad (14)$$

Therefore, the peak current of the inductor can be calculated by Equation 15.

$$I_{LPEAK} = I_{DC} + \frac{I_{LPP}}{2} \quad (15)$$

The calculated peak current of the inductor must be less than the current limit of the TPQ50571. Select an inductor with a saturation current higher than the calculated peak current.

Maximum Output Current

The overcurrent limit of the TPQ50571 limits the maximum input current and thus the maximum input power for a given input voltage. The maximum output power is less than the maximum input power due to power conversion losses. Because of the TPQ50571's peak current limit, the maximum output current can be calculated by Equation 16.

A smaller inductor can increase the high current ripple thus reducing the maximum output current.

$$I_{OUT(MAX)} = \frac{\left(I_{LIMIT} - \frac{I_{LPP}}{2}\right) \times V_{IN(MIN)} \times \eta}{V_{OUT}} \quad (16)$$

Where,

I_{LIMIT} is the switch current limit of the TPQ50571

Selecting the Output Capacitors

At least 4.7-μF capacitance of ceramic X7R capacitor is recommended at the output. The output capacitance is mainly selected to meet the requirements for the output ripple and voltage change during a load transient. Then the loop is compensated for the output capacitor selected. The output capacitance should be chosen based on the most stringent of these criteria. The output ripple voltage is related to the capacitance and equivalent series resistance (ESR) of the output capacitor. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given output ripple voltage can be calculated by Equation 17. If high ESR capacitors are used, it will contribute additional ripple. The maximum ESR for a specified ripple is calculated with Equation 18. ESR ripple can be neglected for ceramic capacitors but must be considered if electrolytic capacitors are used. The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated by Equation 19.

$$C_{OUT} \geq \frac{D_{MAX} \times I_{OUT}}{V_{RIPPLE} \times f_{SW}} \quad (17)$$

$$R_{ESR} \leq \frac{\left(V_{RIPPLE} - \frac{D_{MAX} \times I_{OUT}}{f_{SW} \times C_{OUT}}\right)}{\Delta I_L} \quad (18)$$

$$C_{OUT} \geq \frac{\Delta I_{TRAN}}{2\pi \times f_C \times \Delta V_{TRAN}} \quad (19)$$

Where,

V_{RIPPLE} is the output ripple voltage

f_C is the crossover frequency of the open loop of the converter

ΔI_{TRAN} is the output current change during load transient

ΔV_{TRAN} is the output voltage change during load transient

Selecting the Input Capacitors

At least 4.7-μF capacitance of ceramic input capacitor is recommended. Additional input capacitance may be required to meet ripple and/or transient requirements. High-quality ceramic, type X7R is recommended to minimize capacitance variations over temperature.

Selecting the Schottky Diode

The high switching frequency of the TPQ50571 demands high-speed rectification for optimum efficiency. Ensure that the average and peak current ratings of the Schottky diode exceed the average output current. In addition, the reverse breakdown voltage of the diode must exceed the regulated output voltage. The diode must also be rated for the power dissipated which can be calculated with Equation 20.

$$P_D = V_D \times I_{OUT} \quad (20)$$

Control Loop Compensation for Stability

The TPQ50571 requires external compensation which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external compensation network composed of resistors and capacitors is connected to the COMP pin to provide poles and a zero as shown in Figure 34. These poles and zero, along with the inherent pole and zero of a boost converter, determine the closed-loop frequency response.

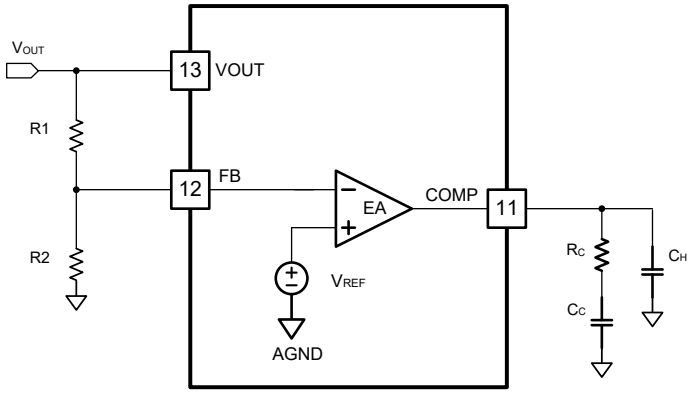


Figure 34. Type II Compensation Network

In CCM mode, approximately, the small signal frequency response of the power stage of the peak current mode boost converter can be modeled by Equation 21.

$$G_{PS}(S) = \frac{R_O \times (1 - D)}{2 \times A_{CS}} \times \frac{\left(1 + \frac{S}{2\pi \times f_{ESRZ}}\right) \times \left(1 - \frac{S}{2\pi \times f_{RHPZ}}\right)}{1 + \frac{S}{2\pi \times f_P}} \quad (21)$$

Where,

D is the switching duty cycle

R_O is the load resistance at the output of the boost converter

A_{CS} is the gain of the current sense of the power stage

f_P is the pole's frequency

f_{ESRZ} is the zero's frequency

f_{RHPZ} is the right-half-plane-zero frequency

The f_P, f_{ESRZ}, and f_{RHPZ} can be calculated by the following equations.

$$f_P = \frac{2}{2\pi \times R_O \times C_{OUT}} \quad (22)$$

Where

C_{OUT} is the effective capacitance of the output capacitor

$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (23)$$

Where

R_{ESR} is the equivalent series resistance of the output capacitor

$$f_{RHPZ} = \frac{R_O \times (1 - D)^2}{2\pi \times L} \quad (24)$$

The COMP pin is the output of the internal transconductance amplifier. Equation 25 shows the small signal transfer function of the compensation network

$$G_C(S) = \frac{G_{mEA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{S}{2\pi \times f_{COMZ}}\right)}{\left(1 + \frac{S}{2\pi \times f_{COMP1}}\right) \times \left(1 + \frac{S}{2\pi \times f_{COMP2}}\right)} \quad (25)$$

Where

Gm_{EA} is the transconductance of the internal error amplifier

R_{EA} is the output resistance of the internal error amplifier, which is about 10 MΩ

V_{REF} is the reference voltage at the FB pin

V_{OUT} is the output voltage

f_{COMP1} and f_{COMP2} are the poles' frequency of the compensation network

f_{COMZ} is the zero's frequency of the compensation network

The next step is to choose the loop crossover frequency, f_C. The higher in frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the crossover frequency is no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}.

At the crossover frequency, the open loop gain is 0 dB. Thus, the value of the R_C can be calculated by Equation 26. Then set the values of C_C and C_H by Equation 27, and Equation 28.

$$R_C = \frac{2\pi \times V_{OUT} \times f_C \times C_{OUT} \times A_{CS}}{(1 - D) \times V_{REF} \times G_{mEA}} \quad (26)$$

$$C_C = \frac{R_O \times C_{OUT}}{2 \times R_C} \quad (27)$$

$$C_H = \frac{R_{ESR} \times C_{OUT}}{R_C} \quad (28)$$

If the calculated C_H is less than 10pF, it can be left open.

Designing the open loop frequency response with greater the 45º phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

Application Examples

SEPIC

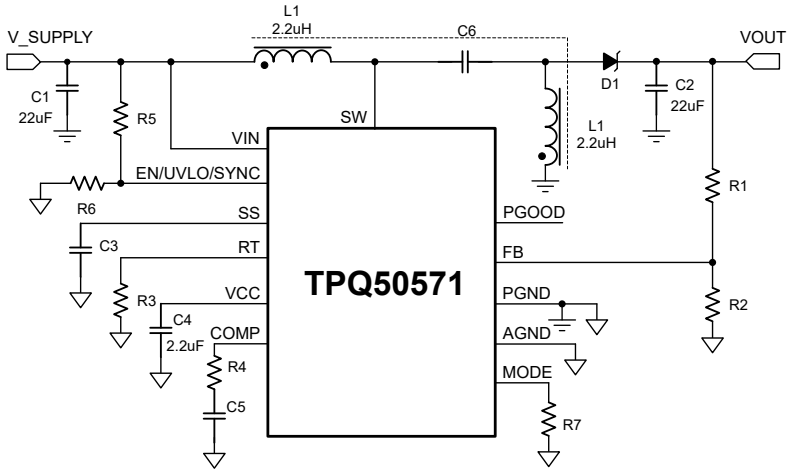


Figure 35. Typical SEPIC Converter

Cuk Converter

The TPQ5057x can be configured as a Cuk converter to output negative voltage. An operational amplifier is needed to invert the negative feedback voltage into the FB pin for output voltage regulation.

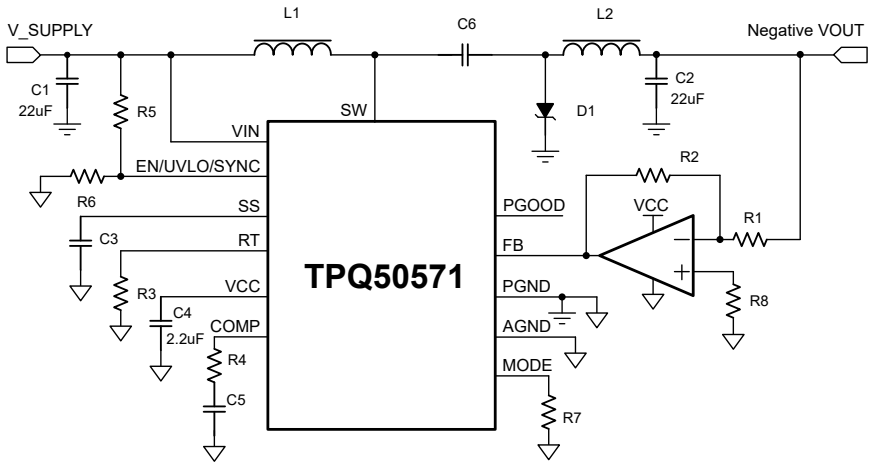


Figure 36. Typical Cuk Converter for Negative Output

Flyback Converter

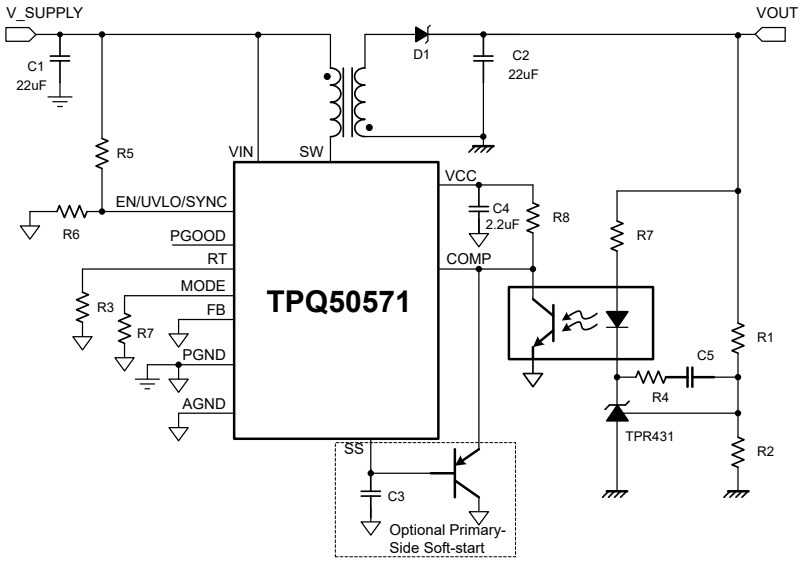


Figure 37. Secondary-Side Regulated Isolated Flyback

Layout

Layout Guideline

The performance of switching converters heavily depends on the quality of the PCB layout. The following guidelines help users design a PCB with the best power conversion performance, and thermal performance, and minimize the generation of unwanted EMI.

- Make the switching loop (C_{OUT} to D1 to SW to PGND to C_{OUT}) as small as possible.
- Use a small size ceramic capacitor for C_{OUT}.
- Leave a copper area near the D1 diode for thermal dissipation.
- Connect the AGND pin directly to the analog ground plane. Connect the AGND pin to the R_{MODE}, R_{UVLO_B}, R_T, C_{SS}, and R_{FB_B} components.
- Connect the exposed pad to the AGND pin under the device.
- Add several vias under the exposed pad to help conduct heat away from the device. Connect the vias to a large ground plane on the bottom layer.

Layout Example

Figure 38 shows the location of external components as they appear on the PCB.

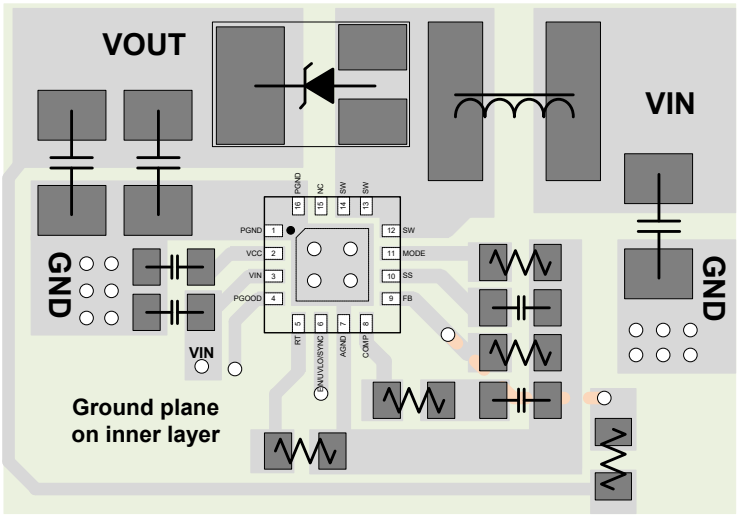
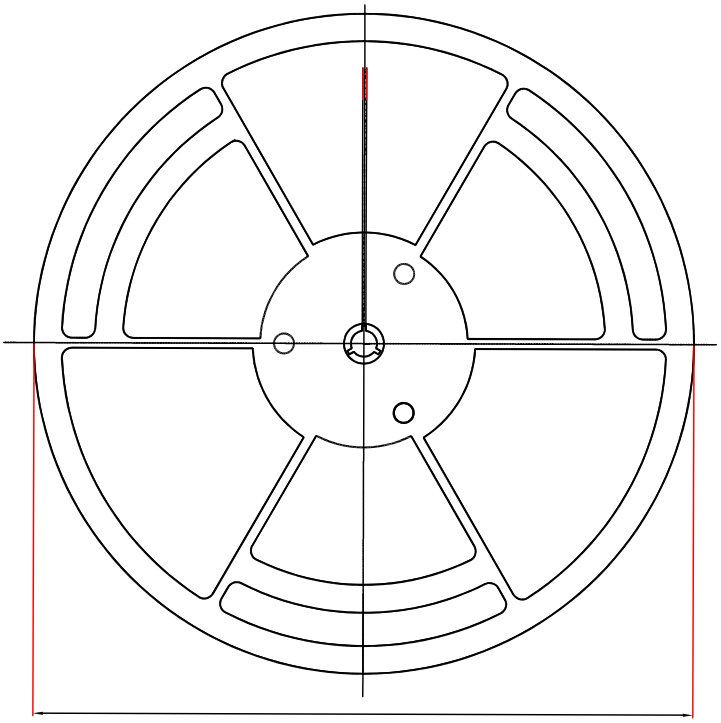
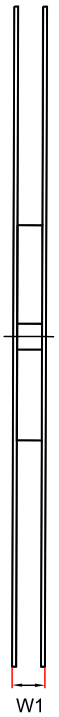
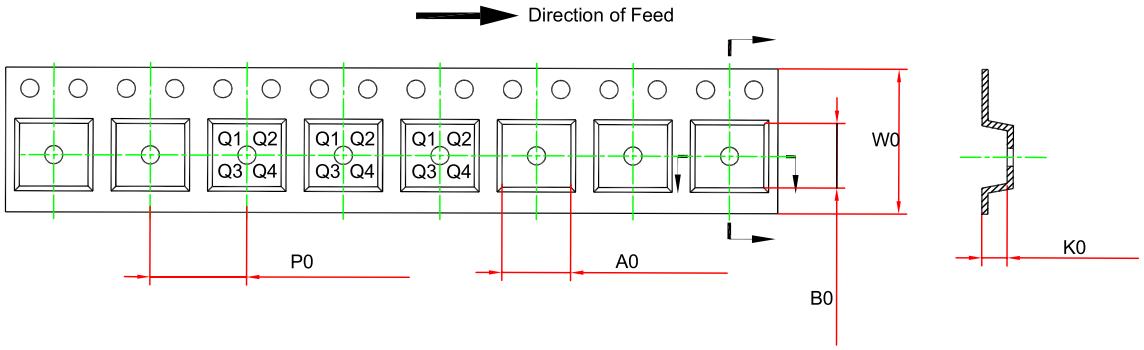


Figure 38. TPQ5057x PCB Layout Example

Tape and Reel Information





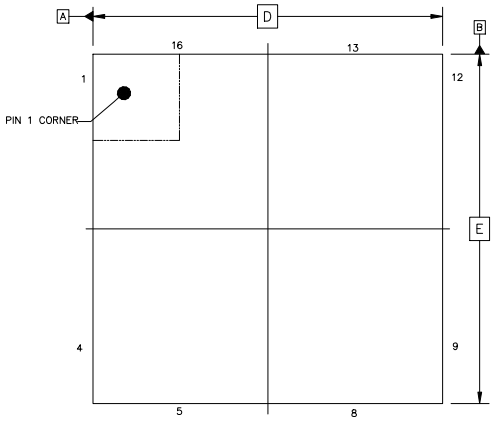


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPQ5057-QFNR-S	QFN3x3-16	330	17.6	3.3	3.3	1.1	8	12	Q2
TPQ50571-QFNR-S	QFN3x3-16	330	17.6	3.3	3.3	1.1	8	12	Q2

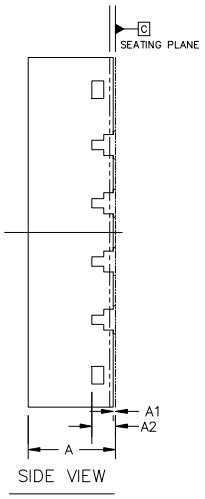
Package Outline Dimensions

QFN3X3-16

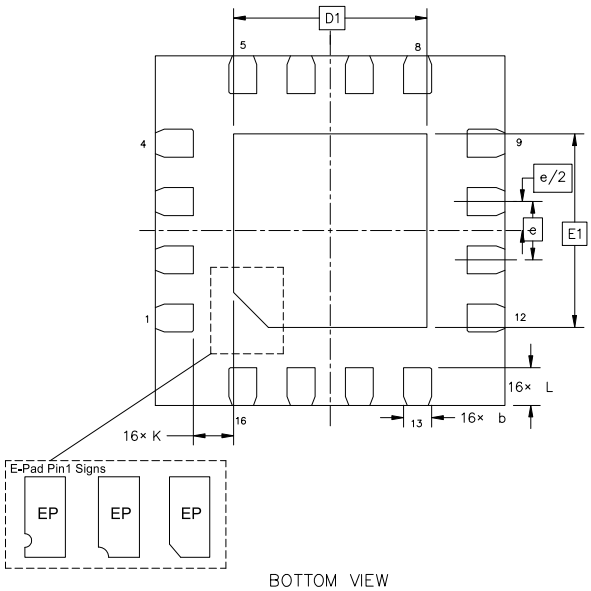
Package Outline Dimensions QFN(QFN3X3-16-D)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
b	0.180	0.300	0.007	0.012
D	3.000 BSC		0.118 BSC	
D1	1.560	1.760	0.061	0.069
e	0.500 BSC		0.020 BSC	
E	3.000 BSC		0.118 BSC	
E1	1.560	1.760	0.061	0.069
L	0.300	0.500	0.012	0.020
k	0.345 BSC		0.064 BSC	

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPQ5057-QFNR-S (1)	−40ºC – 125ºC	QFN3X3-16	Q057	MSL2	Tape & Reel, 4000	Green
TPQ50571-QFNR-S	−40ºC – 125ºC	QFN3X3-16	Q0571	MSL2	Tape & Reel, 4000	Green

(1) For future products, contact the 3PEAK factory for more information and samples

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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