2.2-MHz Wide Input Nonsynchronous Boost, SEPIC, Flyback Controller

Features

- 3.5-V to 45-V Operating Range
- 3.0 V to 20 V when BIAS = VCC
- Low Shutdown Current (typical 2.1 μA)
- Low Operating Current (typical 540 μA)
- Programmable Switching Frequency Range from 100 kHz to 2.2 MHz
- 100-mV Low Current Limit Threshold
- Strong 1.5-A peak Standard MOSFET Driver
- Optional External Clock Synchronization
- ±1% Reference Voltage Accuracy
- Power Good Indicator
- Optional Hiccup Short-Circuit Protection
- Optional Spread-Spectrum to Reduce EMI
- Programmable Input Voltage UVLO
- Adjustable Soft Start Time
- Available in DFN3x2-12 Package

Applications

- Multiple-output Flyback without Optocoupler
- LED Lighting Supply
- Portable Speaker
- General Boost, SEPIC, Flyback Applications

Description

The TPQ5055x (TPQ5055, TPQ50551, TPQ50552, or TPQ50553) is a wide input range, non-synchronous boost controller that uses peak current mode control. The device can be used in boost, SEPIC, and flyback topologies.

The TPQ5055x can start up from a minimum voltage of 3.0 V if the BIAS pin is connected to the VCC pin. It can operate with the input supply voltage as low as 1.5 V if the BIAS pin exceeds 3.5 V.

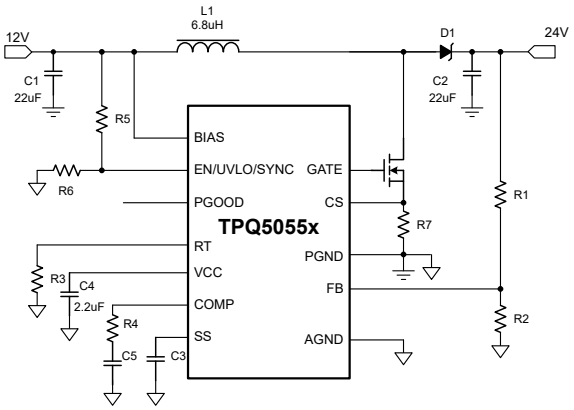
The internal VCC regulator also supports the BIAS pin voltage up to 45 V. The switching frequency is programmable with an external resistor from 100 kHz to 2.2 MHz. Switching at 2.2 MHz minimizes allows for a small solution size and fast transient response.

The TPQ5055x features 1.5-A driver capability and a low 100-mV current limit threshold. The device also supports the use of an external VCC supply to improve efficiency. Low operating current and pulse-skipping operation improve efficiency at light loads.

The TPQ5055x has built-in protection features such as cycle-by-cycle current limit, overvoltage protection, input UVLO, and thermal shutdown. Hiccup mode overload protection is available in the TPQ50551 and the TPQ50553. The spread spectrum switching frequency dithering is available in the TPQ50552 and TPQ50553.

The TPQ5055x is available in a small size 3mm x 2mm DFN package.

Typical Application Circuit



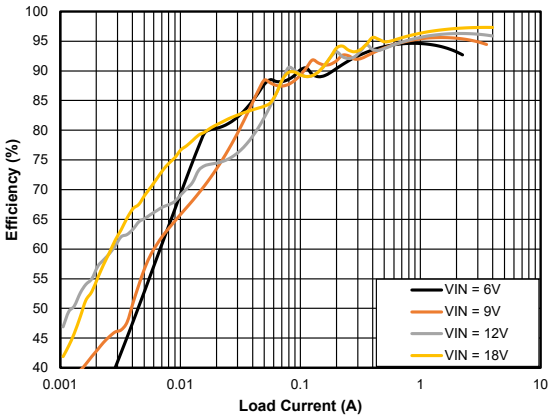


Table of Contents

Product Family Table

Part Number	Hiccup Mode Protection	Spread Spectrum
TPQ5055	Disabled	Disabled
TPQ50551	Enabled	Disabled
TPQ50552 (1)	Disabled	Enabled
TPQ50553 (1)	Enabled	Enabled

(1) For future products, contact the 3PEAK factory for more information and samples.

Revision History

Date	Revision	Notes
2025-02-24	Rev.A.0	Initial release

Pin Configuration and Functions

TPQ5055x

DFN3x2-12

Top View

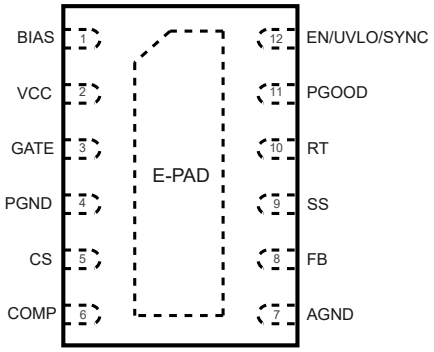


Table 1. Pin Functions: TPQ5055

Pin No.	Pin Name	I/O	Description
1	BIAS	P	Supply voltage input to the VCC regulator. Connect a bypass capacitor from this pin to PGND.
2	VCC	P	Output of the internal VCC regulator and supply voltage input of the MOSFET driver. Connect a ceramic bypass capacitor from this pin to PGND.
3	GATE	O	N-channel MOSFET gate drive output. Connect directly to the gate of the N-channel MOSFET through a short, low inductance path.
4	PGND	GND	Power ground pin. Connect directly to the ground connection of the sense resistor through a low inductance wide and short path.
5	CS	I	Current sense input pin. Connect to the positive side of the current sense resistor through a short path.
6	COMP	O	Output of the internal transconductance error amplifier. Connect the loop compensation components between this pin and AGND.
7	AGND	GND	Analog ground pin. Connect to the analog ground plane through a wide and short path.
8	FB	I	Inverting input of the error amplifier. Connect a voltage divider from the output to this pin to set output voltage in boost/SEPIC topologies. Connect the low-side feedback resistor to AGND.
9	SS	I	Soft-start time programming pin. An external capacitor and an internal current source set the ramp rate of the internal error amplifier reference during soft start. Connect the ground connection of the capacitor to AGND.
10	RT	I	Switching frequency setting pin. The switching frequency is programmed by a single resistor between RT and AGND.

11	PGOOD	O	Power-good indicator. An open-drain output that goes low if FB is below the under-voltage threshold. Connect a pull-up resistor to the system voltage rail.
12	EN/UVLO/ SYNC	I	Undervoltage lockout programming pin. The converter start-up and shutdown levels can be programmed by connecting this pin to the supply voltage through a resistor divider. The internal clock can be synchronized to an external clock by applying a negative pulse signal into the EN/UVLO/SYNC pin. This pin must not be left floating. Connect to BIAS pin if not used. Connect the low-side UVLO resistor to AGND.
	E-PAD		The underneath exposed pad for thermal enhancement. Connect the E-PAD to the ground plane for better thermal performance of the device.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Voltage range at terminals (Refer to AGND)	BIAS	−0.3	50	V
	EN/UVLO/SYNC	−0.3	BIAS+0.2	V
	SS, RT, FB, COMP	−0.3	5.5	V
	CS (DC)	−0.3	0.3	V
	CS (100-ns transient)	−1		V
	CS (20-ns transient)	−2		V
	PGND	−0.3	0.3	V
	VCC	−0.3	22 (2)	V
	GATE (DC)	−0.3		V
	GATE (100-ns transient)	−1		V
	GATE (20-ns transient)	−2		V
	PGOOD	−0.3	18	V
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) 22V or V_{BIAS} + 0.3 V whichever is lower.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
V_{HBM}	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
V_{CDM}	Charged Device Model ESD	ANSE/ESDA/JEDEC JS-002(2)	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{BIAS}	Bias Input	3.0		45	V
V_{CC}	VCC Voltage	3.0		20	V
V_{UVLO}	UVLO Input	0		45	V
V_{FB}	FB Input	0		5.0	V

Parameter		Min	Typ	Max	Unit
f_{SW}	Typical Switching Frequency	100		2200	kHz
f_{SYNC}	Synchronization Pulse Frequency	100		2200	kHz
T_J	Junction Temperature Range	–40		125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
QFN3X2-12	63.6	29.4	59.8	°C/W

Electrical Characteristics

All test conditions: V_{BIAS} = 12 V, R_T = 9.09 kΩ, T_J = −40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Current						
$I_{SHUTDOWN(VIN)}$	BIAS Shutdown Current	V_{BIAS} = 12 V, V_{UVLO} = 0 V		2.1	5	μA
$I_{OPERATING(VIN)}$	BIAS Operating Current	V_{BIAS} = 12 V, V_{UVLO} = 2.0 V, V_{FB} = V_{REF}, RT = 220 kΩ		540	700	μA
VCC Regulation						
$V_{VCC-REG}$	VCC Regulation	V_{BIAS} = 8 V, No load	6.5	6.85	7	V
		V_{BIAS} = 8 V, I_{CC} = 35 mA	6.5			V
$V_{CC-UVLO(RISING)}$	VCC UVLO Threshold	V_{CC} rising	2.80	2.89	2.95	V
$V_{CC\_UVLO\_HYS}$	VCC UVLO Hysteresis	V_{CC} falling		0.075		V
I_{CC_CL}	VCC Sourcing Current Limit	V_{BIAS}=10 V, V_{CC} = 5 V	60	90		mA
Enable						
V_{EN_R}	Enable Threshold	EN rising	0.7	0.9	1.1	V
V_{EN_F}	Enable Threshold	EN falling	0.55	0.8	1	V
V_{EN_HYS}	Enable Hysteresis			0.1		V
UVLO/SYNC						
V_{UVLO_R}	UVLO/SYNC Threshold	UVLO rising	1.41	1.48	1.56	V
V_{UVLO_F}	UVLO/SYNC Threshold	UVLO falling	1.36	1.44	1.51	V
V_{UVLO_HYS}	UVLO/SYNC Threshold Hysteresis	UVLO falling		0.04		V
I_{UVLO}	UVLO Hysteresis Current	V_{UVLO} = 1.6 V	4.5	5	5.5	μA
SOFT START						
I_{SS}	Soft-start Current		8	10	12	μA
R_{SS_PD}	SS Pulldown Switch R_{DSON}			23		Ω
Pulse Width Modulation						
f_{SW}	Switching Frequency	RT = 220 kΩ	85	100	115	kHz
		RT = 9.09 kΩ	1900	2100	2300	kHz
$t_{ON(MIN)}$	Minimum on Time	RT = 9.09 kΩ		50		ns
D_{MAX}	Maximum Duty Cycle Limit	RT = 9.09 kΩ	81%	89%	97%	
	Maximum Duty Cycle Limit	RT = 220 kΩ	92%	95%	98%	
V_{RT}	RT Regulation Voltage		0.4	0.5	0.6	V
Current Sense						

Parameter		Conditions	Min	Typ	Max	Unit
I_{SLOPE}	Peak Slope Compensation Current	R_T = 220 kΩ	22.5	30	37.5	μA
V_{CLTH}	Current Limit Threshold (CS-PGND)		93	100	107	mV
Hiccup Mode Protection (TPQ50551, TPQ50553)						
T_{HIC}	Hiccup Enable Cycles			64		Cycles
T_{HIC_RST}	Hiccup Timer Reset Cycles			8		Cycles
Error Amplifier						
V_{REF}	FB Reference		0.99	1	1.01	V
Gm	Transconductance			1.7		mA/V
$I_{SOURCING}$	COMP Sourcing Current	V_{COMP} = 1.2 V	155			μA
V_{CLAMP_H}	COMP Clamp Voltage	COMP rising (V_{UVLO} = 2.0 V)	1.6	1.77	2.0	V
V_{CLAMP_L}	COMP Clamp Voltage	COMP falling		0.89	0.95	V
OVP						
V_{OVTH}	Overvoltage Threshold	FB rising (reference to V_{REF})	107%	110%	113%	V_{REF}
V_{OVTL}	Overvoltage Threshold	FB falling (reference to V_{REF})		105%		V_{REF}
PGOOD						
R_{PG_PD}	PGOOD Pulldown Switch R_{DSON}	1-mA sinking		81		Ω
V_{UVTH}	Undervoltage Threshold	FB falling (reference to V_{REF})	87%	90%	93%	V_{REF}
V_{UVTL}	Undervoltage Threshold	FB rising (reference to V_{REF})		95%		V_{REF}
MOSFET Driver						
V_{OH_DP}	High-state Voltage Drop	100-mA sourcing		0.26		V
V_{OL_DP}	Low-state Voltage Drop	100-mA sinking		0.16		V
Thermal Protection						
T_{SD}	Thermal Shutdown Protection Threshold	T_J rising		175		ºC
T_{SD_HYS}	Thermal Shutdown Hysteresis	T_J falling below T_{SD}		15		ºC

Typical Performance Characteristics

All test conditions: V_{BIAS} = 12 V, T_A = 25℃, unless otherwise noted.

Figure 1. Frequency vs. RT Resistance

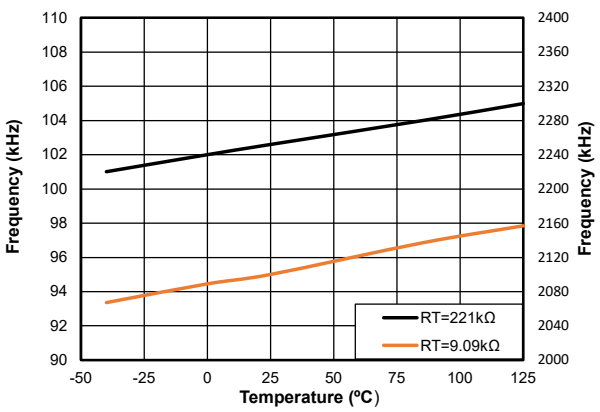


Figure 2. Frequency vs. Temperature

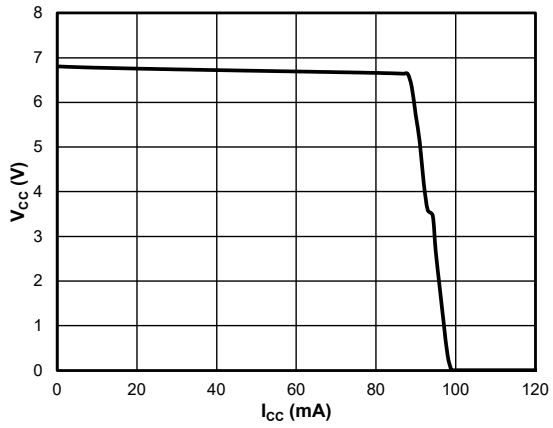


Figure 3. V_{CC} vs. I_{CC}

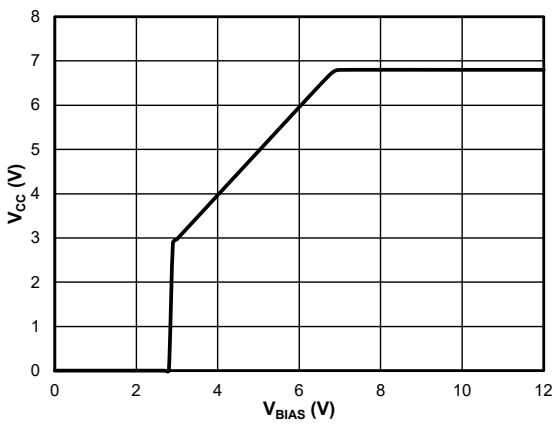
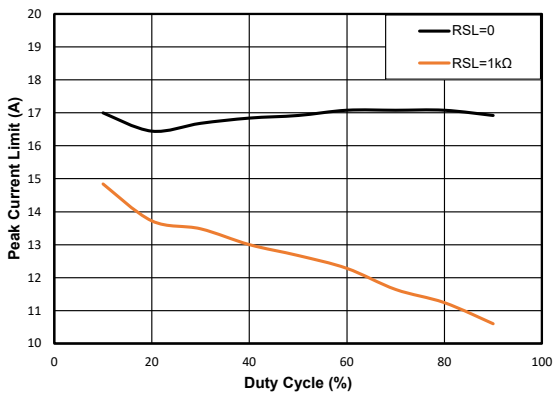
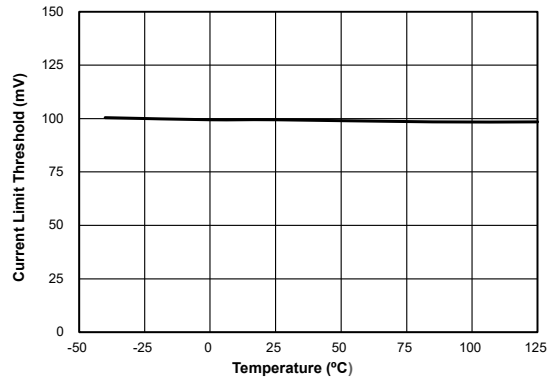


Figure 4. V_{CC} vs. V_{BIAS} (No Load)



RSL = 0 Ω, 1 kΩ

Figure 5. Peak Current Limit vs. Duty Cycle



I_{OUT} = 0 A

Figure 6. Current Limit Threshold vs. Temperature

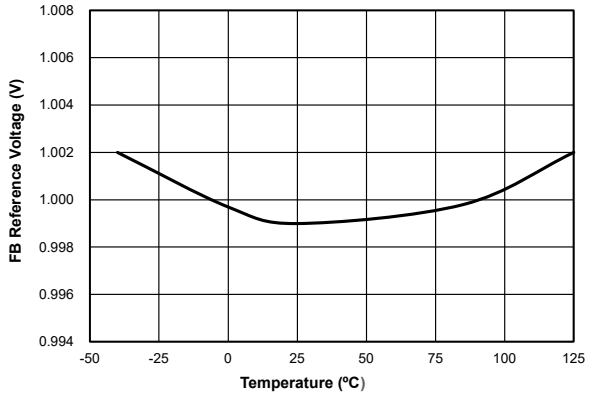


Figure 7. FB Reference vs. Temperature

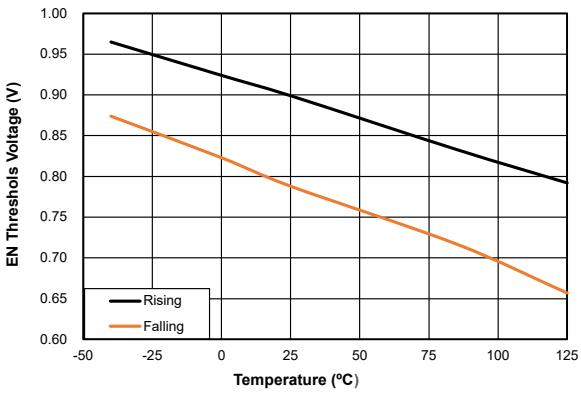
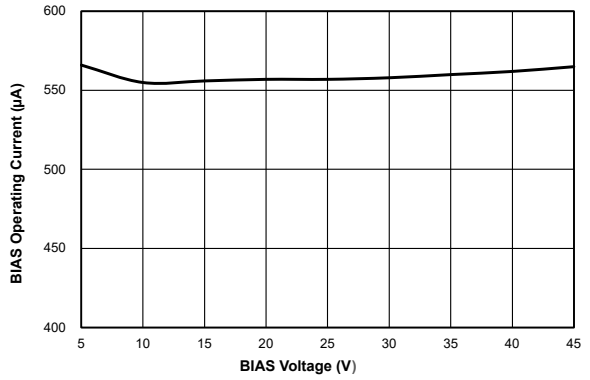


Figure 8. EN Threshold vs. Temperature



V_{FB} = V_{REF} + 0.1 V, RT = 221 kΩ, V_{CC} = 7 V, COMP = 1.75 V

Figure 9. I_{BIAS_OP} vs. V_{BIAS}

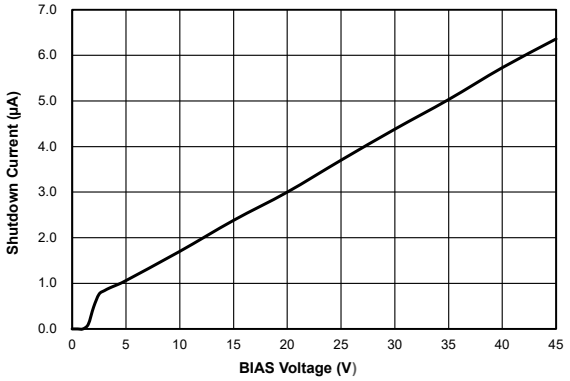
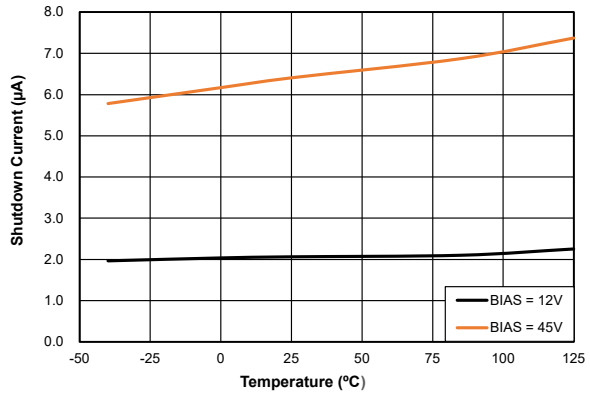


Figure 10. I_{BIAS_SD} vs. V_{BIAS}



V_{BIAS} = 12 V, V_{BIAS} = 45 V

Figure 11. I_{BIAS_SD} vs. Temperature

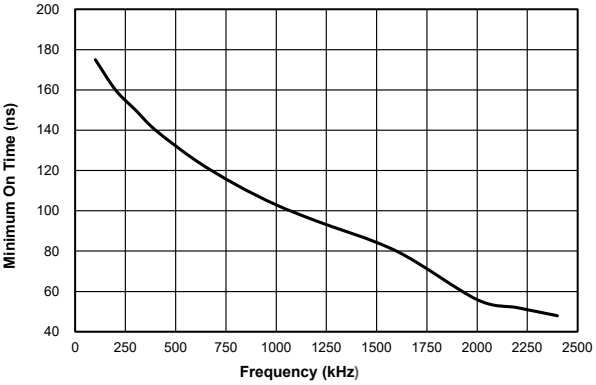


Figure 12. $T_{ON(MIN)}$ vs. Frequency

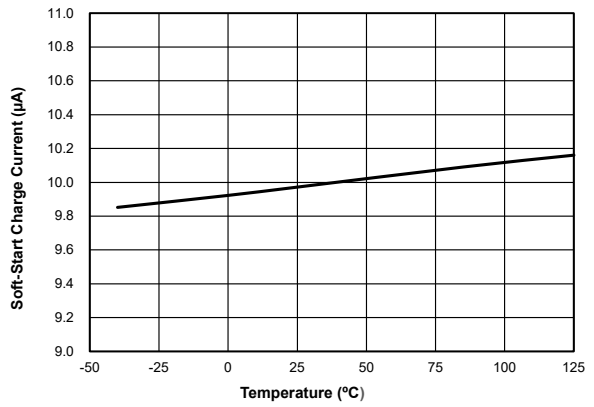


Figure 13. I_{SS} vs. Temperature

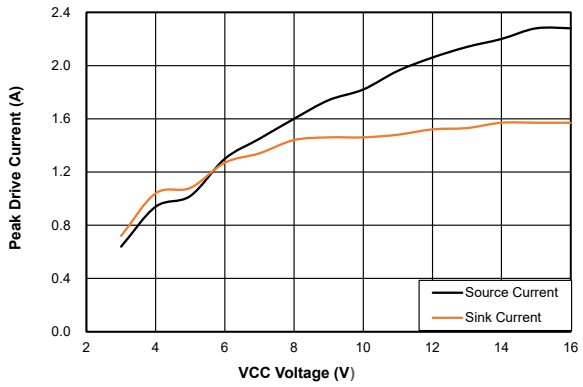


Figure 14. Peak Driver Current vs. V_{CC}

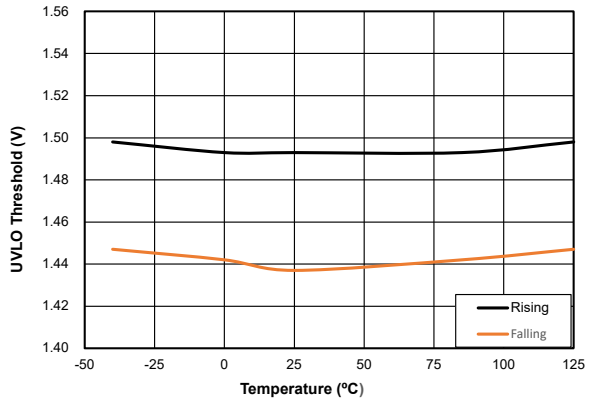


Figure 15. UVLO Threshold vs. Temperature

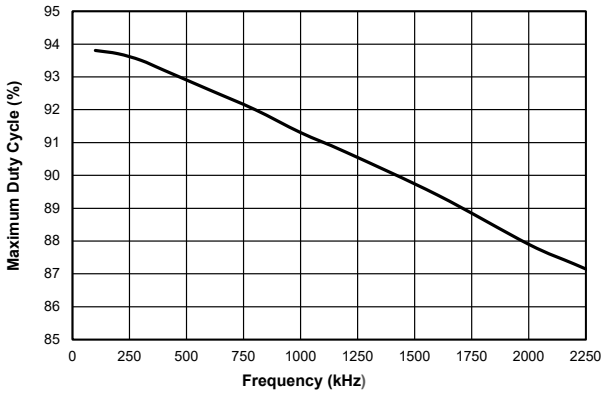


Figure 16. Maximum Duty Cycle vs. Frequency

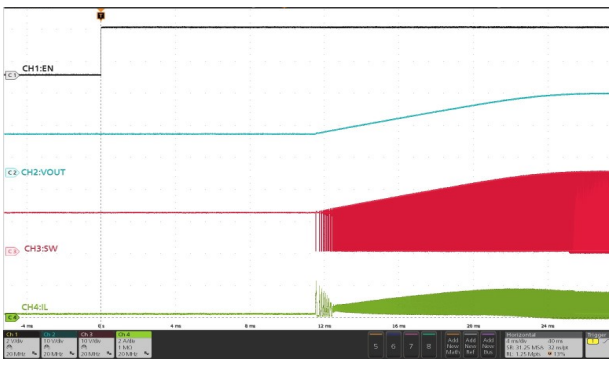


Figure 17. Startup Waveform

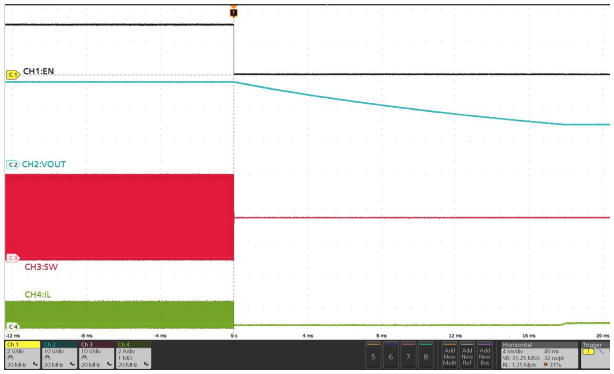


Figure 18. Shutdown Waveform

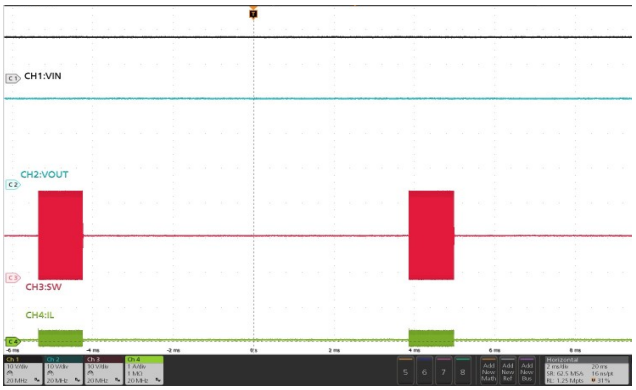


Figure 19. Switching Waveform at 0-A Load Current

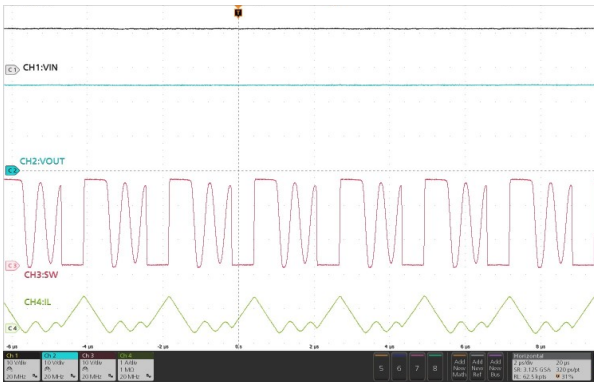


Figure 20. Switching Waveform at 0.1-A Load Current

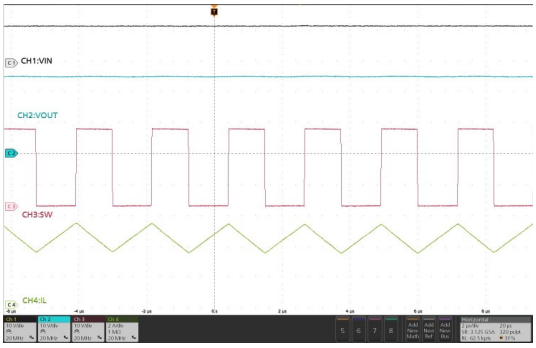
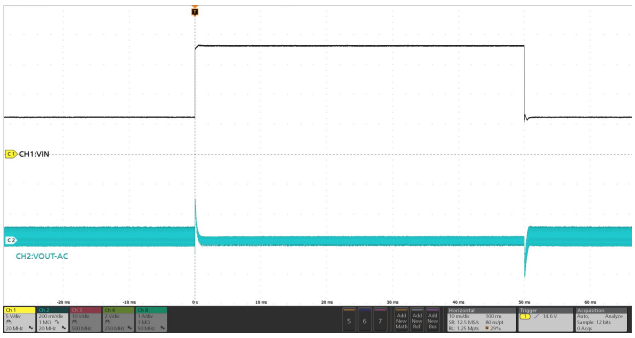
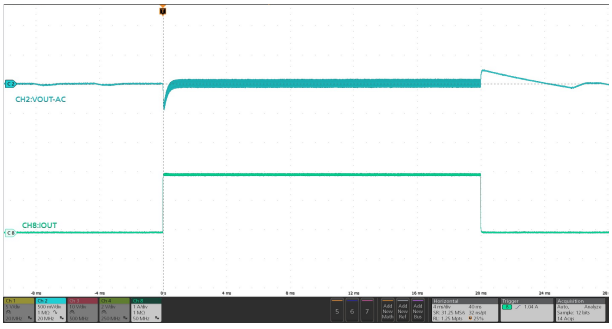


Figure 21. Switching Waveform at 2-A Load Current



V_{BIAS} from 6 V to 18 V, V_{OUT} = 24 V, I_{OUT} = 1 A

Figure 22. Line Transient



V_{BIAS} = 12 V, V_{OUT} = 24 V, I_{OUT} from 0 A to 2 A

Figure 23. Load Transient

Detailed Description

Overview

The TPQ5055x device is a 45-V wide input voltage, non-synchronous boost controller. The device uses a peak current control scheme with fast line transient and load transient response. The device can be used in boost, SEPIC, and flyback topologies.

The input power supply of the TPQ5055x can be down to 3.0 V if the BIAS pin is connected to the VCC pin. The input supply voltage for the power stage can be as low as 1.5 V if the BIAS pin is supplied by a voltage higher than 3.5 V. The internal linear regulator also supports the BIAS pin operation up to 45 V. The switching frequency is dynamically programmable with an external resistor from 100 kHz to 2.2 MHz. Switching at 2.2 MHz allows for a small solution size and fast transient response.

The device features a 1.5-A standard MOSFET driver and a low 100-mV current limit threshold. The device also supports using an external VCC supply to improve efficiency. Low operating current and pulse skipping operation improve efficiency at light loads.

The device has built-in protection features such as cycle-by-cycle current limit, overvoltage protection, input voltage UVLO, and thermal shutdown. Hiccup mode overload protection is available in the TPQ50551 and TPQ50553. The spread spectrum switching frequency dithering is available in the TPQ50552 and TPQ50553.

Additional features include low shutdown quiescent current, programmable soft start time, programmable slope compensation, precision reference, power good indicator, and external clock synchronization.

Functional Block Diagram

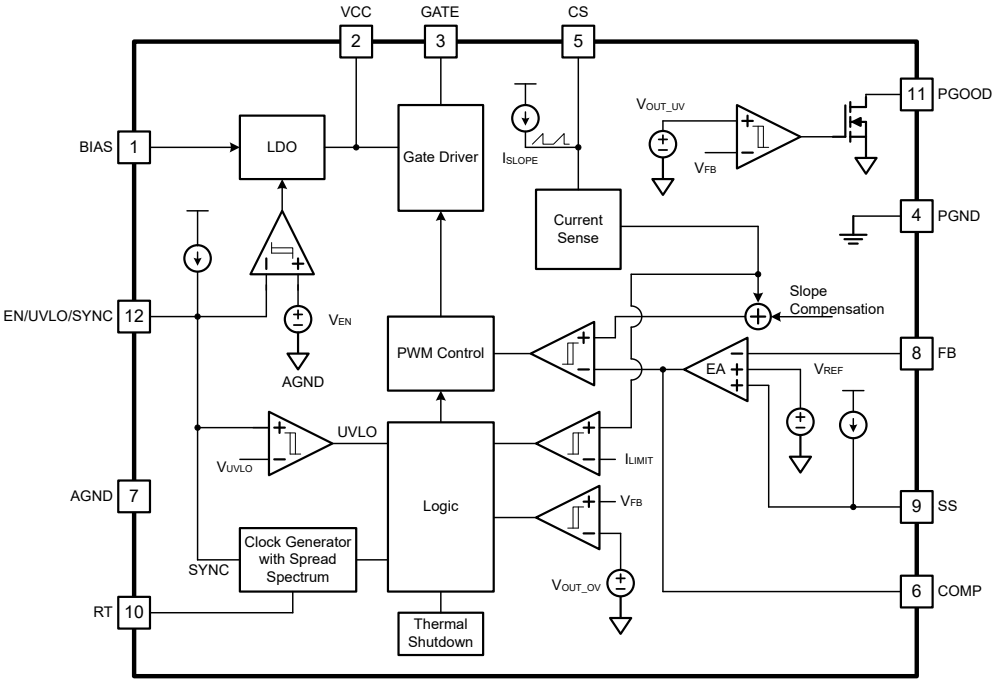


Figure 24. Functional Block Diagram

Feature Description

Enable and Programmable Input Undervoltage Lockout

The TPQ5055x has a dual function enable and input undervoltage lockout (UVLO) circuit. During power-on, when the BIAS pin voltage is higher than 3.0 V and the voltage at the EN/UVLO/SYNC pin is between the enable threshold (V_{EN}) and the UVLO threshold (V_{UVLO}) for more than 1.5 µs, the device starts up and an internal configuration starts. The device typically requires 65 µs for internal start-up and then goes into standby mode. In standby mode, the VCC regulator and the RT regulator are active, the SS pin is grounded, and there is no switching at the SW pin.

When the EN/UVLO/SYNC pin voltage continues to go up above the UVLO rising threshold, the device enters run mode. In run mode, a soft-start sequence starts when the VCC voltage is higher than the VCC UVLO threshold ($V_{CC-UVLO}$). The UVLO threshold has a 40-mV hysteresis and an additional 5-µA current source is switched on or off at the EN/UVLO/SYNC pin to make a desired hysteresis for input voltage. When the EN/UVLO/SYNC pin voltage exceeds the UVLO rising threshold, the current source is enabled to quickly raise the voltage at the EN/UVLO/SYNC pin. When the EN/UVLO/SYNC pin voltage falls below the UVLO falling threshold, the current source is disabled, causing the voltage at the EN/UVLO/SYNC pin to fall quickly. When the UVLO pin voltage is less than the enable threshold (V_{EN}), the device enters shutdown mode after a 40-µs (typical) delay with all functions disabled.

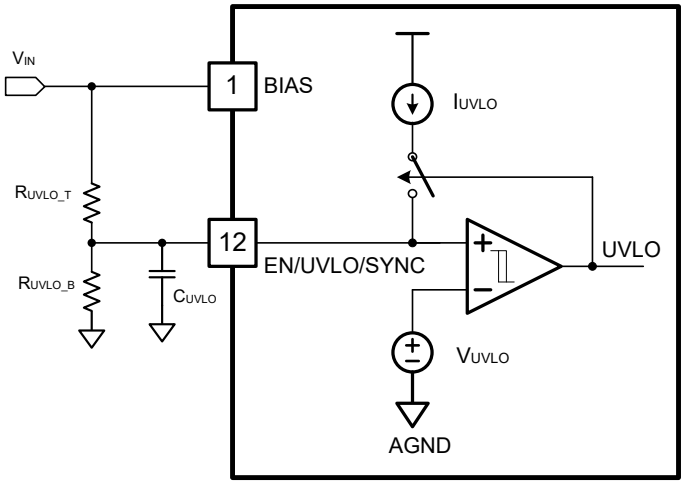


Figure 25. Input UVLO Threshold Setting

The external UVLO resistor divider must be designed so that the voltage at the EN/UVLO/SYNV pin is higher than 1.5 V (typical) when the input voltage is in the desired operating range. The values of two resistors, R_{UVLO_T} and R_{UVLO_B} can be calculated as shown in Equation 1 and Equation 2.

$$R_{UVLO\_T} = \frac{V_{IN\_ON} \times \frac{V_{ULVO\_F}}{V_{ULVO\_R}} - V_{IN\_OFF}}{I_{UVLO}} \quad (1)$$

$$R_{UVLO\_B} = \frac{V_{UVLO\_R} \times R_{UVLO\_T}}{V_{IN\_ON} - V_{UVLO\_R}} \quad (2)$$

Where

- V_{IN_ON} is the desired start-up voltage of the converter.
- V_{IN_OFF} is the desired turnoff voltage of the converter.

A UVLO glitch filtering capacitor (C_{UVLO}) is required in case the input voltage drops below the V_{IN_OFF} momentarily during the start-up or a severe load transient at the low input voltage. The UVLO filtering capacitor should be less than 1nF to allow the voltage at the UVLO pin to be quickly raised when the 5-μA hysteresis current turns on.

Do not leave the EN/UVLO/SYNC pin floating. Connect it to the BIAS pin if not used.

High Voltage VCC Regulator

The TPQ5055x has an internal wide input linear regulator sourced from the BIAS pin. The BIAS pin can be connected directly to supply voltages from 3.0 V to 45 V.

The linear regulator turns on when the device is enabled. When the BIAS pin voltage is below the VCC regulation target, the VCC output tracks the BIAS pin voltage with a small dropout voltage. When the BIAS pin voltage is higher than 6.85 V, the VCC regulator provides a 6.85-V supply for the device and the internal N-channel MOSFET driver.

The VCC regulator sources current into the capacitor connected to the VCC pin with a minimum of 60-mA capability. The recommended VCC capacitor value is from 1 μF to 4.7 μF.

The device supports a wide input range from 3.5 V to 45 V in normal configuration. By connecting the BIAS pin directly to the VCC pin, the device supports inputs from 3.0 V to 20 V. This configuration is recommended when the device starts up from a 1-cell battery.

The minimum supply voltage after start-up can be further decreased by supplying the BIAS pin from the boost converter output or from an external power supply as shown in Figure 26.

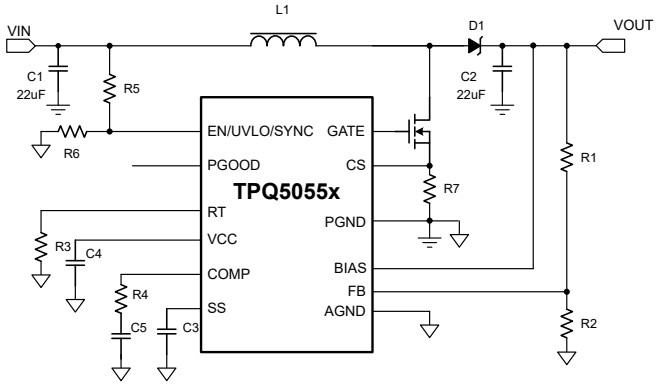


Figure 26. Decreasing the Minimum Operating Voltage after Start-up

In flyback topology, the internal power dissipation of the device can be decreased by supplying the VCC using an additional transformer winding. In this configuration, the external VCC supply voltage must be higher than the VCC regulation target ($V_{CC\text{-}REG}$), and the BIAS pin voltage must be higher than the VCC voltage because the VCC regulator includes a diode between VCC and BIAS.

If the voltage of the external VCC bias supply is higher than the BIAS pin voltage, use an external blocking diode from the input power supply to the BIAS pin to prevent the external bias supply from passing current to the boost input supply through V_{CC}.

Soft Start

The soft-start feature helps the converter gradually reach the steady state operating point, thus reducing start-up stresses and surges. The device regulates the FB pin to the SS pin voltage or the internal reference, whichever is lower.

At start-up, the internal 10-μA soft-start current source (I_{SS}) turns on 50 μs after the V_{CC} voltage exceeds the 2.85-V_{CC} UV threshold, or if the V_{CC} voltage is higher than 4.5 V, whichever comes first. The soft-start current gradually increases the voltage on an external soft-start capacitor connected to the SS pin. This results in a gradual rise of the output voltage. The

SS pin is pulled down to the ground by an internal switch when the V_{CC} is less than the V_{CC} UVLO threshold, the UVLO pin voltage is less than the UVLO threshold, during hiccup mode off-time or thermal shutdown.

In boost topology, the soft-start time (t_{SS}) varies with the input supply voltage. The soft-start time in boost topology is calculated as shown in Equation 3.

$$t_{SS} = \frac{C_{SS}}{I_{SS}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times V_{REF} \quad (3)$$

In the SEPIC topology, the soft-start time (t_{SS}) is calculated as shown in Equation 4.

$$t_{SS} = \frac{C_{SS}}{I_{SS}} \times V_{REF} \quad (4)$$

It is recommended to choose a soft-start time long enough so that the converter can start up without going into an overcurrent state.

In the primary side flyback topology, a PNP transistor can be used by connecting the base to the SS pin and emitter to the COMP pin to achieve a soft start. Figure 27 shows the implementation.

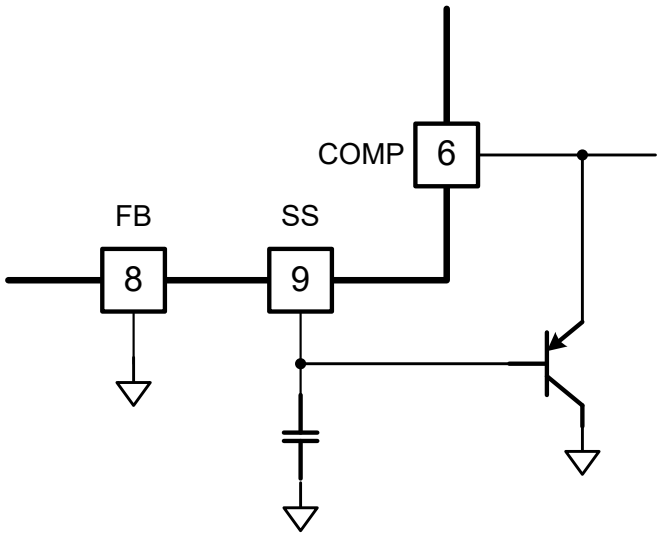


Figure 27. Soft Start Configuration in Primary Side Flyback Topology

In secondary side flyback topology, the soft start is implemented by an external RC circuit as shown in Figure 28.

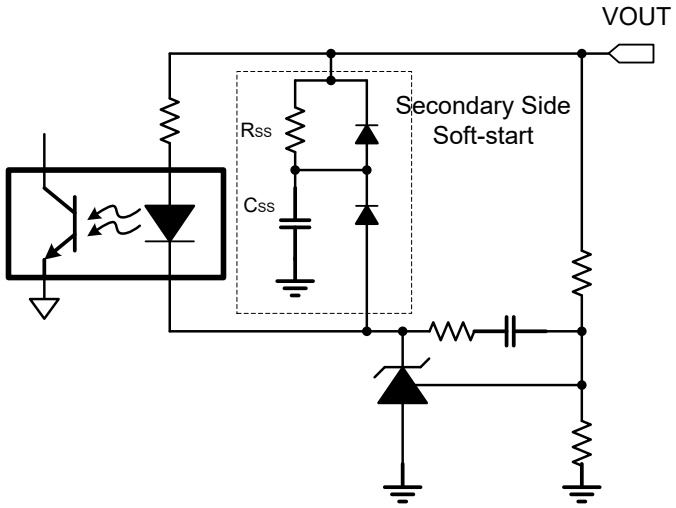


Figure 28. Soft Start Configuration in Secondary Side Flyback Topology

Switching Frequency

The switching frequency of the device can be set by a single R_T resistor connected between the R_T and the AGND pins. The resistor value R_T to set the switching frequency (f_{SW}) is calculated in Equation 5.

$$R_T = \frac{2.29 \times 10^{10}}{f_{SW(TYPICAL)}} - 1750 \quad (5)$$

The RT pin is regulated to 0.5 V by the internal RT regulator when the device is enabled.

Dual Triangle Spread Spectrum (TPQ50552 and TP50553 Only)

The TPQ50552 and TPQ50553 provide a digital spread spectrum that reduces the EMI of the power supply over a wide frequency range. The internal modulator dithers the internal clock. When an external synchronization clock is applied to the EN/UVLO/SYNC pin, the internal spread spectrum is disabled. The dual Triangle spread spectrum combines a low-frequency triangular modulation profile with a high-frequency triangular modulation profile. The low-frequency triangular modulation improves performance in lower radio frequency bands (for example, AM band), while the high-frequency triangular modulation improves performance in higher radio frequency bands (for example, FM band). In addition, the frequency of the triangular modulation is further modulated to reduce the likelihood of any audible tones. To minimize output voltage ripple caused by the spread spectrum, the duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled (see Figure 29.)

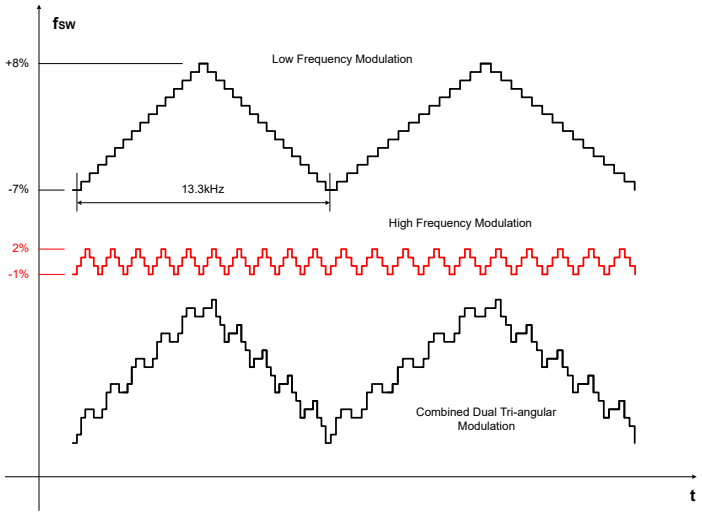


Figure 29. Dual Tri-angular Switching Frequency Dithering

Clock Synchronization

The switching frequency of the device can be synchronized to an external clock by feeding the clock into the EN/UVLO/SYNC pin. The internal clock of the device is synchronized at the falling edge but ignores the falling edge input during the forced off-time which is determined by the maximum duty cycle limit. The external synchronization clock must pull down the EN/UVLO/SYNC pin voltage below 1.45 V (typical). The duty cycle of the pulldown pulse is not limited, but the minimum pulldown pulse width must be greater than 150 ns, and the minimum pull-up pulse width must be greater than 250 ns.

When the input UVLO function is not required, the external synchronization clock can connect to the EN/UVLO/SYNC pin directly. in this configuration, it is recommended to apply the external clock pulses after the VIN is supplied. By limiting the current flowing into the EN/UVLO/SYNC pin below 1 mA using a current-limiting resistor, the external clock pulses can be supplied before the VIN power is supplied

When the input UVLO is also required with an external resistor divider connected, Figure 30 shows an implementation of the enable function and the external clock synchronization with the programmable UVLO function. The EN/UVLO/SYNC pin is pulled down by a discrete MOSFET or an open-drain output of an MCU. In this configuration, the device stops switching immediately after the EN/UVLO/SYNC pin is grounded, and the device shuts down in 35 µs (typical) after the EN/UVLO/SYNC pin is grounded.

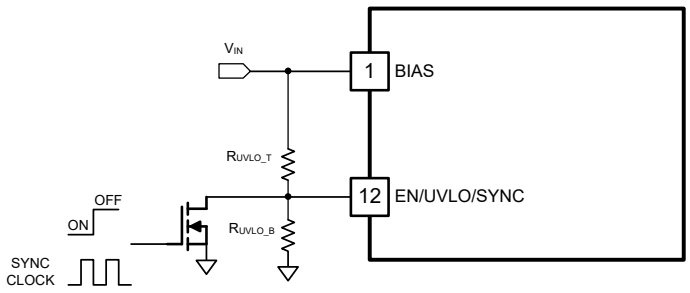


Figure 30. Enable and External Clock Synchronization with Input UVLO Function

The external clock frequency (f_{SYNC}) must be within +25% and –30% of the setting switching frequency $f_{RT(TYPICAL)}$. Because the maximum duty cycle limit and the peak current limit are affected by the clock synchronization, take extra care when using the clock synchronization function.

Current Sense and Slope Compensation

The device has a low-side current sense and provides both fixed and optional programmable slope compensation ramps, which help to prevent subharmonic oscillation at high-duty cycles. Both fixed and programmable slope compensation ramps are added to the sensed inductor current input for the PWM operation, but only the programmable slope compensation ramp is added to the sensed inductor current input for the current limit comparator (see Figure 31). For an accurate peak current limit operation over the input supply voltage, 3PEAK recommends using only the fixed slope compensation (see Figure 5).

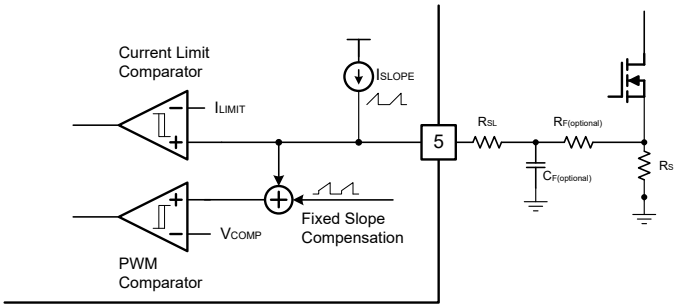


Figure 31. Current Sensing and Slope Compensation

The device can generate the programmable slope compensation ramp using an external slope resistor (R_{SL}) and a sawtooth current source with a slope of 30 μA × f_{SW}. This current flows out of the CS pin.

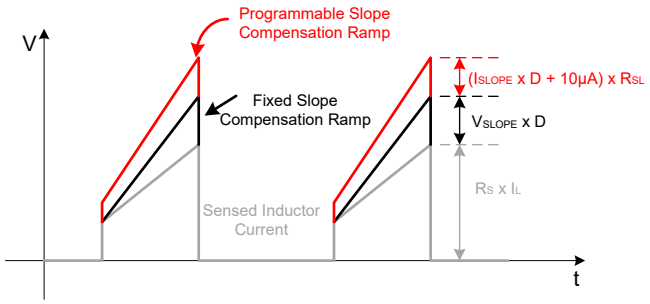


Figure 32. Slope Compensation Ramp at PWM Comparator Input

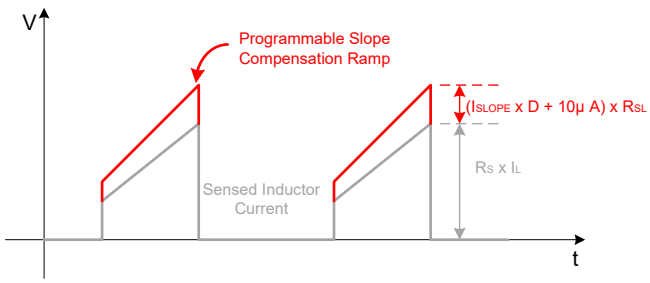


Figure 33. Slope Compensation Ramp at Current Limit Comparator Input

The slope current sourcing from the CS pin is shown by Equation 6. The internal fixed slope compensation voltage V_{SLOPE} is shown by Equation 7.

$$I_{SLOPE} = 30\mu A \quad (6)$$

$$V_{SLOPE} = 40mV \quad (7)$$

According to peak current mode control theory, the slope of the compensation ramp must be greater than half of the sensed inductor current falling slope to prevent subharmonic oscillation at the high duty cycle. Therefore, the minimum amount of slope compensation in boost topology should satisfy the following inequality:

$$0.5 \times \frac{(V_{LOAD} + V_F) - V_{IN}}{L} \times R_S \times Margin < 40mV \times f_{SW} \quad (8)$$

where

- V_F is the forward voltage drop of D1, the external diode.
- R_S is the value of the low-side current sensing resistor

The recommended value for the margin to cover non-ideal factors is 1.2. If required, R_{SL} can be added to further increase the slope of the compensation ramp. Typically 82% of the sensed inductor current falling slope is known as an optimal amount of the slope compensation. The R_{SL} value to achieve 82% of the sensed inductor current falling slope is calculated as shown in Equation 9.

$$0.82 \times \frac{(V_{OUT} + V_F) - V_{IN}}{L} \times R_S = (30\mu A \times R_{SL} + 40mV) \times f_{SW} \quad (9)$$

If clock synchronization is not used, the f_{SW} frequency equals the f_{RT} frequency. If clock synchronization is used, the f_{SW} frequency equals the f_{SYNC} frequency. The maximum value for the R_{SL} resistance is 2 kΩ.

Current Limit and Minimum On-time

The device provides cycle-by-cycle peak current limit protection that turns off the MOSFET when the sum of the inductor current and the programmable slope compensation ramp reaches the current limit threshold (V_{CLTH}). The peak inductor current limit (I_{PEAK_CL}) in steady state is calculated as shown in Equation 10.

$$I_{PEAK\_CL} = \frac{V_{CLTH} - (30\mu A \times D + 10\mu A) \times R_{SL}}{R_S} \quad (10)$$

The practical duty cycle is greater than the estimated due to voltage drops across the MOSFET and sense resistor. The estimated duty cycle is calculated as shown in Equation 11.

$$D = 1 - \frac{V_{IN}}{V_{OUT} + V_F} \quad (11)$$

Boost converters have a natural pass-through path from the supply to the load through the high-side power diode (D1). Because of this path and the minimum on-time limitation of the device, boost converters cannot provide current limit protection when the output voltage is close to or less than the input supply voltage. The minimum on-time is shown in Figure 12 and is calculated as Equation 12.

$$t_{ON(MIN)} \approx \frac{800 \times 10^{-15}}{\frac{1}{8 \times R_T} + 4 \times 10^{-6}} \quad (12)$$

If required, a small external RC filter (R_F, C_F) at the CS pin can be added to overcome the large leading-edge spike of the current sense signal. Select an R_F value in the range of 10 Ω to 200 Ω and a C_F value in the range of 100 pF to 2 nF. Because of the effect of this RC filter, the peak current limit is not valid when the on-time is less than 2 × R_F × C_F. To fully discharge the C_F during the off-time, the RC time constant should satisfy the following inequality.

$$3 \times R_F \times C_F < \frac{1 - D}{f_{SW}} \quad (13)$$

Feedback and Error Amplifier

The feedback resistor divider is connected to an internal transconductance error amplifier which features high output resistance (R_O = 10 MΩ) and wide bandwidth (BW = 7 MHz). The internal transconductance error amplifier sources current which is proportional to the difference between the FB pin and the SS pin voltage or the internal reference, whichever is lower. The internal transconductance error amplifier provides symmetrical sourcing and sinking capability during normal operation and reduces its sinking capability when the FB voltage is higher than the OVP threshold.

To set the output regulation target, select the feedback resistor values as shown in Equation 14.

$$V_{OUT} = V_{REF} \times \left(\frac{R_{FBT}}{R_{FBB}} + 1\right) \quad (14)$$

The output of the error amplifier is connected to the COMP pin, allowing the use of a Type 2 loop compensation network. R_{COMP}, C_{COMP}, and optional C_{HF} loop compensation components configure the error amplifier gain and phase characteristics to achieve a stable loop response. The absolute maximum voltage rating of the FB pin is 5.5 V. If necessary, the feedback resistor divider input can be clamped with an external zener diode.

The COMP pin features internal clamps. The maximum COMP clamp limits the maximum COMP pin voltage below its absolute maximum rating even in shutdown. The minimum COMP clamp limits the minimum COMP pin voltage to start switching as soon as possible during no load to heavy load transition. The minimum COMP clamp is disabled when the FB pin is connected to the ground in a flyback topology.

Power Good Indicator

The device has a power-good indicator (PGOOD) to simplify sequencing and supervision. The PGOOD switches to a high impedance open-drain state when the FB pin voltage is higher than the feedback undervoltage threshold (V_{UVTH}), the V_{CC} is higher than the V_{CC} UVLO threshold and the EN/UVLO/SYNC voltage is higher than the EN threshold. A 25-µs deglitch filter prevents any false pulldown of the PGOOD due to transients. The recommended minimum pullup resistor value is 10 kΩ.

Due to the internal diode path from the PGOOD pin to the BIAS pin, the PGOOD pin voltage cannot be higher than V_{BIAS} + 0.3 V.

Hiccup Mode Overload Protection (TPQ50551 and TP50553 Only)

To further protect the converter during prolonged current limit conditions, the TPQ50551 and TPQ50553 provide a hiccup mode overload protection. The internal hiccup mode fault timer of the device counts the PWM clock cycles when the cycle-by-cycle current limiting occurs. When the hiccup mode fault timer detects 64 cycles of current limiting, an internal hiccup mode off timer forces the device to stop switching and pulls down the SS pin. Then, the device will restart after 32768 cycles of hiccup mode off-time. The 64-cycle hiccup mode fault timer is reset if eight consecutive switching cycles occur without exceeding the current limit threshold. The soft-start time must be long enough not to trigger the hiccup mode protection during the soft-start time because the hiccup mode fault timer is enabled during the soft start.

To avoid an unexpected hiccup mode operation during a harsh load transient condition, it is recommended to have more margin when programming the peak-current limit.

Maximum Duty Cycle Limit and Minimum Input Supply Voltage

When designing boost converters, the maximum duty cycle should be reviewed at the minimum supply voltage. The minimum input supply voltage that can achieve the target output voltage is limited by the maximum duty cycle limit, and it can be estimated as follows.

$$V_{IN(MIN)} \approx (V_{OUT} + V_F) \times (1 - D_{MAX}) + I_{IN(MAX)} \times \left(R_{DCR} + \left(R_{DS(ON)} + R_S\right) \times D_{MAX}\right) \quad (15)$$

where

$I_{IN(MAX)}$ is the maximum input current.

R_{DCR} is the DC resistance of the inductor.

$R_{DS(ON)}$ is the on-resistance of the MOSFET.

D_{MAX} is the maximum duty cycle, which is 90%.

The minimum input voltage can be lower at the low switching frequency as the maximum duty cycle increases. Refer to Figure 16 for the maximum duty cycle at the different switching frequencies.

MOSFET Driver

The device provides an N-channel MOSFET driver that can source or sink a peak current of 1.5 A. The peak sourcing current is larger when supplying an external VCC that is higher than the 6.85-V VCC regulation target. During start-up, especially when the input voltage range is below the VCC regulation target, the VCC voltage must be sufficient to completely enhance the MOSFET. If the MOSFET drive voltage is lower than the MOSFET gate plateau voltage during start-up, the boost converter may not start up properly and it can stick at the maximum duty cycle in a high-power dissipation state. This condition can be avoided by selecting a lower threshold N-channel MOSFET switch and setting the $V_{SUPPLY(ON)}$ greater than 6 to 7 V. Since the internal VCC regulator has a limited sourcing capability, the MOSFET gate charge should satisfy the following inequality.

$$Q_{G@VCC} \times f_{SW} < 60mA \quad (16)$$

An internal 1-MΩ resistor is connected between the GATE pin and the PGND pin to prevent a false turn-on during shutdown. In boost topology, a switch node dV/dT must be limited during the 65-µs internal start-up delay to avoid a false turn-on, which is caused by the coupling through C_{DG} parasitic capacitance of the MOSFET.

Overvoltage Protection

The device has over-voltage protection (OVP) for the output voltage. OVP is sensed at the FB pin. If the voltage at the FB pin rises above the overvoltage threshold (V_{OVTH}), OVP is triggered, and switching stops. During OVP, the internal error amplifier is operational, but the maximum source and sink capability is decreased to 40 µA.

Thermal Shutdown

An internal thermal shutdown disables switching and pulls down the SS when the junction temperature exceeds the thermal shutdown threshold (T_{SD}). After the temperature is decreased by 15°C, the device performs a soft start.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPQ5055x is a wide input range, non-synchronous boost controller that uses peak current mode control. The device can be used in boost, SEPIC, and flyback topologies.

Typical Application

Figure 34 shows a typical circuit for a 12 V to 24 V boost converter.

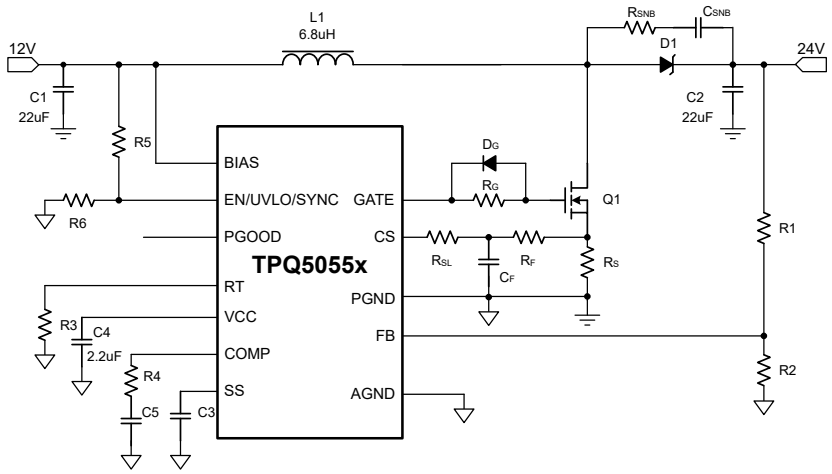


Figure 34. TPQ5055 12-V to 24-V Boost Converter Application Circuit

Inductor Selection

When selecting the inductor, consider three key parameters: inductor current ripple ratio (RR), falling slope of the inductor current, and right half-plane zero frequency (f_{RHP}).

The inductor current ripple ratio is selected to have a balance between core loss and copper loss. The falling slope of the inductor current must be low enough to prevent subharmonic oscillation at high duty cycle (additional RSL resistor is required if not). Higher f_{RHP} (= lower inductance) allows a higher crossover frequency and is always preferred when using a small value output capacitor. However, lower inductance means a higher inductor current ripple had a higher falling slope.

To balance the current ripple, right half-plane zero, and inductor falling slope, the inductance value can be selected to set the inductor current ripple between 30% and 70% of the average inductor current.

Output Capacitor

There are a few ways to select the proper value of the output capacitor (C_{OUT}). The output capacitor value can be selected based on output voltage ripple, output overshoot, or undershoot due to load transient.

The ripple current rating of the output capacitors must be enough to handle the output ripple current. By using multiple output capacitors, the ripple current can be split. In practice, ceramic capacitors are placed closer to the diode and the MOSFET than the bulk aluminum capacitors to absorb the majority of the ripple current.

Input Capacitor

The input capacitors decrease the input voltage ripple. The required input capacitor value is a function of the impedance of the source power supply. More input capacitors are required if the impedance of the source power supply is not low enough.

MOSFET Selection

The MOSFET gate driver of the device is sourced from the VCC. The maximum gate charge is limited by the 35-mA VCC sourcing current limit.

A leadless package is preferred for high switching-frequency designs. The MOSFET gate capacitance should be small enough so that the gate voltage is fully discharged during the off-time.

Diode Selection

A Schottky is the preferred type for a D1 diode due to its low forward voltage drop and small reverse recovery charge. Low reverse leakage current is an important parameter when selecting the Schottky diode. The diode must be rated to handle the maximum output voltage plus any switching node ringing. Also, it must be able to handle the average output current.

Application Examples

Low-cost LED Driver

Figure 35 is the high-voltage LED driver application. The resistor R_S is to set the LED current. The voltage drop V_S across the R_S can be set by the resistor dividers R1 and R2. Normally the V_S is set to below 0.2 V to minimize the power dissipation on the R_S. The Zener diode DZ is to clamp the output voltage when the LED string open fault condition happens.

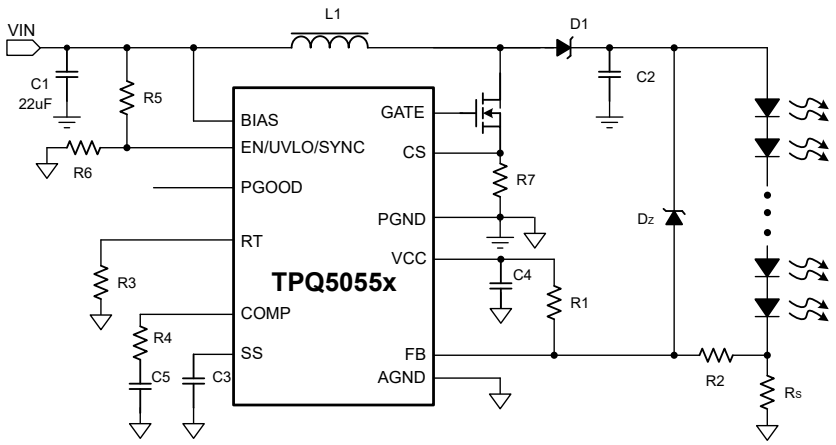


Figure 35. Low-Cost LED Driver Application Circuit

SEPIC Application

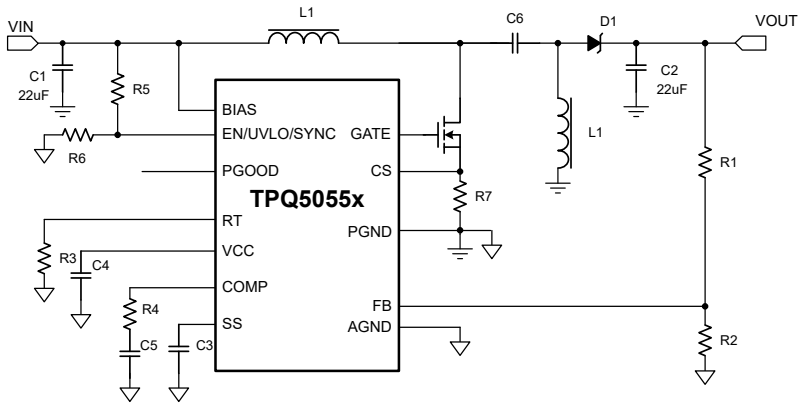


Figure 36. Typical SEPIC Application Circuit

Isolated Flyback Application

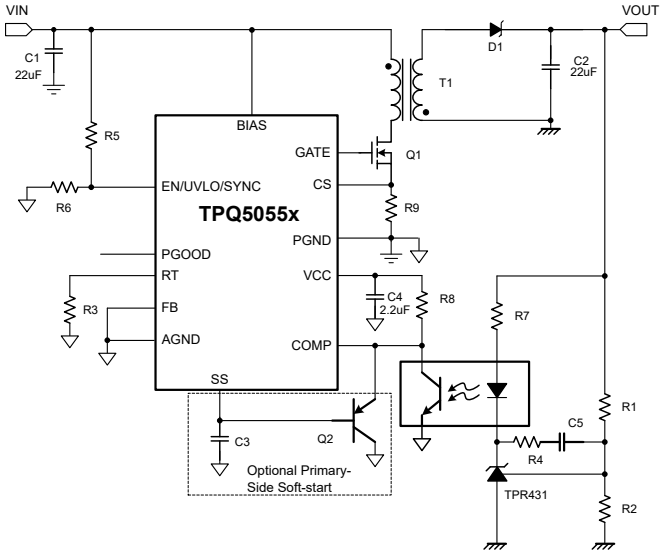


Figure 37. Secondary-Side Regulated Isolated Flyback Application Circuit

Layout

Layout Guideline

The performance of switching converters heavily depends on the quality of the PCB layout. The following guidelines will help users design a PCB with the best power conversion performance, and thermal performance, and minimize generation of unwanted EMI.

- Put the MOSFET Q1, diode D1, and current sense resistor R_S on the board first.
- Use a small-size ceramic capacitor for output capacitor C_{OUT}.
- Make the switching loop (C_{OUT} to D1 to Q1 to R_S to C_{OUT}) as small as possible.
- Leave a copper area near the D1 diode for thermal dissipation.
- Put the device near the R_S resistor.
- Put the C_{VCC} capacitor as near the device as possible between the VCC and PGND pins.
- Use a wide and short trace to connect the PGND pin directly to the center of the sense resistor.
- Connect the CS pin to the center of the sense resistor. If necessary, use vias.
- Connect a filter capacitor between the CS pin and power ground trace.
- Connect the COMP pin to the compensation components (R_{COMP} and C_{COMP}).
- Connect the CCOMP capacitor to the analog ground trace.
- Connect the AGND pin directly to the analog ground plane. Connect the AGND pin to the R_{UVLOB}, R_T, C_{SS}, and R_{FBB} components.
- Connect the exposed pad to the AGND and PGND pins under the device.
- Connect the GATE pin to the gate of the Q1 FET. If necessary, use vias.
- Make the switching signal loop (GATE to Q1 to R_S to PGND to GATE) as small as possible.
- Add several vias under the exposed pad to help conduct heat away from the device. Connect the vias to a large ground plane on the bottom layer.

Layout Example

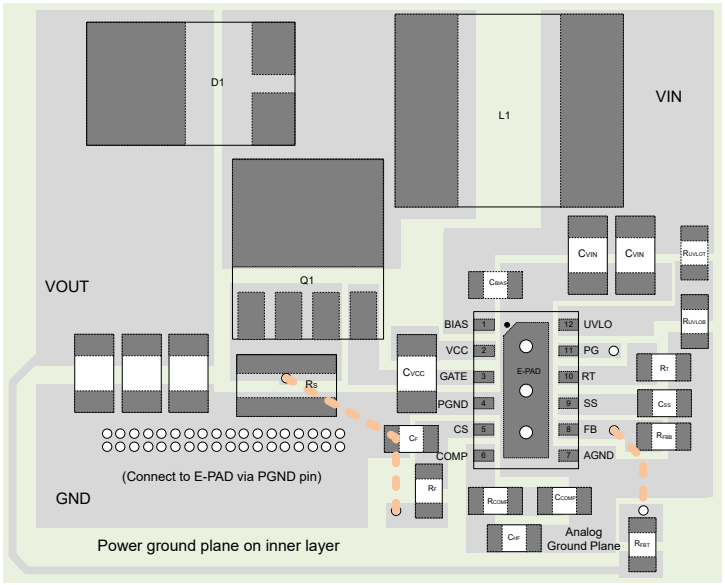
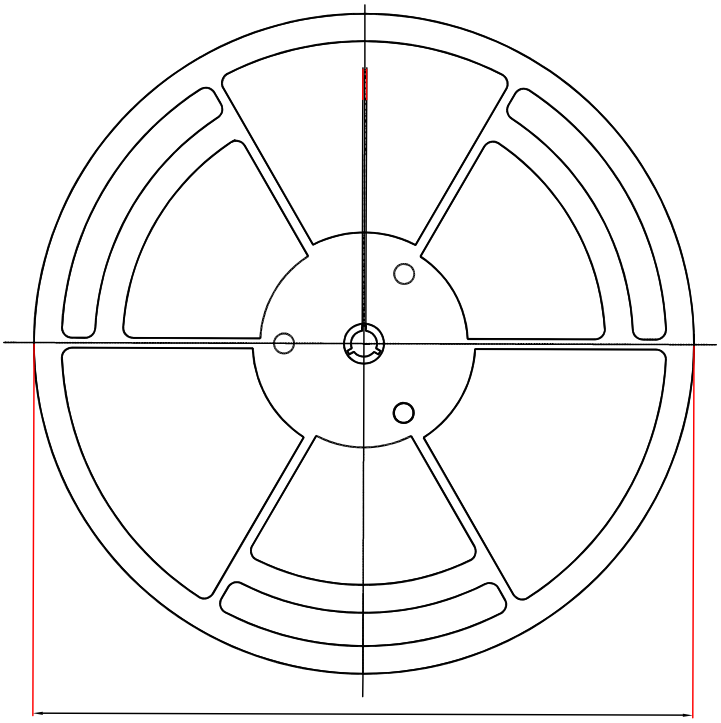
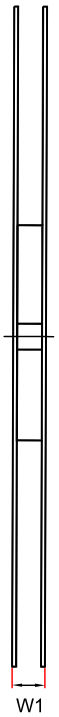
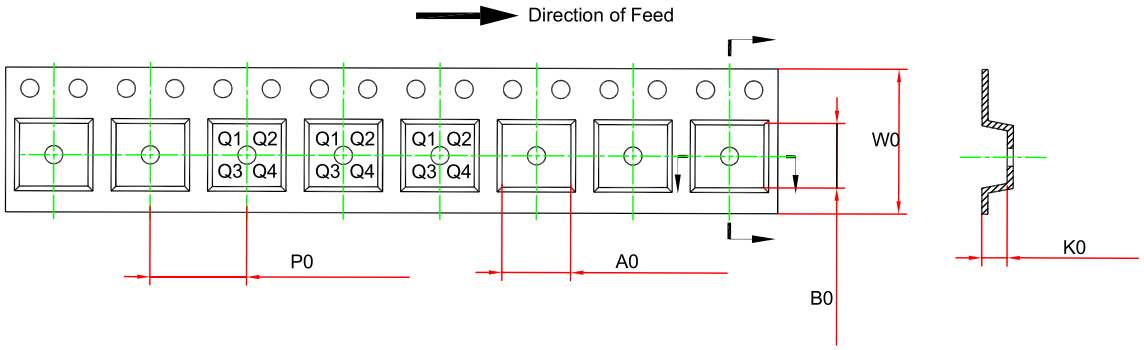


Figure 38. PCB Layout Example for Boost Converter

Tape and Reel Information





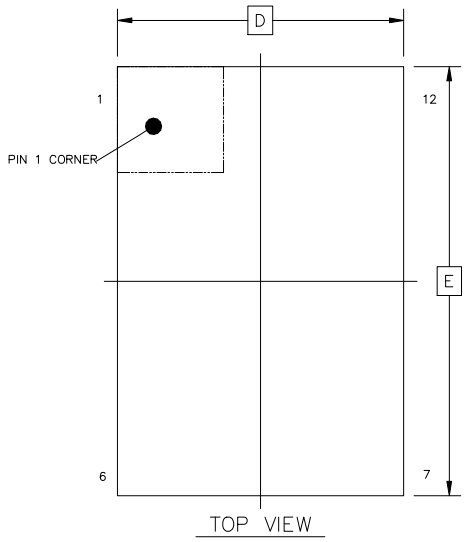


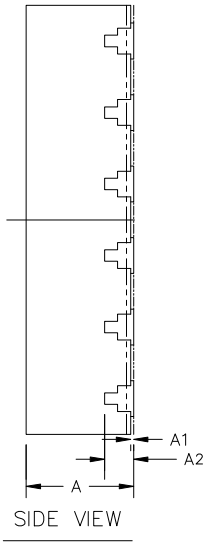
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPQ5055-DFTR-S	DFN3X2-12	180	13.1	2.3	3.3	1.1	4	8	Q1
TPQ50551-DFTR-S	DFN3X2-12	180	13.1	2.3	3.3	1.1	4	8	Q1
TPQ50552-DFTR-S	DFN3X2-12	180	13.1	2.3	3.3	1.1	4	8	Q1
TPQ50553-DFTR-S	DFN3X2-12	180	13.1	2.3	3.3	1.1	4	8	Q1

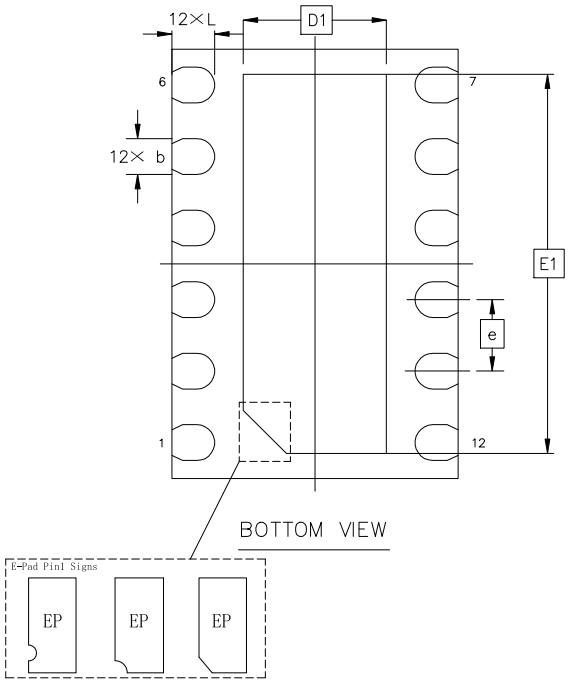
Package Outline Dimensions

DFN3X2-12

Package Outline Dimensions DFT(DFN3X2-12-A)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 BSC	
b	0.200	0.300	0.008	0.012
D	1.900	2.100	0.075	0.083
D1	0.900	1.100	0.035	0.043
E	2.900	3.100	0.114	0.122
E1	2.550	2.750	0.100	0.108
e	0.500 BSC		0.020 BSC	
L	0.250	0.350	0.010	0.014

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPQ5055-DFTR-S	−40ºC – 125ºC	DFN3X2-12	055	2	Tape & Reel, 3000	Green
TPQ50551-DFTR-S	−40ºC – 125ºC	DFN3X2-12	551	2	Tape & Reel, 3000	Green
TPQ50552-DFTR-S (1)	−40ºC – 125ºC	DFN3X2-12	552	2	Tape & Reel, 3000	Green
TPQ50553-DFTR-S (1)	−40ºC – 125ºC	DFN3X2-12	553	2	Tape & Reel, 3000	Green

(1) For future products, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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