2.7-V to 16-V Input, 12-A Synchronous Step-Down Regulator with Remote Sense and Adjustable Current Limit

Features

- 3-V to 16-V Input Voltage Range with Internal VCC Bias
- 2.7-V to 16-V Input Voltage Range with External VCC Bias from 3 V to 5 V
- Adjustable and Accurate Current Limit Level
- Adjustable Switching Frequency with Fixed Frequency Function: 600 kHz, 800 kHz, 1 MHz
- Stable with Zero ESR Output Capacitor
- Selectable Power-Save Mode or Forced-PWM Mode
- Adjustable Soft Start from 1 ms and Smoothly Pre-bias Power up
- 0.6-V ±0.5% Reference Voltage Accuracy from 0℃ to +85℃
- 0.6-V ±1% Reference Voltage Accuracy from −40℃ to +125℃
- Integrated Output Track and Discharge Function
- Non-latch for OCP, UVP, UVLO, OTP, Latch-off for OVP
- Available in the QFN3X4-21 Package

Applications

- Server
- Telecom and Communication Equipment
- Switch and Access Point
- Industrial PC

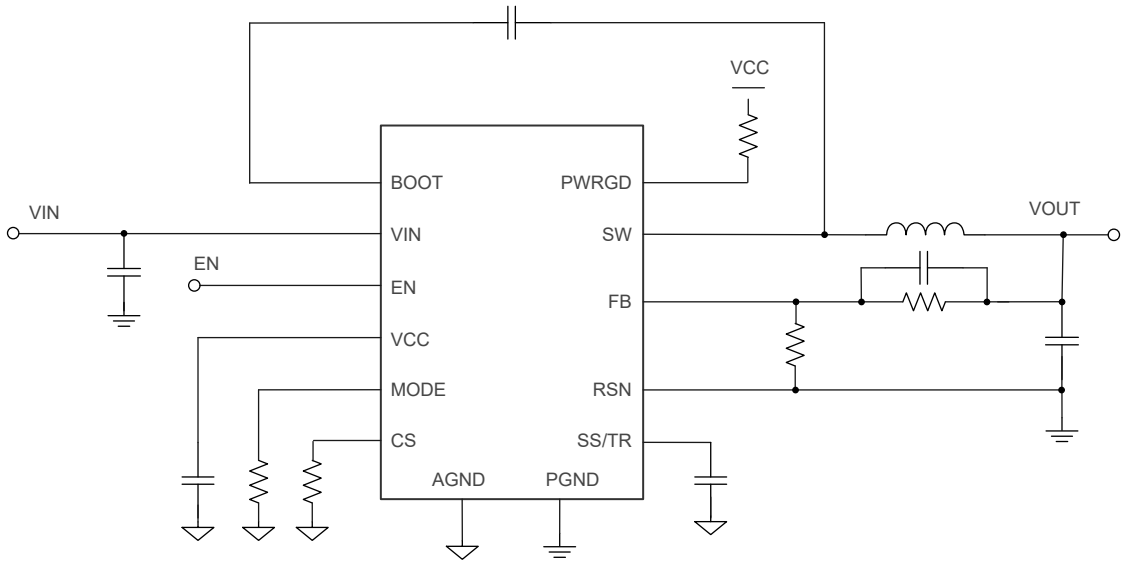
Description

The TPP21206 is a high-efficiency, easy-to-use, fully integrated synchronous step-down regulator with 2.7-V to 16-V wide input voltage range and 12-A continuous output current capability. One internal LDO is integrated for a compact single-input power supply. A wide range of external VCC bias from 3 V to 5 V can replace the internal LDO to further enhance the efficiency of the system.

The TPP21206 adopts fast transient response, constant-on-time control with fixed frequency function over different duty cycle and load current range. Differential remote sense feedback with 1% accuracy reference voltage over the full operating temperature range ensures excellent output accuracy and regulation. The high-integrated compensation provides a stable control loop with zero ESR output capacitors, supporting flexible component selection and easy-control stability.

The device features adjustable and accurate current limits for both high-side, low-side positive, and low-side negative current limit to ensure safety. The open-drain PWRGD with active clamped output can enhance the supply reliability during system malfunction. The device has built-in protection and diagnostic features such as cycle-by-cycle current limit, under-voltage protection, over-voltage protection, UVLO, and over-temperature protection.

Typical Application Circuit



2.7-V to 16-V Input, 12-A Synchronous Step-Down Regulator with Remote Sense and Adjustable Current Limit

Table of Contents

Product Family Table

Order Number	Package
TPP212060-FC5R	QFN3X4-21

Revision History

Date	Revision	Notes
2025-06-15	Rev.A.0	Initial release.

Pin Configuration and Functions

TPP21206
QFN3X4-21
Top View

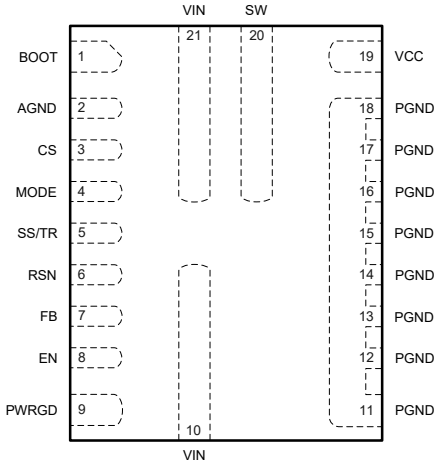


Table 1. Pin Functions: TPP21206

Pin No.	Name	I/O	Description
1	BOOT	O	High-side MOSFET gate supply pin. Recommend connecting a 0.1-μF ceramic capacitor between BOOT and SW pins.
2	AGND	G	Analog ground pin. The reference point for control circuits. Connect to the analog ground plane at the point of the ground of the VCC capacitor.
3	CS	I/O	Current limit setting pin. Connect a resistor to the AGND pin to set the valley current limit value.
4	MODE	I	Operation mode setting pin. Connect a resistor between the MODE pin and the AGND pin to select FPWM/PSM operation and switching frequency.
5	SS/TR	I/O	Soft start and tracking input pin. When using the soft start function, connect an external capacitor to this pin to set the output start-up time; When using the tracking function, the external DC voltage on this pin overrides the internal voltage reference to set the output voltage.
6	RSN	I	Differential remote-sensing ground pin. Connect this pin directly to the negative side of the remote voltage sense point. Short to AGND if the remote sense is not used.
7	FB	I	Voltage feedback pin. Connect the output voltage and the RSN pin with a feedback resistor divider to set the output value.
8	EN	I	Enable the input pin. An input signal to turn the regulator on or off. Connect this pin to the VIN pin with a pull-up resistor or a resistor divider. Do not leave the EN pin floating.

Pin No.	Name	I/O	Description
9	PWRGD	O	Power-good indicator pin. An open-drain output which is actively clamped low if the output voltage is outside the normal regulation range. Connect a pull-up resistor to one system voltage rail.
10, 21	VIN	P	Input voltage supply pin. Input capacitors should be placed as close to this pin and the PGND pin as possible.
11-18	PGND	G	Power ground pin. The reference ground of the internal power stage. Use the connection with wide PCB traces.
19	VCC	I/O	Internal LDO pin. The power supply for the driver and control circuits. Connect a ceramic bypass capacitor from this pin to the AGND pin. An external VCC supply can be connected to overdrive the internal LDO to enhance the efficiency.
20	SW	O	Switching output pin. Connect this pin to the external inductor.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
VIN	Supply Voltage	−0.3	18	V
SW	Switching Node Voltage	−0.3	18	V
	Switching Node Voltage (less than 25 ns transient)	−5	25	V
BOOT	Bootstrap to SW Voltage	−0.3	6	V
VCC	Internal Supply Voltage	−0.3	6	V
	All Other Pins	−0.3	6	V
RSN	Remote Sense Voltage	−0.3	0.3	V
T_J	Junction Temperature Range	−40	150	°C
T_S	Storage Temperature Range	−55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
VIN	Input Voltage Range When VCC Pin is Powered by External Bias	2.7	16	V
VIN	Input Voltage Range When VCC Pin is Powered by Internal VCC LDO	3.0	16	V
SW	Switching Node Voltage	− 0.3	VIN + 0.3	V
	Switching Node Voltage (less than 25 ns transient)	− 5	VIN + 0.3	V
VOUT	Output Voltage Range	0.6	5.5	V
VCC	External VCC Bias	3.12	5	V
IOUT	Maximum Output Current		12	A
T_J	Junction Temperature Range	− 40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
QFN3X4-21	56.37	18.42	25.41	°C/W

Electrical Characteristics

Unless otherwise noted, the min and max limits apply over the recommended operating ambient temperature range (T_A) of −40°C to 125°C. Typical values are measured under T_A = 25°C and represent the most likely parameters normally for reference. The default test conditions: V_{IN} = 12 V, internal VCC LDO.

Parameter		Conditions	Min	Typ	Max	Unit
Input Supply						
I_{Q_VIN}	VIN Quiescent Current	V_{IN} = 12 V, V_{EN} = 2 V, non-switching, no external bias on VCC		730		μA
I_{SD_VIN}	VIN Shut Down Current	V_{IN} = 12 V, V_{EN} = 0 V, no external bias on VCC		1	15	μA
I_{Q_VCC}	VCC Quiescent Current	V_{IN} = 12 V, V_{EN} = 2 V, non-switching, external bias 3.3V on VCC		660		μA
I_{SD_VCC}	VCC Shut Down Current	V_{IN} = 12 V, V_{EN} = 0 V, external bias 3.3 V on VCC		40	60	μA
VIN_{UVLO_R}	VIN UVLO Rising Threshold	VIN Rising, external bias 3.3 V on VCC	2.1	2.55	2.7	V
VIN_{UVLO_F}	VIN UVLO Falling Threshold	VIN Falling, external bias 3.3V on VCC	1.55	1.9	2.15	V
Enable						
V_{EN_R}	Enable Voltage Rising Threshold	Enable rising	1.15	1.20	1.25	V
V_{EN_F}	Enable Voltage Falling Threshold	Enable falling	0.95	1.00	1.05	V
I_{EN}	Enable Input Leakage Current	V_{EN} = 2 V		0		μA
MOSFET						
R_{DSON_HS}	High-side MOSFET on-resistance	V_{EN} = 2 V, T_A = 25°C		14		mΩ
R_{DSON_LS}	Low-side MOSFET on-resistance	V_{EN} = 2 V, T_A = 25°C		4		mΩ
Current Limit						
V_{LIMIT}	Current Limit Reference			0.3		V
G_{OCP_LS}	I_{CS} to I_{OUT} Ratio	I_{OUT} > 2 A		5		μA/A
I_{LIMIT_LS}	Low-side Current Limit		12	14	16	A
I_{LIMIT_HS}	High-side Current Limit		14.5	16.5	18.5	A
I_{NG}	Low-side Negative Current Limit			-9.5		A
I_{ZC}	Zero-cross Detection Current Threshold	V_{IN} = 12 V with internal LDO		200		mA
BOOT Supply						
$VBOOT_{UV\_F}$	Bootstrap UVLO Falling Threshold	T_A = 25°C, V_{IN} = 12 V, $V_{BOOT-SW}$ falling		2.1		V
VCC Regulator						

Parameter		Conditions	Min	Typ	Max	Unit
VCC	Internal LDO Output	V_{IN} = 12 V, I_{LOAD_VCC} = 2 mA		3.1		V
VCC_{UVLO_R}	Internal VCC UVLO Rising Threshold	VCC rising	2.8	2.87	2.94	V
VCC_{UVLO_F}	Internal VCC UVLO Falling Threshold	VCC falling	2.62	2.7	2.77	V
I_{VCC_LIM}	VCC LDO Short Circuit Current Limit			90		mA
Voltage Reference						
V_{REF}	Internal Voltage Reference Range	T_A = 0°C to 85°C	597	600	603	mV
		T_A = –40°C to 125°C	594	600	606	mV
I_{FB}	Feedback Input Leakage Current	V_{FB} = V_{REF}		1		nA
V_{OS_EA}	EA Amplifier Offset			0		mV
Switching Frequency						
f_{SW}	Switching Frequency, FPWM Operation		540	600	700	kHz
			720	800	880	kHz
			850	1000	1100	kHz
T_{ON_MIN}	Minimum on-time			60		ns
T_{OFF_MIN}	Minimum off-time			180		ns
Soft Start and Tracking (SS/TR)						
T_{SS}	Internal Fixed Soft Start Time	Output rising from 0 V to 95% of final setpoint, $C_{SS/TR}$ = 1 nF		1	1.5	ms
I_{SOURCE}	SS/TR Sourcing Current	$V_{SS/TR}$ = 0 V		42		μA
I_{SINK}	SS/TR Sinking Current	$V_{SS/TR}$ = 1 V		12		μA
Voltage Protection						
V_{OVP}	Over-Voltage Protection Threshold		113%	116%	119%	
V_{UVP}	Under-Voltage Protection Threshold		77%	80%	83%	
Power Good						
V_{PG_TH}	PWRGD Threshold	FB rising, PWRGD Low to High	89%	92%	95%	
		FB rising, PWRGD High to Low	113%	116%	119%	
		FB falling, PWRGD High to Low	77%	80%	83%	
V_{PG_OLP}	Output Limitation Protection Threshold	FB rising, PWRGD Stays High	103%	106%	109%	
V_{PG_LOW}	PWRGD Low-level Output Voltage	I_{PWRGD} = 10 mA, V_{IN} = 12 V, internal VCC			150	mV
T_{PG_DLYR}	Delay for PWRGD from Low to High			1		ms

Parameter		Conditions	Min	Typ	Max	Unit
T_{PG_DLYF}	Delay for PWRGD from High to Low			0.5		μs
I_{PG_LKG}	PWRGD Leakage Current	T_A = 25°C, V_{PWRGD} = 3.3 V			5	μA
$V_{PG\_CLAMP\_LOW}$	PWRGD Clamp Low Output Voltage @ V_{IN} =12 V	VCC = 0 V, V_{EN} = 0 V, PWRGD pulled up to 3.3 V through one 100 kΩ resistor		0	5	mV
	PWRGD Clamp Low Output Voltage @ V_{IN} =0 V	VCC = 0 V, V_{EN} = 0 V, PWRGD pulled up to 3.3 V through one 100 kΩ resistor		710	850	mV
		VCC = 0 V, V_{EN} = 0 V, PWRGD pulled up to 3.3 V through one 10 kΩ resistor		850	1000	mV
VCC_{MIN_PG}	Minimum VCC for Valid PWRGD Output	V_{IN} = 0 V, V_{EN} = 0 V, PWRGD pulled up to 3.3 V through One 100 kΩ resistor, V_{PWRGD} ≤ 0.4 V			1.3	V
Output Discharge						
R_{ON_DIS}	Output Discharge Resistance			95		Ω
Thermal Shutdown						
T_{SD}	Thermal Shutdown Threshold	Rising temperature		160		°C
T_{HYS}	Thermal Shutdown Hysteresis			30		°C

Typical Performance Characteristics

All test conditions: V_{IN} = 12 V, V_{OUT} = 1.2 V, F_{SW} = 800 kHz, FPWM Mode, T_A = 25 °C, unless otherwise noted.

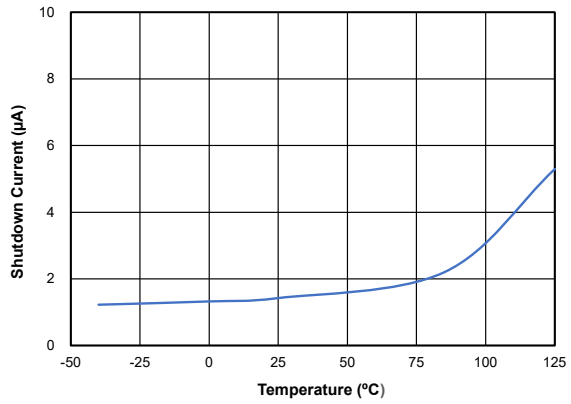


Figure 1. Input Shutdown Current

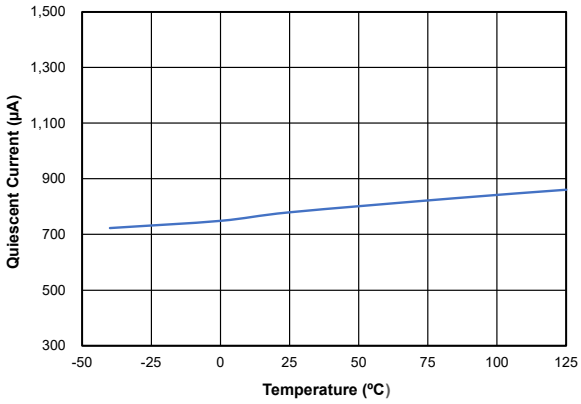
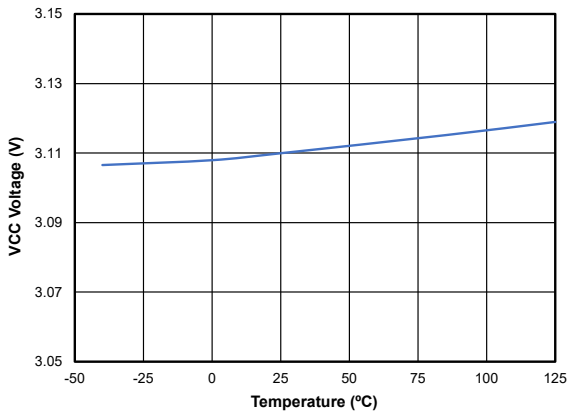
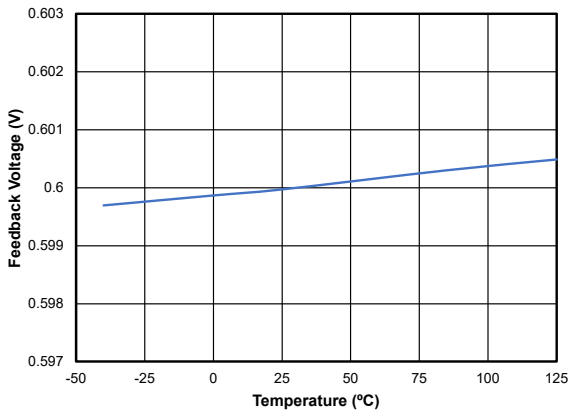


Figure 2. Input Quiescent Current



I_{VCC} = 2 mA

Figure 3. Internal VCC LDO



I_{VCC} = 2 mA

Figure 4. Feedback Voltage

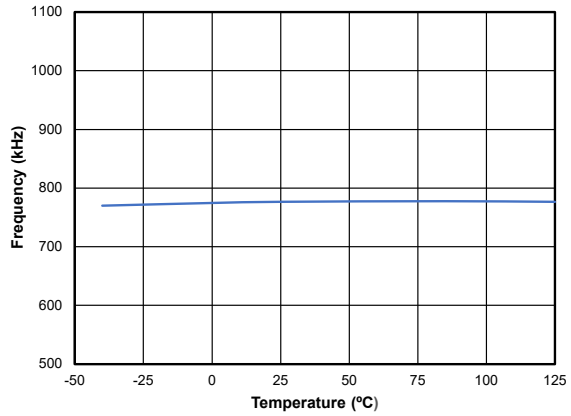


Figure 5. Switching Frequency

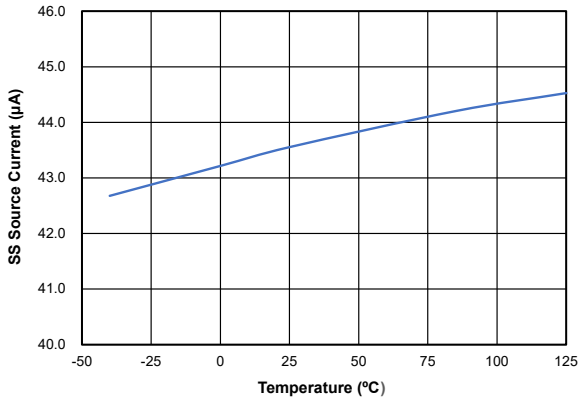


Figure 6. Soft Strat Sourcing Current

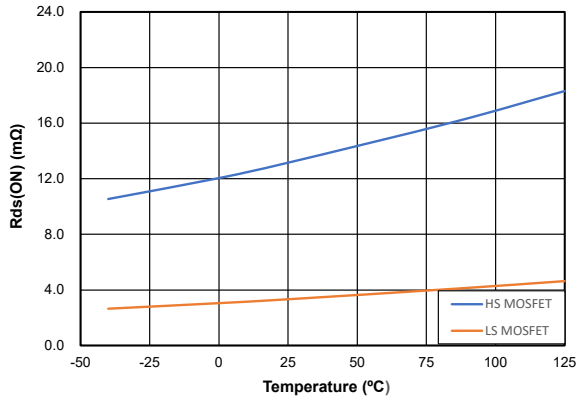


Figure 7. High-side and Low-side MOSFET

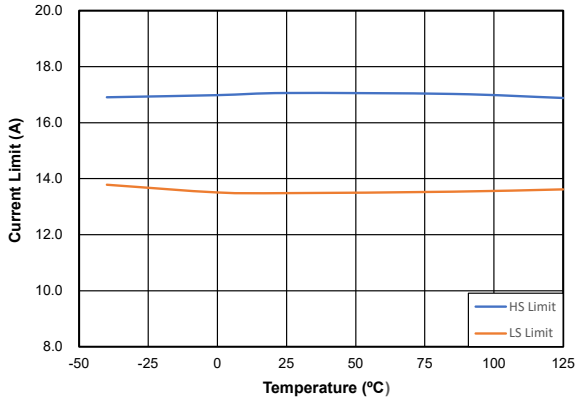


Figure 8. High-side and Low-side Current Limits

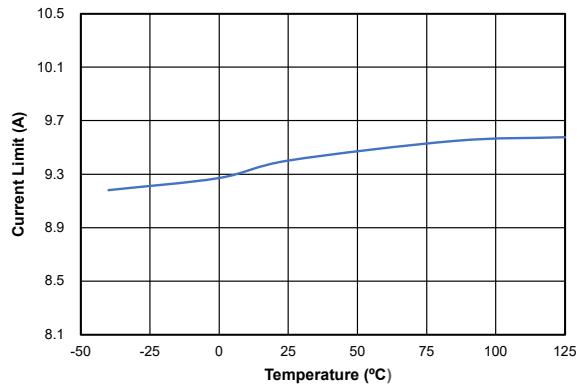


Figure 9. Low-side Negative Current Limit

Detailed Description

Overview

The TPP21206 is a high-efficiency, easy-to-use, fully integrated synchronous step-down regulator with 2.7-V to 16-V wide input voltage range and 12-A continuous output current capability. One internal LDO is integrated for a compact single-input power supply. A wide range of external VCC bias from 3 V to 5 V can replace the internal LDO to further enhance the efficiency of the system.

The TPP21206 adopts fast transient response, constant-on-time control with fixed frequency function over different duty cycles and load current ranges. Differential remote sense feedback with 1% accuracy reference voltage over the full operating temperature range ensures excellent output accuracy and regulation. The high-integrated compensation provides a stable control loop with zero ESR output capacitors, supporting flexible component selection and easy-control stability.

The device features adjustable and accurate current limits for both high-side, low-side positive, and low-side negative current limit to ensure safety. The open-drain PWRGD with active clamped output can enhance the supply reliability during system malfunction. The device has built-in protection and diagnostic features such as cycle-by-cycle current limit, under-voltage protection, over-voltage protection, UVLO, and over-temperature protection.

Functional Block Diagram

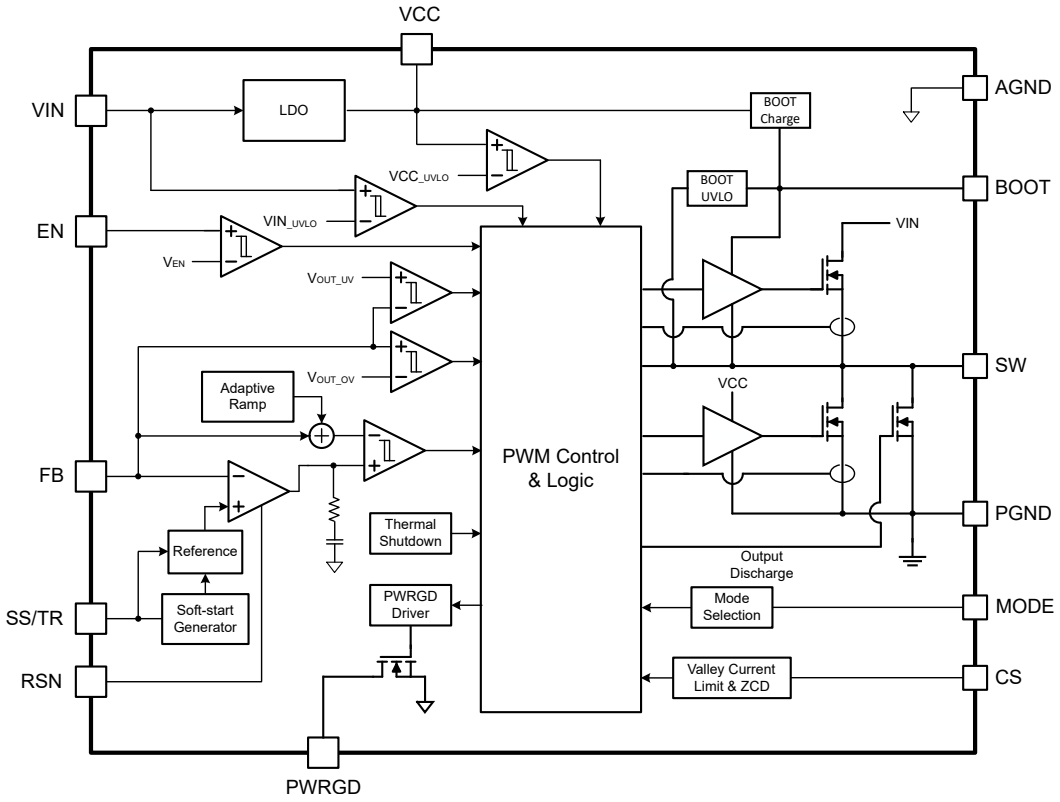


Figure 10. Functional Block Diagram

Feature Description

Constant-on-time Control with Fixed Frequency Loop

The TPP21206 adopts constant-on-time control to achieve the fast load transient performance and the easy use of external components. An error amplifier is integrated to provide the accurate output voltage and excellent load regulation over the whole load range. The feedback voltage is sensed from the resistor divider through the FB pin to compare with the internal voltage reference. The device also integrates an internal ripple compensation to support low-ESR output capacitors such as MLCC. The adaptive internal ramp is optimized to ensure the device is stable in the whole operating voltage range with proper design of the external components.

The output of the error amplifier is superimposed onto the internal ripple compensation and directly compared with the feedback voltage. When the feedback voltage drops below the superimposed signal, the high-side MOSFET turns on for a fixed on-time determined by the one-shot generator. The fixed on-time is mainly determined by the input voltage, output voltage, and selected switching frequency. When the fixed high-side on-time elapses, the low-side MOSFET turns on after the dead time until the feedback voltage drops below the superimposed signal again. The device regulates the output voltage stable by operating in this way.

For constant-on-time control, the on-time generated by the one-shot generator typically has deviation from the accurate on-time value, especially in different duty cycle and load current conditions. In the small duty cycle conditions, the actual switching frequency deviates from the setting frequency largely. When the load current is large, the efficiency loss also leads to the switching frequency deviation. One fixed frequency loop is integrated in the constant-on-time architecture of the TPP21206 to maintain the switching frequency fairly constant under different application conditions.

Mode Selection

The TPP21206 provides FPWM mode to optimize the output ripple and PSM mode to improve the light load efficiency. In FPWM mode, the device operates in continuous conduction mode (CCM) during light-load conditions. During CCM operation, the switching frequency is almost constant over the entire load range. In PSM mode, the inductor current also decreases when the load decreases until the inductor current reaches zero. The low-side MOSFET turns off when the zero-inductor current is detected. As the load current decreases further, the device runs into discontinuous conduction mode (DCM). During DCM operation, the on-time is maintained similar to that during CCM operation.

The TPP21206 also has three options for switching frequency selection: 600 kHz, 800 kHz, and 1000 kHz. The operation mode and switching frequency are selected by connecting a resistor from the MODE pin to the AGND pin. One ±1% tolerance resistor is recommended, and the resistor values are listed in the table below.

Mode	Light Load Operation	Switching Frequency
VCC	PSM	600 kHz
243 kΩ (±10%) to AGND	PSM	800 kHz
121 kΩ (±10%) to AGND	PSM	1000 kHz
AGND	FPWM	600 kHz
30.1 kΩ (±10%) to AGND	FPWM	800 kHz
60.4 kΩ (±10%) to AGND	FPWM	1000 kHz

VCC LDO and External Bias Function

The TPP21206 integrates an internal VCC LDO powering input from VIN and output to VCC. The VCC LDO provides the power supply for the driver and control circuits. An external bias which is above the output of the internal VCC LDO can override the internal LDO. This function can enhance the efficiency of the system because the internal driver and control circuits are now powered from the external bias instead of the internal VCC LDO.

The VCC pin needs to be decoupled with a minimum 1-μF ceramic capacitor as close to VCC as possible. The VCC UVLO circuit monitors the VCC voltage and disables the internal circuits when the VCC voltage falls below the VCC UVLO threshold. Maintaining a stable and clean VCC voltage to provide a smooth operation of the device.

Enable Control and Power-on Sequence

When the enable voltage rises above the enable threshold and the input voltage rises above the UVLO rising threshold, the TPP21206 enters its internal power-on sequence. When using the applications of such default internal VCC LDO, the internal power-on sequence is described below.

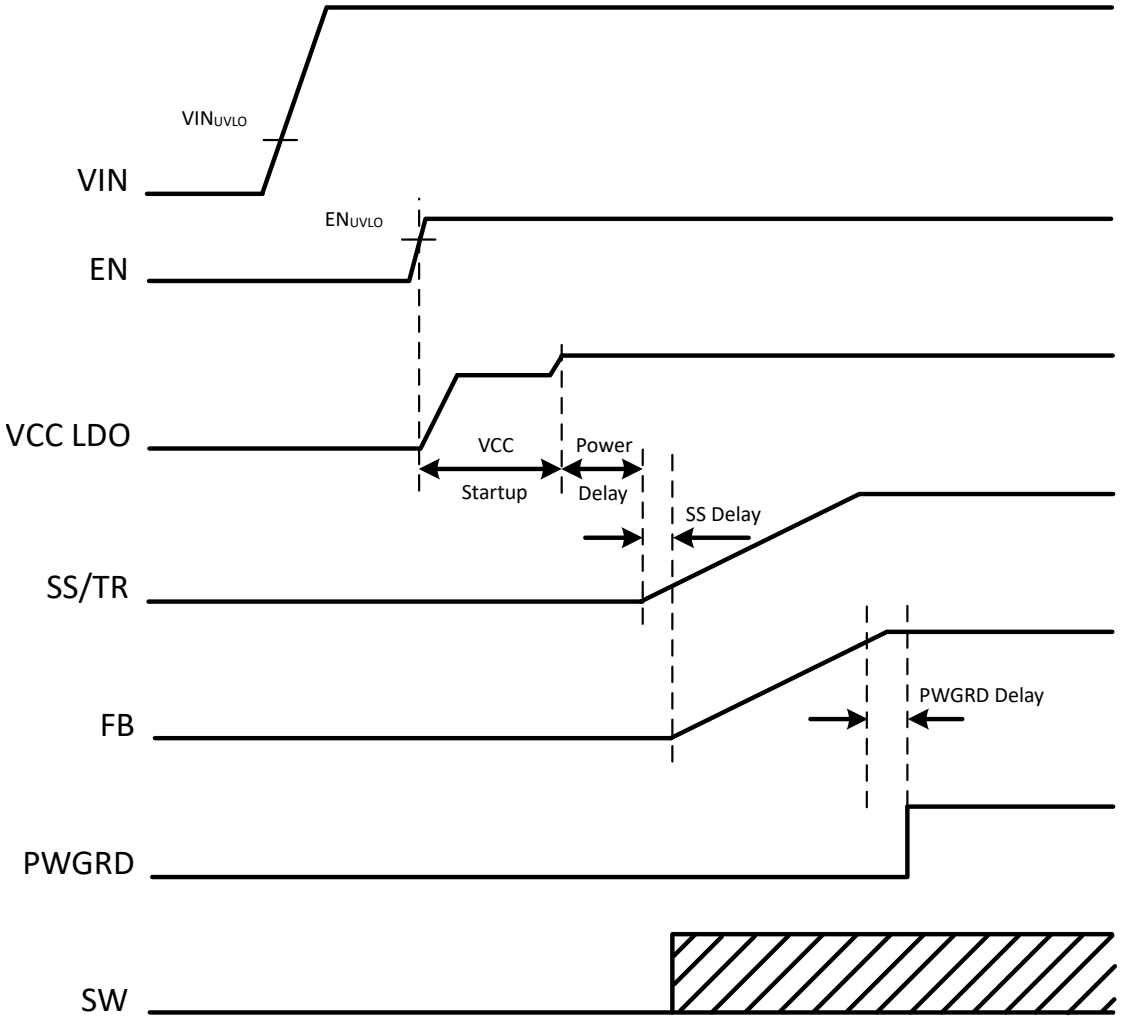


Figure 11. Power-on Sequence with Internal VCC LDO

1. The input supply rises above the UVLO threshold and the enable control rises above the enable threshold.

2. The internal VCC voltage is charged up on the bypass capacitor. If the input supply ramps up very slowly, the VCC voltage is limited by the input voltage level, and the VCC start-up time can be extended longer.

3. When the VCC voltage rises above the VCC UVLO threshold, the soft start ramp starts, and the device begins to switch after the power-on delay.

When using the applications of the external bias on the VCC pin, the internal power-on sequence is described below.

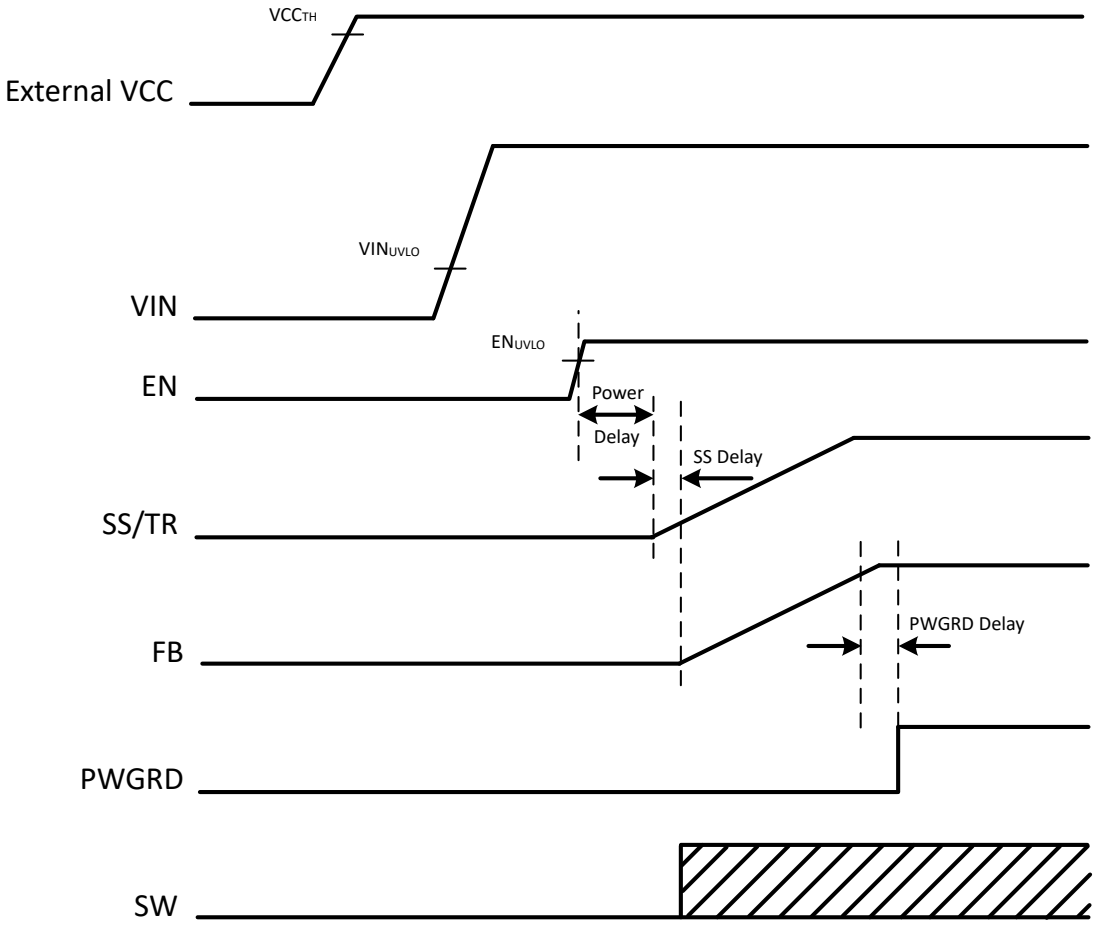


Figure 12. Power-on Sequence with External Bias

1. The external VCC voltage is built up already and rises above the VCC UVLO threshold.
2. The input supply rises above the UVLO threshold, and the enable control rises above the enable threshold.
3. The soft start ramp starts and the device begins to switch after the power-on delay.

Soft Start

The TPP21206 integrates a soft start function to control the inrush current during start-up. The device supports both internal fixed soft start and external adjustable soft start. The internal soft start time is typically 1 ms which is also the minimum soft start time. It can be increased by adding a capacitor C_{SS} between the SS/TR pin and ground.

The soft start time T_{SS} is determined by the following equation.

$$T_{SS}(ms) = \frac{C_{SS}(nF) \times 0.6\,(V)}{I_{SOURCE}(\mu A)} \quad (1)$$

Differential Output Remote Sense

The TPP21206 supports differential output remote sense function through the FB and RSN pins. The RSN pin helps sense the remote ground voltage, cooperating with the remote output sense. This function compensates for the potential voltage drop on the PCB traces and maintains the output voltage accuracy under steady state and load transient operation. The connection of the remote sense trace should be kept in low impedance and implement Kelvin sensing to achieve the best performance. To maintain a stable output voltage and minimize the output ripple, the pair of remote sensing traces should

stay away from any noise sources such as inductor, and SW nodes, or high-frequency clock traces. It is recommended to shield the pair of remote sensing traces with ground planes.

Pre-bias Start up

The TPP21206 also supports a monotonic start-up with pre-biased loads. If the output voltage is pre-biased to a certain value during start-up, the device disables switching for both high-side and low-side power switches until the soft-start reference voltage exceeds the feedback voltage.

Output Discharge

When the device is disabled through EN or triggers the protections, such as UVLO or thermal shutdown, it enables the output discharge function. This function forces both high-side and low-side MOSFETs to latch off but turns on the discharge MOSFET. The MOSFET is connected between the SW and ground to directly discharge the output voltage.

Power Good

The device employs an open-drain output PWRGD signal to check whether the output voltage is operating within the normal range. The external pull-up voltage resource is recommended to be less than 5.5 V (such as VCC) with a 1-kΩ resistor. After the feedback voltage reaches 92% of the reference voltage, PWRGD is pulled high after a short time. Once the feedback voltage is lower than 80% or greater than 116% of the internal reference voltage, the PWRGD is pulled low. The TPP21206 still has the ability to pull the PWRGD pin low when the input supply is provided while the enable voltage is low.

Protection

Undervoltage Lockout (UVLO)

The device monitors the voltage on both the VIN and the VCC pins. Both VIN and VCC UVLO protections are non-latching protections. When the VCC pin voltage drops below the UVLO falling threshold, the device shuts down. When the VCC pin voltage increases above the UVLO rising threshold, the device turns on.

When the VIN pin voltage drops below the UVLO falling threshold but the VCC pin voltage remains higher than the UVLO rising threshold, the device stops switching and shuts down. Once the VIN pin voltage increases above the UVLO rising threshold, the device turns back on and switches again. It can be adjusted by using the EN pin with an external resistor divider.

V_{UVLO_R} is the desired system-level undervoltage protection rising threshold voltage, and V_{UVLO_F} is the desired system-level undervoltage protection falling threshold voltage. V_{EN_R} and V_{EN_F} are rising and falling enable thresholds. R_{UVLO_H} and R_{UVLO_L} can be calculated below.

$$V_{UVLO\_R} = \left(1 + \frac{R_{UVLO\_H}}{R_{UVLO\_L}}\right) \times V_{EN\_R} \quad (2)$$

$$V_{UVLO\_F} = \left(1 + \frac{R_{UVLO\_H}}{R_{UVLO\_L}}\right) \times V_{EN\_F} \quad (3)$$

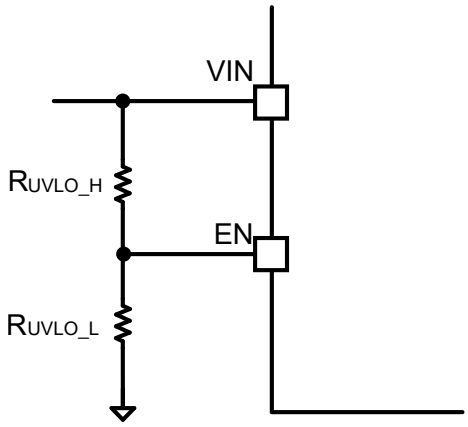


Figure 13. UVLO Adjustment

Valley Current Limit

The TPP21206 employs a cycle-by-cycle valley current limit to prevent the positive inductor current from running away. The inductor current is monitored when the low-side MOSFET turns on. If the monitored current of the low-side MOSFET exceeds the valley current limit, the low-side MOSFET remains on until the current returns to the safe level.

The valley current limit protection limits the inductor current without a latch-off behavior. During an overcurrent condition, the load current exceeds the valley current limit; thus, the output voltage tends to decrease. It ends up with triggering the under-voltage protection (UVP) threshold. Refer to the UVP section for details.

The valley current limit can be programmable through an external resistor from the CS pin to the ground. One ±1% tolerance resistor is recommended to ensure an accurate current limit threshold. The valley current limit threshold setting from the resistor can be calculated by below equation.

$$I_{LIMIT\_LS} = \frac{V_{LIMIT}}{R_{LIMIT}(\Omega) \times G_{OCP\_LS}} \quad (4)$$

where V_{LIMIT} is the Current limit reference, and R_{LIMIT} is the current limit resistor value.

Peak Current Limit

The TPP21206 also employs a fixed, cycle-by-cycle peak current limit. The current is monitored when the high-side MOSFET turns on. If the monitored current of the high-side MOSFET exceeds the peak current limit, the high-side MOSFET turns off to avoid the inductor current from further increasing. Delay needs to be taken into account which may cause the sensed current to be slightly different from open-loop current limits.

Negative Current Limit

The TPP21206 also employs a fixed, cycle-by-cycle negative current limit. Similar to the valley current limit, the current is monitored when the low-side MOSFET turns on. If the monitored current of the low-side MOSFET exceeds the negative current limit, the low-side MOSFET turns off, and then the high-side MOSFET turns on for a proper time. After the high-side MOSFET on-time expires, the low-side MOSFET turns on again.

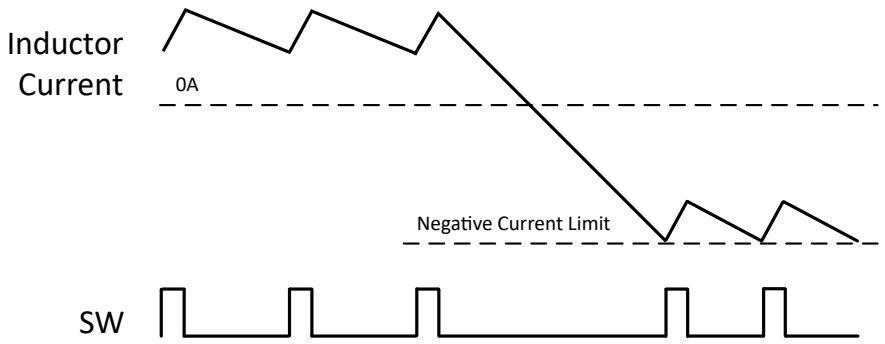


Figure 14. Negative Current Limit Operation

Under Voltage Protection (UVP)

If the output voltage drops lower than 80% of the regulation voltage level, the UVP comparator detects and an internal delay counter is triggered. After this UVP delay time, the device enters the hiccup mode. The UVP function is enabled after the soft-start period is complete.

Over Voltage Protection (OVP)

If the output voltage rises higher than 116% of the regulation voltage level, the OVP comparator detects and the device latches off the high-side MOSFET and turns on the low-side MOSFET until the device reaches the negative current limit. Upon reaching the negative current limit, the low-side MOSFET turns off and the high-side MOSFET turns on again. The device operates in this operation until the output voltage is pulled below the UVP threshold voltage for approximately 60 µs. After the UVP delay time, both the high-side MOSFET and the low-side MOSFET are latched off. The fault is cleared with a reset of VIN or by re-toggling the EN pin.

Output Limitation Protection

The TPP21206 employs the output limitation protection to regulate the output voltage to the targeted value. It protects the output voltage at a much lower overvoltage threshold of 5% above the regulation voltage level. The output limitation protection does not trigger the over-voltage fault, so this protection is non-latching. During the protection, the device operates in forced-PWM mode. The low-side MOSFET turns on beyond the zero inductor current, which quickly discharges the output capacitors to help regulate the output voltage to the set value. During the protection, the cycle-by-cycle negative current limit is also activated to ensure the safe operation of the internal power switches.

Short Circuit Protection

To further ensure the protection during prolonged overload or short circuits, the device features hiccup overload protection. When the inductor current is clamped at the set current limit and the feedback voltage drops below the UVP threshold, the device enters the hiccup mode. Entering the hiccup sleep period for approximately 20 ms, the device stops switching and restarts a normal soft start operation after the recovery time. If the overload still exists, the device keeps switching with the current limit and turns off the power switches again. The device can automatically recover to normal operation when the overload condition is removed. The hiccup function is disabled at the normal soft start period to avoid being mistakenly triggered.

Thermal Shutdown

Once the temperature of the device rises above the internal over-temperature shutdown threshold, the internal temperature sensor shuts down the device. The device recovers operating when the temperature falls below the threshold with hysteresis.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPP21206 is a high-efficiency, easy-to-use, fully integrated synchronous step-down regulator with 2.7-V to 16-V wide input voltage range and 12-A continuous output current capability. The TPP21206 adopts constant-on-time control to achieve the fast load transient performance and the easy use of external components. The device provides FPWM mode to optimize the output ripple and PSM mode to improve the light load efficiency. The device also has three options for switching frequency selection: 600 kHz, 800 kHz, and 1000 kHz. The operation mode and switching frequency are selected by connecting a resistor from the MODE pin to the AGND pin.

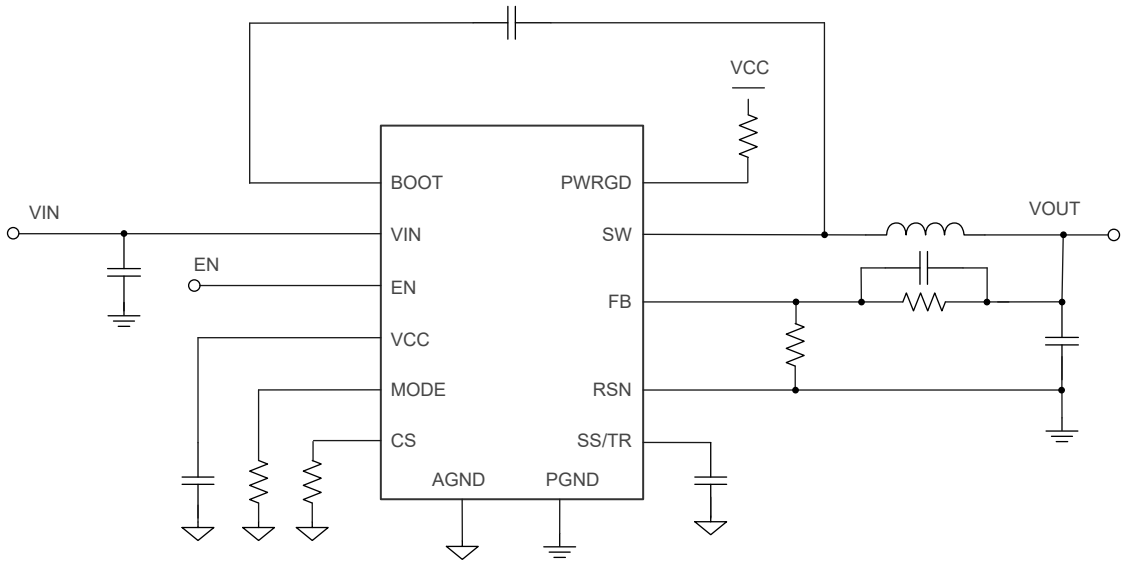


Figure 15. Typical Application Circuit

Choosing Switching Frequency

Switching frequency of the DCDC regulator is a compromise between system efficiency and total solution size. The lower switching frequency can help reduce power losses and usually results in higher system efficiency, while the higher switching frequency allows the selection of smaller external components, such as inductors and output capacitors, and increases the system power density.

Setting Output Voltage

The external resistor divider network connected to the FB pin sets the output voltage. The resistance of the divider is a compromise between noise suppression and output current consumption. The smaller value resistor reduces noise sensitivity but also increases the quiescent current of the system and reduces light load efficiency. It is typically recommended to select a 10-kΩ resistor for the bottom feedback resistor. If low quiescent current and high light load efficiency are required, a larger

top feedback resistor can be selected, and one feedback capacitor can be used to improve the phase margin. Once the bottom feedback resistor is selected, the value of the top feedback resistor can be calculated with the equation below.

$$R_{FBB} = \frac{V_{FB} * R_{FBT}}{V_{OUT} - V_{FB}} \quad (5)$$

where V_{FB} is the internal reference voltage, which is typically 0.6 V for TPP21206. For a 1.2-V output, if R_{FBB} = 10 kΩ, R_{FBT} = 15.2 kΩ is chosen.

Inductor Selection

The selection of the inductor affects steady-state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications: inductor value, DC resistance, and saturation current. The inductor value is designed based on the desired peak-to-peak ripple current and is typically chosen to be in the range of 20% to 40% of the maximum output current. Once the desired inductor ripple current is selected, the inductor value can be calculated with the equation below.

$$L = \frac{V_{OUT}}{f_{SW} * \Delta I_L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

where f_{SW} is the switching frequency and ΔI_L is the inductor ripple current.

When the inductor current approaches its saturation level, the effective inductance can fall to a fraction of the zero current value. Although one high-side valley current limit is integrated to avoid the current runaway, the inductor current can rise to a high value very rapidly if the inductor is saturated. The inductor saturation current must leave a safe margin from the high-side peak current limit in the worst-case conditions. The RMS current and peak current of the inductor can be calculated with the equation below.

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (7)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (8)$$

Input Capacitor Selection

The input capacitor of the step-down regulator is used to supply the AC input current and maintain a stable DC input voltage. At least a 10-μF capacitance of ceramic input capacitor is recommended. Additional input capacitance may be required to meet ripple and transient requirements. A high-quality ceramic capacitor, X5R or X7R, is recommended because of low equivalent series resistance (ESR) characteristics and small capacitance variations over a temperature range. In addition, one small value and small case size, ceramic capacitor (such as 100 nF, 0603 package) is recommended to be used at the input and be placed as close as possible to the VIN and GND pins. This can provide a high-frequency bypass for the internal control circuits. The input capacitor can be calculated with the equation below when the input voltage ripple is determined.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

where C_{IN} is the input capacitance value.

The input capacitor ripple current rating should be greater than the maximum input current ripple. The RMS current of the input capacitor can be calculated with the equation below.

$$I_{CIN\_RMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (10)$$

The worst case for the input voltage ripple and RMS current occurs when the duty cycle is 50%.

Output Capacitor Selection

The output capacitance is mainly selected to meet the requirement of the output ripple and voltage change during a load transient. Then the control loop is compensated for the output capacitor selected. The output voltage ripple is related to the capacitance and ESR of the output capacitor. Assuming the capacitor has a small ESR, the minimum output capacitance needed for a given output ripple voltage can be calculated with the equation below.

$$C_{OUT} > \frac{\Delta I_L}{8 * f_{SW} * \Delta V_{OUT}} \quad (11)$$

where ΔI_L is the inductor ripple current and ΔV_{OUT} is the output voltage ripple.

If a large ESR capacitor is used, it contributes additional output ripple. ESR ripples can be neglected for ceramic capacitors but must be considered if electrolytic capacitors are used. The maximum ESR for a given ripple can be calculated with the equation below.

$$R_{ESR} < \frac{\Delta V_{OUT}}{\Delta I_L} - \frac{1}{8 * f_{SW} * C_{OUT}} \quad (12)$$

The effective value of the ceramic capacitor decrease should be considered when the output DC bias voltage is added across the capacitors. The RMS current of the output capacitor can be calculated with the equation below.

$$I_{COUT\_RMS} = \frac{V_{OUT} * (V_{IN\_MAX} - V_{OUT})}{\sqrt{12} * V_{IN\_MAX} * L * f_{SW}} \quad (13)$$

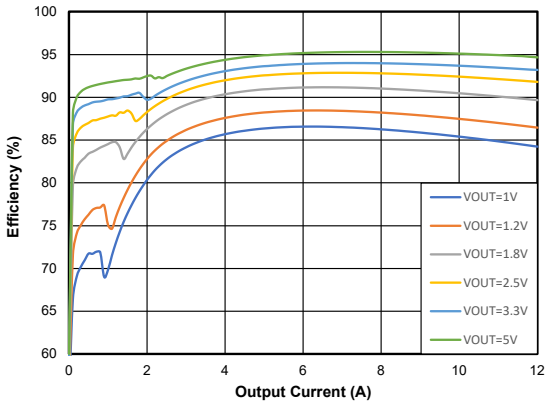
where V_{IN_MAX} is the maximum input voltage, and L is the selected inductor value.

Bootstrap Capacitor Selection

A typical 0.1-μF bootstrap capacitor is connected between the BOOT pin and the SW pin. It is recommended to use a ceramic capacitor with X5R or superior grade dielectric and a voltage rating of 10 V or higher.

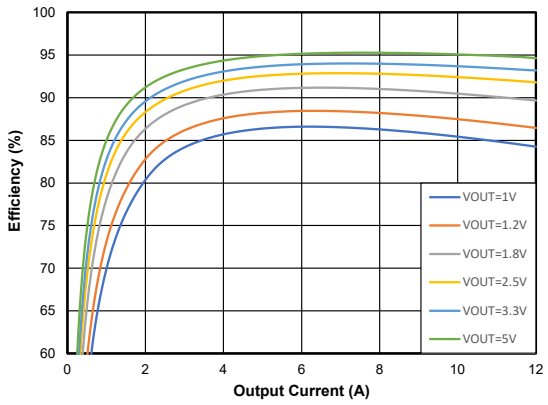
Application Waveforms

All test conditions: V_{IN} = 12 V, V_{OUT} = 1.2 V, F_{SW} = 800 kHz, FPWM Mode, T_A = 25 °C, unless otherwise noted.



PFM Mode

Figure 16. Efficiency



FPWM Mode

Figure 17. Efficiency

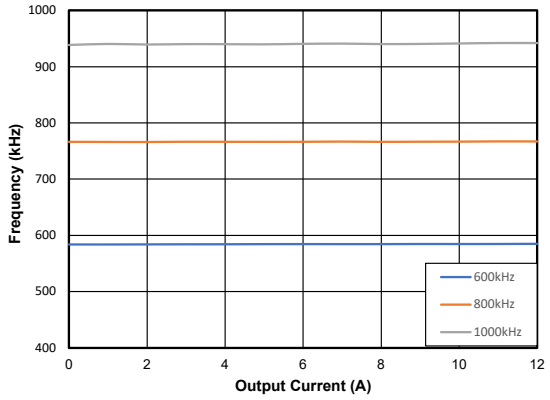


Figure 18. Switching Frequency vs. Output Current

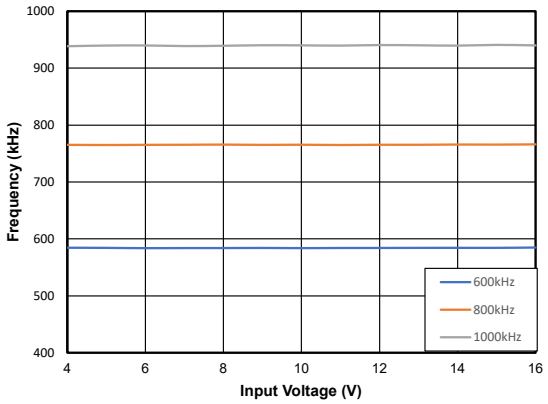


Figure 19. Switching Frequency vs. Input Voltage

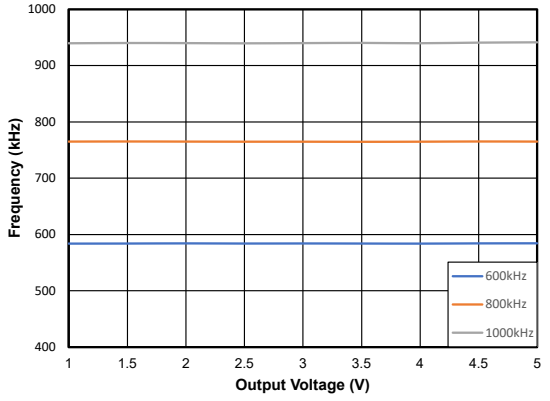
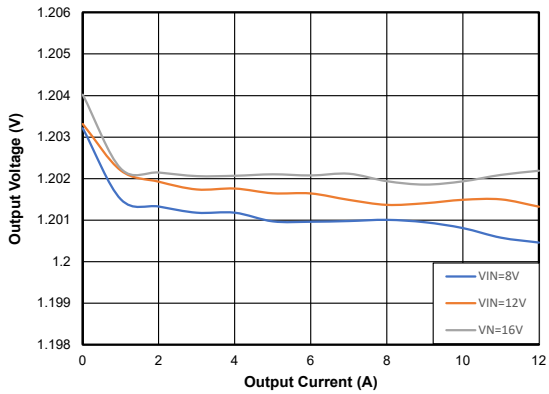
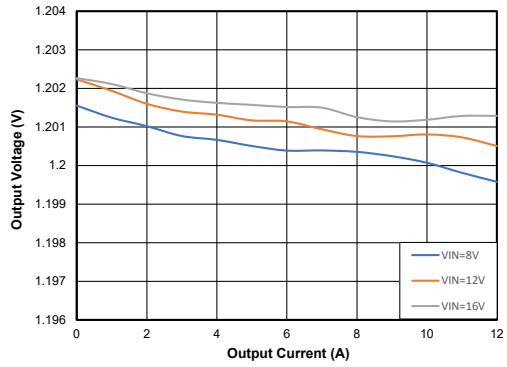


Figure 20. Switching Frequency vs. Output Voltage



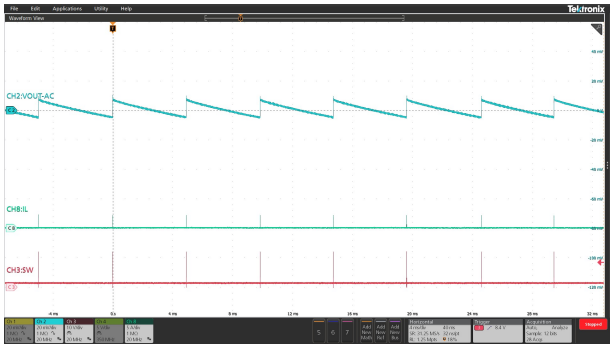
PFM Mode

Figure 21. Load Regulation



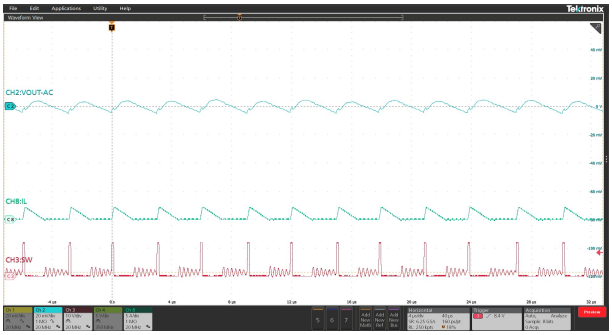
FPWM Mode

Figure 22. Load Regulation



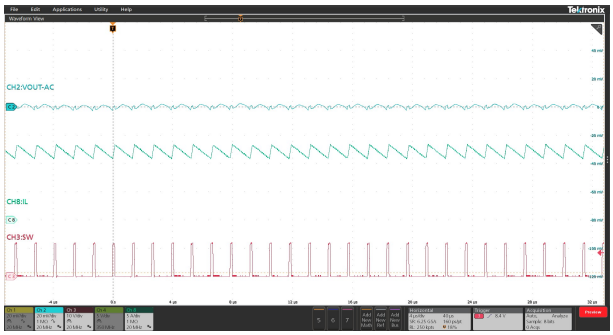
I_{OUT} = 0 A, PFM Mode

Figure 23. Switching Waveform and Output Ripple



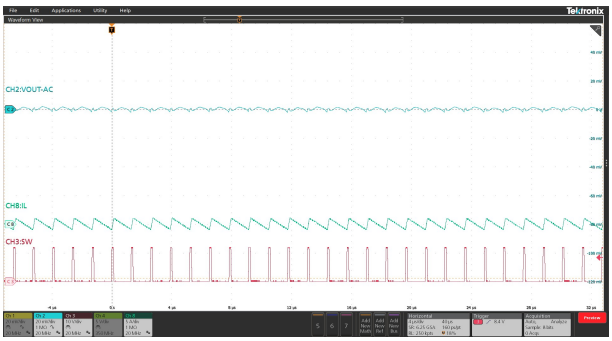
I_{OUT} = 0.5 A, PFM Mode

Figure 24. Switching Waveform and Output Ripple



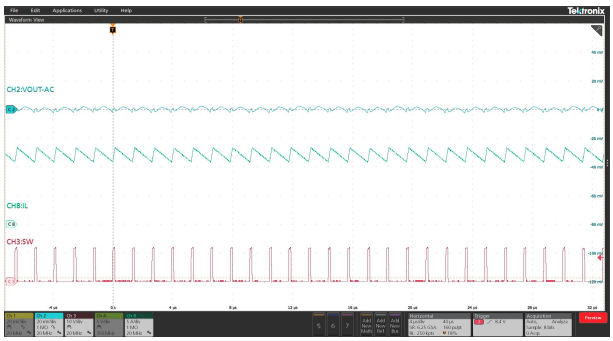
I_{OUT} = 12 A, PFM Mode

Figure 25. Switching Waveform and Output Ripple



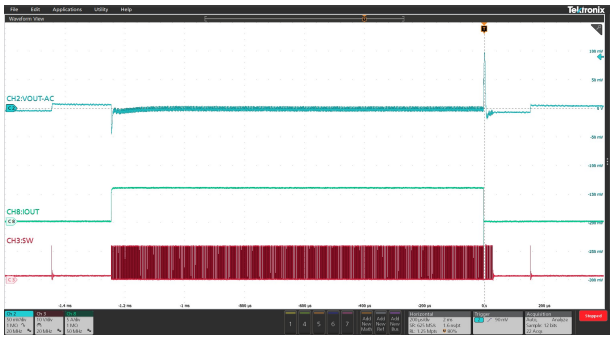
I_{OUT} = 0 A, FPWM Mode

Figure 26. Switching Waveform and Output Ripple



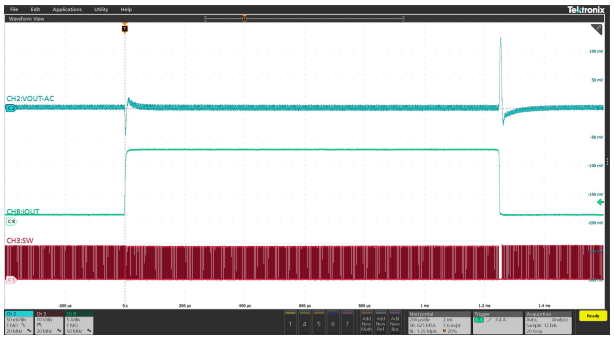
I_{OUT} = 12 A, FPWM Mode

Figure 27. Switching Waveform and Output Ripple



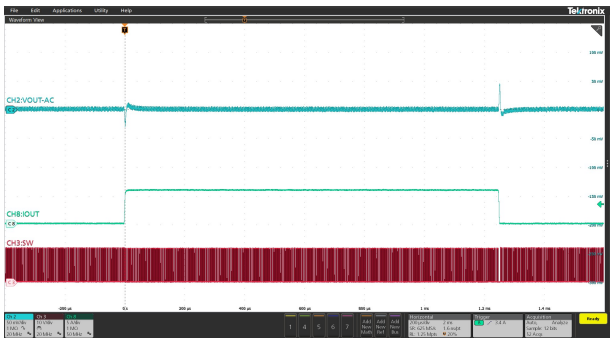
I_{OUT} = 0 A to 6 A to 0 A, PFM Mode

Figure 28. Load Transient



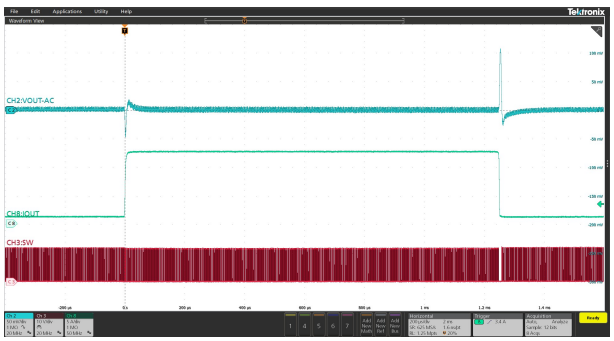
I_{OUT} = 1.2 A to 12 A to 1.2 A, PFM Mode

Figure 29. Load Transient



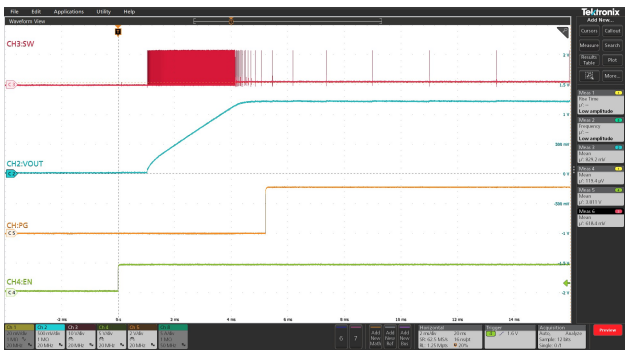
I_{OUT} = 0 A to 6 A to 0 A, FPWM Mode

Figure 30. Load Transient



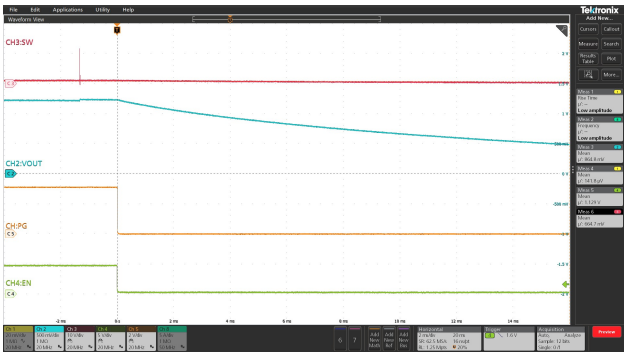
I_{OUT} = 1.2 A to 12 A to 1.2 A, FPWM Mode

Figure 31. Load Transient



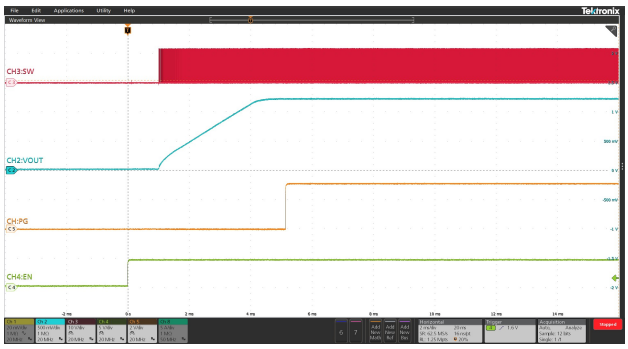
I_{OUT} = 0 A, PFM Mode

Figure 32. Power up by Enabling



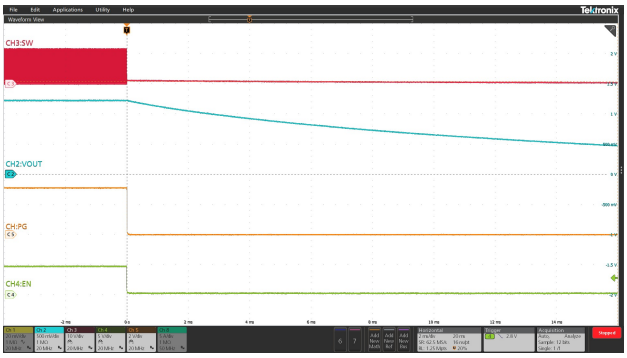
I_{OUT} = 0 A, PFM Mode

Figure 33. Power down by Enabling



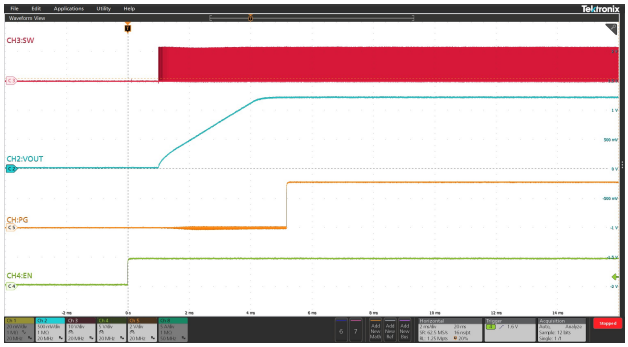
I_{OUT} = 0 A, FPWM Mode

Figure 34. Power up by Enabling



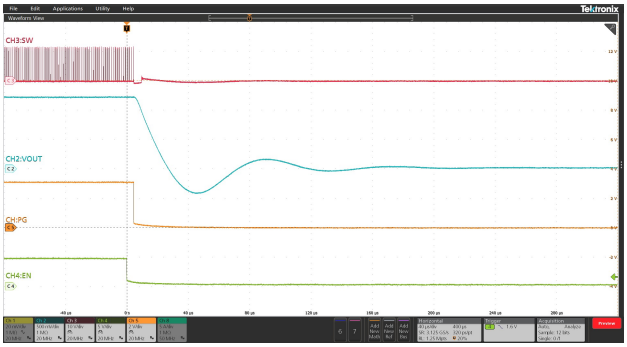
I_{OUT} = 0 A, FPWM Mode

Figure 35. Power down by Enabling



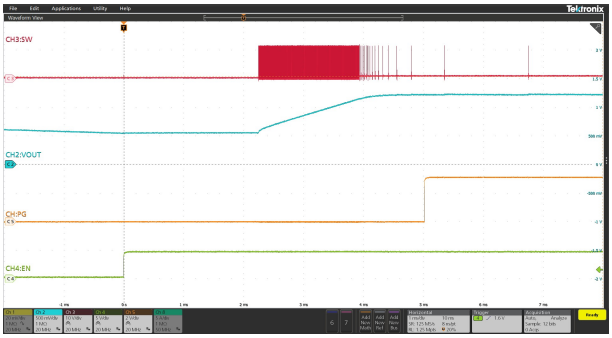
I_{OUT} = 12 A, FPWM Mode

Figure 36. Power up by Enabling



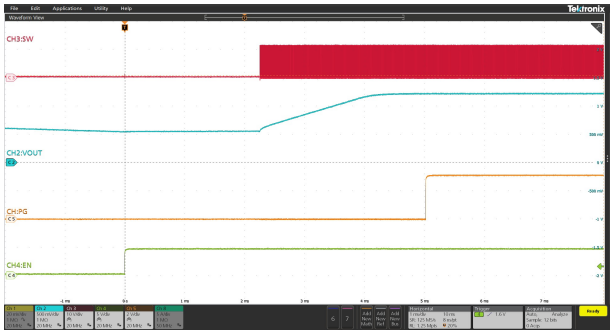
I_{OUT} = 12 A, FPWM Mode

Figure 37. Power down by Enabling



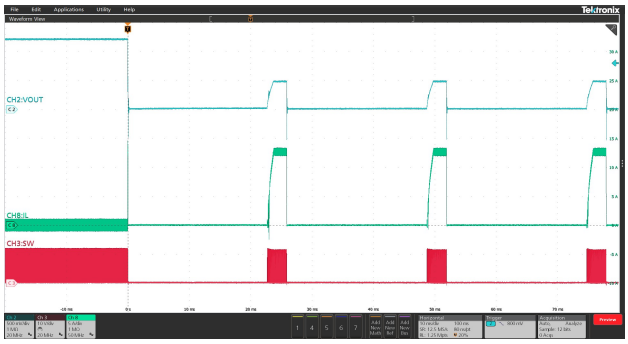
PFM Mode

Figure 38. Pre-bias Power Up



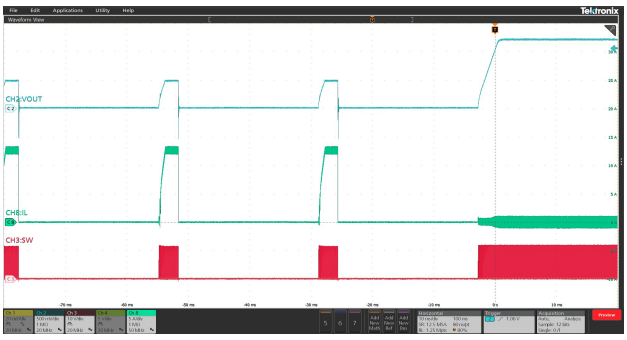
FPWM Mode

Figure 39. Pre-bias Power Up



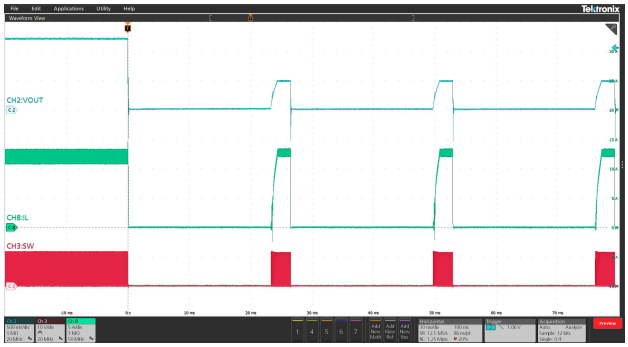
I_{OUT} = 0 A

Figure 40. Hiccup Protection Entry



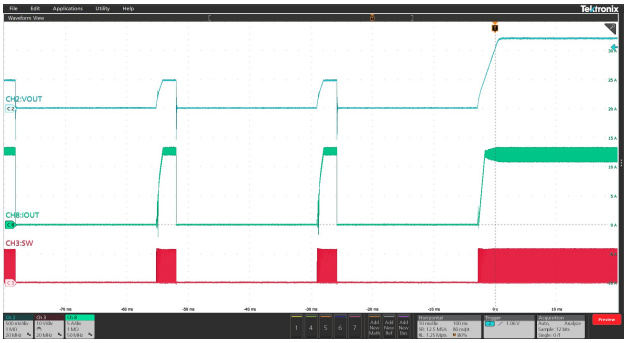
I_{OUT} = 0 A

Figure 41. Hiccup Protection Recovery



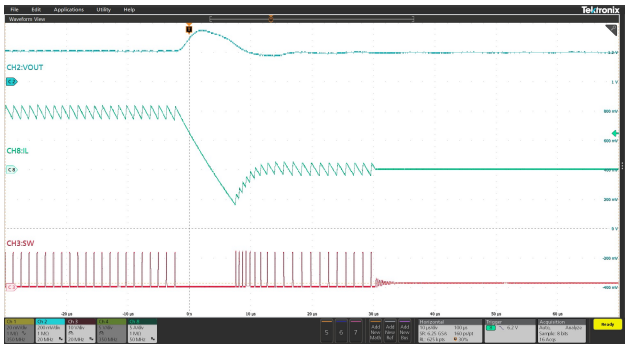
I_{OUT} = 12 A

Figure 42. Hiccup Protection Entry



I_{OUT} = 12 A

Figure 43. Hiccup Protection Recovery

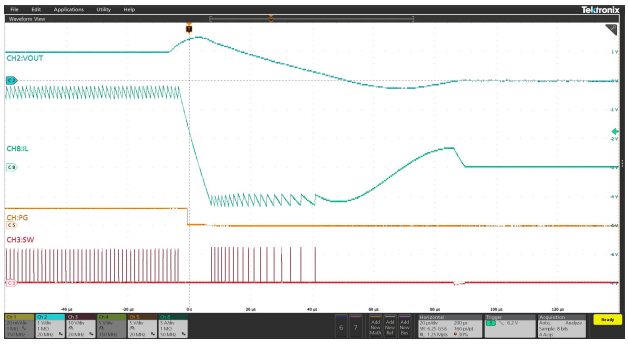


PFM Mode

Figure 44. Output Limitation Protection

PFM Mode

Figure 45. Over Voltage Protection



FPWM Mode

Figure 46. Over Voltage Protection

Layout

Layout Guideline

The performance of switching regulators heavily depends on the quality of the PCB layout, especially for thermal design and EMI design. Even if the schematic design is good, an inappropriate PCB layout can disrupt the operation of the regulator.

1. The input MLCC capacitors should be placed as close to the VIN and PGND pins as possible.

2. The major MLCC capacitors should be placed on the same layer as the TPP21206.

3. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.

4. Place as many PGND vias as possible close to the PGND pins to minimize both parasitic impedance and thermal resistance.

5. Place the VCC decoupling capacitor as close as possible to the device.

6. Connect AGND and PGND at the point of the ground connection of the VCC capacitor.

7. Place the BOOT capacitor as close as possible to the BOOT and SW pins with wider traces to route the path.

8. Place the SS/TR capacitor close to the SS/TR pin to RGND.

9. The feedback terminal is sensitive to noise, so the feedback resistor should be placed as close as possible to the device. Do not place vias on the feedback output and ground sense trace.

Layout Recommendations

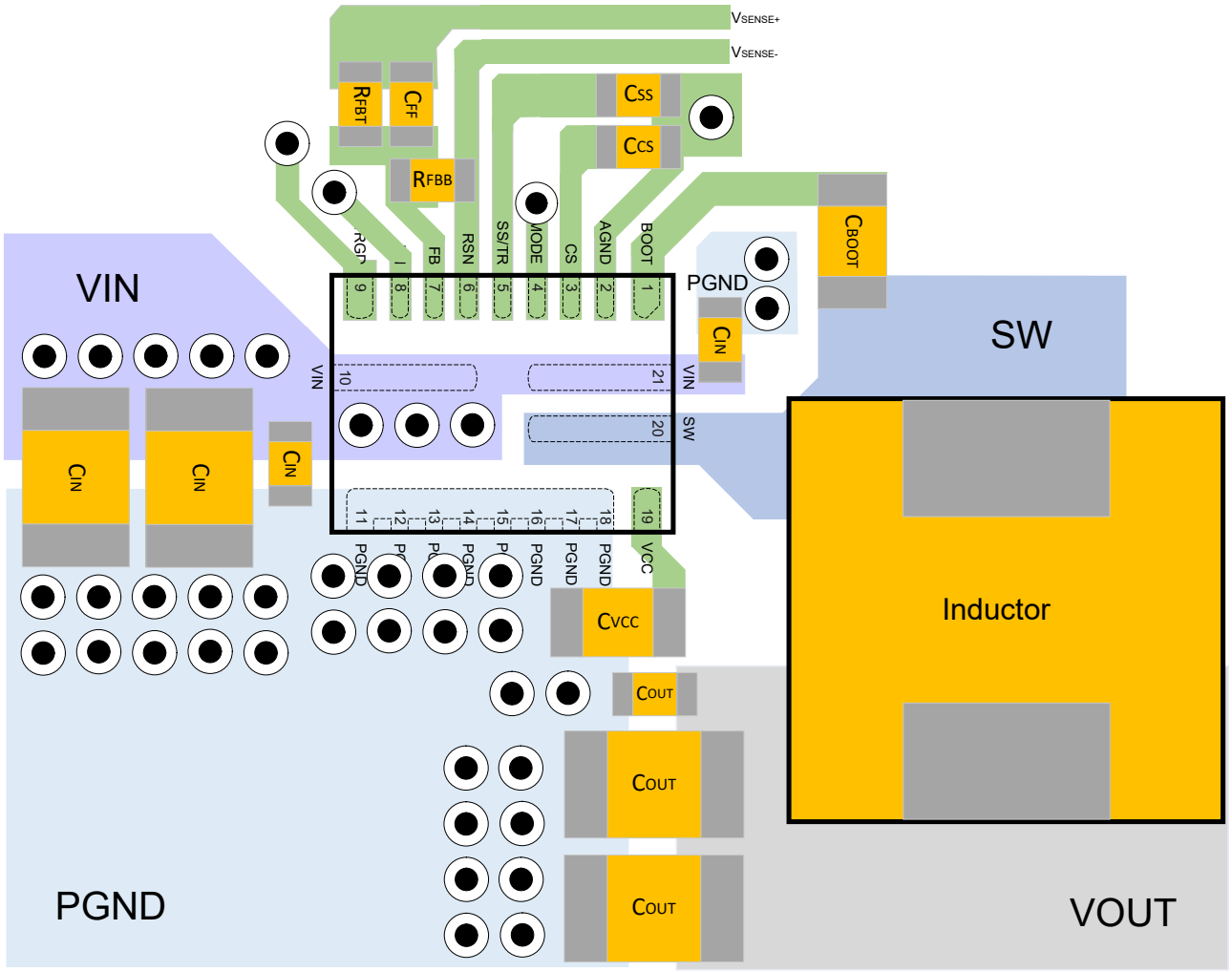
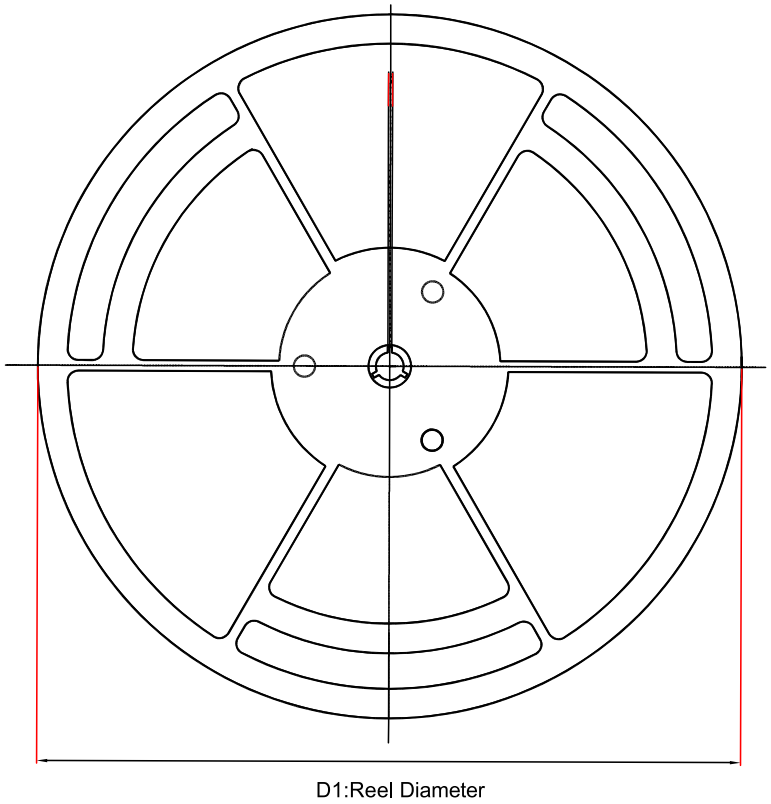
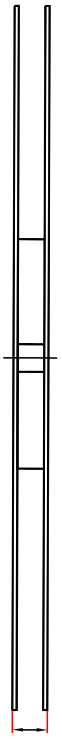
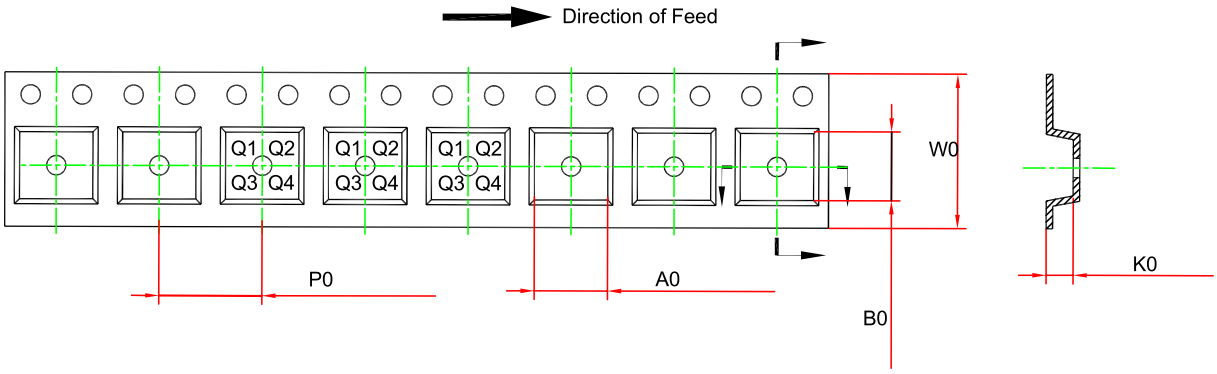


Figure 47. Layout Example

Tape and Reel Information





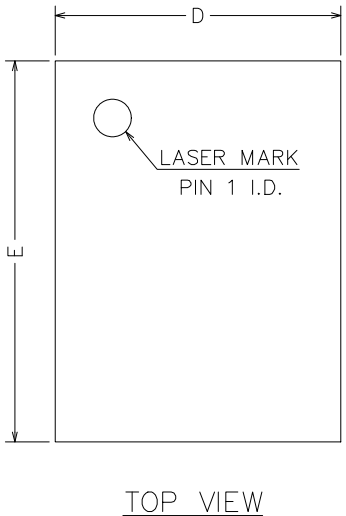


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPP212060-FC5R	QFN3X4-21	330	17.6	3.3	4.3	1.0	8.0	12.0	Q1

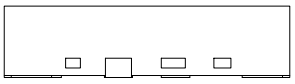
Package Outline Dimensions

QFN3X4-21

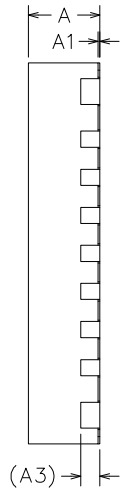
Package Outline Dimensions QFW(QFN3X4-21-A)



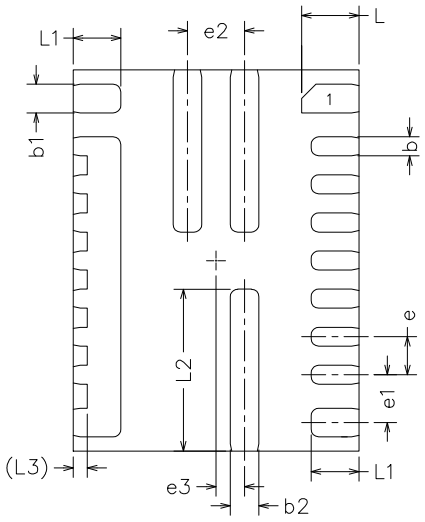
TOP VIEW



SIDE VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.150	0.250	0.006	0.010
A3	0.203 REF		0.008 REF	
b1	0.250	0.350	0.010	0.014
b2	0.250	0.350	0.010	0.014
D	3.000 BSC		0.118 BSC	
E	4.000 BSC		0.157 BSC	
e	0.400 BSC		0.016 BSC	
e1	0.500 BSC		0.020 BSC	
e2	0.600 BSC		0.024 BSC	
e3	0.300 BSC		0.012 BSC	
L	0.550	0.650	0.022	0.026
L1	0.450	0.550	0.018	0.022
L2	1.630	1.770	0.064	0.070
L3	0.150REF		0.006REF	

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPP212060-FC5R	−40°C to 125°C	QFN3X4-21	2120	Level 3	Tape & Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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